SIM8960 Series Hardware Design

Smart Module

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2020-03-03	V1.01	Initial release	Bing Li
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2020-06-08	V1.03	Add current consumption and modify document format	Daofu yang

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1 Introduction

This document describes the electronic specifications, RF specifications, interfaces, mechanical characteristics and testing results of the SIMCom module. With the help of this document and other software application notes/user guides, users can understand and use module to design and develop applications quickly.

1.1 Product Outline

SIM8960x is a multi-mode and multi-band wireless smart module, which is based on Qualcomm SDM450 platform.

- 14nm FinFET ,64-bit ARM Cortex-A53 octa-core at 1.8GHz
- Non-PoP 2GB LPDDR3 SDRAM designed for 933Mhz clock.
- 16GB eMMC Flash
- Qualcomm Adreno 506 GPU at 600MHz, with 64-bit addressing
- Rich multimedia features: Support Dual-LCM, two cameras and multi-path analog audio IO
- Support for USB3.0 and SD3.0
- Global location-based service, wireless connectivity, and air interface standards including GSM, WCDMA, TD-SCDMA, and LTE.

With higher integration to reduce PCB surface area, time-to-market, and BOM costs, SIM8960x will help drive wireless products adoption in more industry around the world.

The operating bands are different between SIM8960x variants, which are summarized in Table 1.

Table 1: Module frequency bands

Module		SIM8960CE	SIM8960E	SIM8060
CPU clock speed		1.8GHz	1.8GHz	1.8GHz
Memory	**RAM**	2GB	2GB	2GB
	ROM	16GB	16GB	16GB
Standard & Frequency				
GSM	GSM850			
	EGSM900	✓	✓	

	DCS1800	✓	✓	
	PCS1900			
WCDMA	B1	✓	✓	
	B2			
	B4			
	B5		✓	
	B8	✓	✓	
TDSCDMA	B34	✓		
	B39	✓		
FDD-LTE	B1	✓	✓	
	B2			
	B3	✓	✓	
	B4			
	B5	✓	✓	
	B7		✓	
	B8	✓	✓	
	B12			
	B13			
	B14			
	B17			
	B18			
	B19			
	B20		✓	
	B25			
	B26			
	B28A			
	B28B			
	B66			
	B71			
TDD-LTE	B34	✓		
	B38	✓	✓	
	B39	✓		
	B40	✓	✓	
	B41	✓	✓	
WLAN 2.4G	802.11b/g/n/ac	✓	✓	✓
WLAN 5G	802.11a/n/ac	✓	✓	✓
BT	BT4.2 LE	✓	✓	✓
GNSS	GPS	✓	✓	
	GLONASS	✓	✓	
	BEIDOU	✓	✓	

With a small physical dimension of 43×44×2.85mm and with the functions integrated, the module can meet almost any space requirement in users' applications, such as smart phone, PDA, industrial handhold, machine-to-machine and vehicle application, etc.

1.2 Hardware Interface Overview

The interfaces are described in detail in the next chapters include:

- Power Supply
- USB2.0/3.0 Interface
- SDIO /SD Interface
- LCM Interface(MIPI DSI)
- Camera Interface(MIPI CSI0/CSI1/CSI2)
- USIM Interface
- GPIO
- ADC
- LDO Power Output
- AUDIO Interface (Three inputs and Four outputs)
- UART Interface
- SPI Interface
- I2C Interface

1.3 Hardware Block Diagram

The block diagram of the module is shown in the figure below.

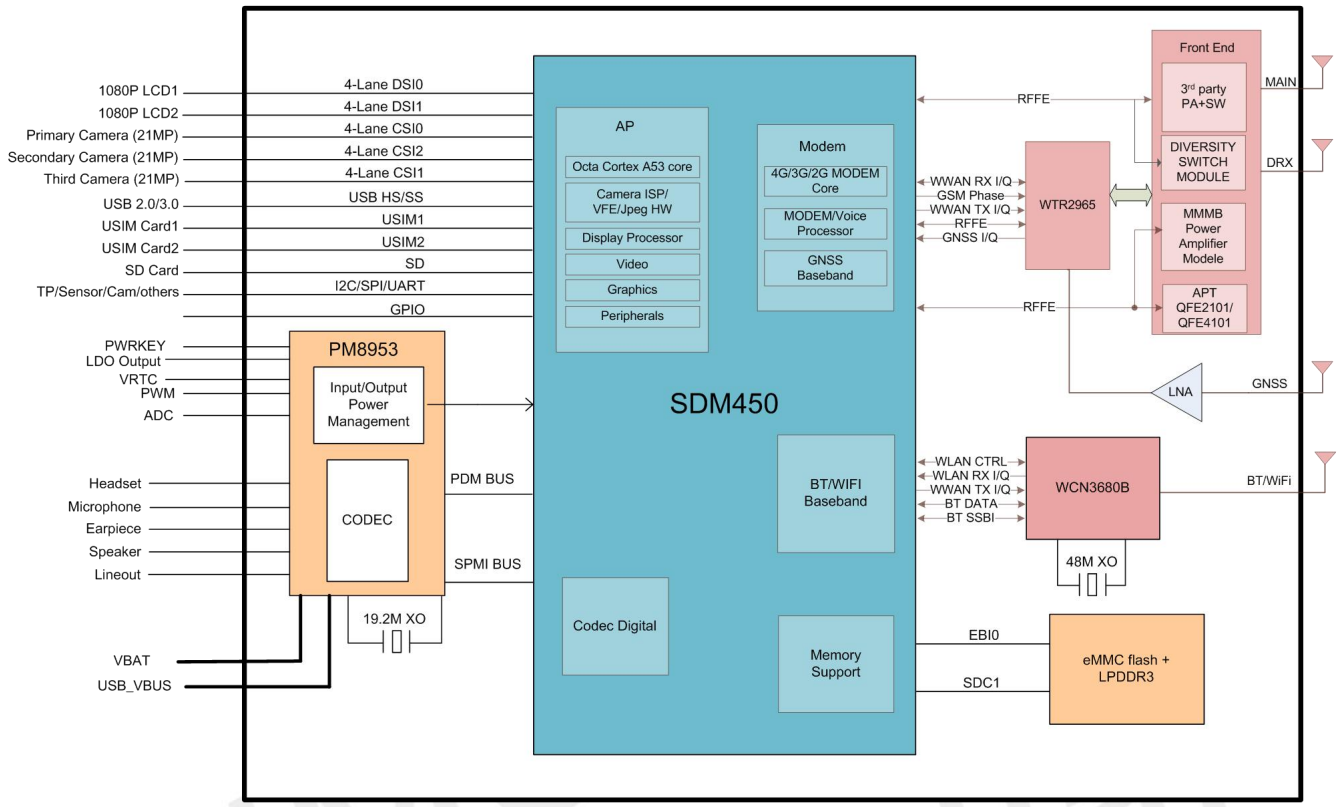

Figure 1: SIM8960x functional diagram

1.4 Functional Overview

Table 2: General features

Feature	Implementation
Power supply	3.4V ~4.4V
Power saving	Current in sleep mode : <5mA
Application processor	Octa ARM Cortex-A53 cores up to 1.8 GHz
Memory	LPDDR3 up to 933Mhz eMMC NAND flash Please refer to the table 1 Customization: 3GB eMMC + 32GB LPDDR3 4GB eMMC + 64GB LPDDR3
Operating system	Android OS 7.x/8.x/9.x
Display	Dual MIPI DSI four-lane FHD (1920 × 1200) 60 fps; 16/18/24 bpp RGB
Camera	Three mipi_csi interfaces with a maximum speed of 2.1gbps/lane Support Three cameras (4-lane + 4-lane + 4-lane) or Four cameras (4-lane + 4-lane + 2-lane + 1-lane)

	4-lane Mipi_CSI: up to 21mp pixels 2-lane Mipi_CSI: up to 8mp
Video performance	Encode: 1080p60, H.264, H.265, and VP8 Decode: 1080p60, H.264, H.265, VP8, and VP9
Audio	One digital port I2S, support both master and slave mode Three analog input ports: MIC1 supports differential configuration MIC2 supports single-ended configuration MIC3 supports single-ended configuration Supports dual-mic noise suppression 16, 32, and 48 KHzsample rate Four analog output ports: earpiece, stereo headphones, class-D speaker driver ,and line out 16, 32, 48, 96 and 192 KHz sample rate Audio codec support: G711; QCELP; EVRC, EVRC-B, EVRC-WB; AMR-NB, AMR-WB; GSM-EFR, GSM-FR, GSM-HR
Radio frequency bands	Please refer to the table 1
Transmitting power	Class 4 (33dBm±2dB) for EGSM900 Class 1 (30dBm±2dB) for DCS1800 Class E2 (27dBm±3dB) for EGSM900 8-PSK Class E2 (26dBm±3dB) for DCS1800 8-PSK Class 3 (24dBm+1/-3dB) for WCDMA bands Class 2 (24dBm+1/-3dB) for TD-SCDMA bands Class 3 (23dBm±2dB) for LTE-FDD bands Class 3 (23dBm±2dB) for LTE-TDD bands
LTE features	● Support 3GPP R8 Cat.4 ● Support 1.4 ~ 20MHz RF bandwidth ● Support MIMO in DL direction ● Cat.4 FDD: Max 150Mbps (DL)/Max 50Mbps (UL) ● Cat.4 TDD: Max 130Mbps (DL)/Max 35Mbps (UL)
UMTS features	● Support 3GPP R9 DC-HSDPA/HSPA+/HSDPA/HSUPA/WCDMA ● Support QPSK, 16-QAM and 64-QAM modulation ● DC-HSDPA: Max 42Mbps (DL) ● DC-HSUPA: Max 11.2Mbps (UL) ● WCDMA: Max 384Kbps (DL)/Max 384Kbps (UL)
TD-SCDMA features	● Support CCSA Release 3 TD-SCDMA ● Max 4.2Mbps (DL)/Max 2.2Mbps (UL)
GSM features	● R99: ● CSD: 9.6kbps, 14.4kbps ● GPRS: ● Support GPRS multi-slot class 33 (default) ● Coding scheme: CS-1, CS-2, CS-3 and CS-4

	● Max 85.6Kbps (UL), 107Kbps (DL) ● EDGE: ● Support EDGE multi-slot class 33 (default) ● Support GMSK and 8-PSK for different MCS ● Downlink coding schemes: CS 1-4 and MCS 1-9 ● Uplink coding schemes: CS 1-4 and MCS 1-9 ● Max 236.8Kbps (UL), 296Kbps (DL)
Bluetooth features	BT2.1+EDR /3.0 /4.2 LE
WLAN features	2.4G/5GHz, 802.11a/b/g/n/ac, up to 433Mbps Support AP mode
GNSS	GPS /GLONASS /BEIDOU
Antenna	GSM/UMTS/LTE main antenna. UMTS/LTE auxiliary antenna GNSS antenna WIFI/BT antenna
USIM interface	Support identity card: 1.8V/ 2.95V Dual cards dual standby
UART	4*UART UART2: for debug，2-line UART4: 2-line UART5 & UART6 are 4-line that support RTS and CTS hardware flow control, the speed can up to 4Mbps.
I2C	10* I2C
SPI	7* SPI
eMMC/SD/SDIO	SD3.0; Support SD flash devices up to 128GB
ADC	1*ADC (15bit) Detection range: 0.1V~1.7V or 0.3V~4.5V (software controlled)
USB	One USB 3.0/2.0 Support Type-C Support OTG (external 5V power supply is needed)
Physical features	Dimension: 43.0(±0.2)×44.0(±0.2) ×2.85(±0.2)mm Weight: about 12.5g
Temperature range	Operating temperature: -35℃ ~ +75℃ [1] Extreme operating temperature：-40℃ ~ +85℃ [2] Storage temperature: -40℃ ~ +90℃

NOTE

1. Module can operate in the -35℃ ~ +75℃ range, and the performance can be meet the 3GPP specifications.

2. Module is working when the temperature change to -40℃ ~ +85℃,Module is able to make and receive voice calls, data calls, SMS and make GPRS/UMTS/HSPA+/LTE traffic. The performance will be reduced slightly from the 3GPP specifications if the temperature is outside the normal operating temperature range and still within the extreme operating temperature range.

1.5 Evaluation board

SIMCom provides a complete set of evaluation boards to facilitate the test and use of SIM8960x module. The evaluation board tool comprises an EVB board, a SIM8960-TE core board, a USB data cable, a headset, an antenna, an adapter and other peripherals.

2 Package Information

2.1 Pin Assignment Overview

All functions of the module will be provided through 327 pads that will be connected to the customers' platform. The following Figure is a high-level view of the pin assignment of the module.

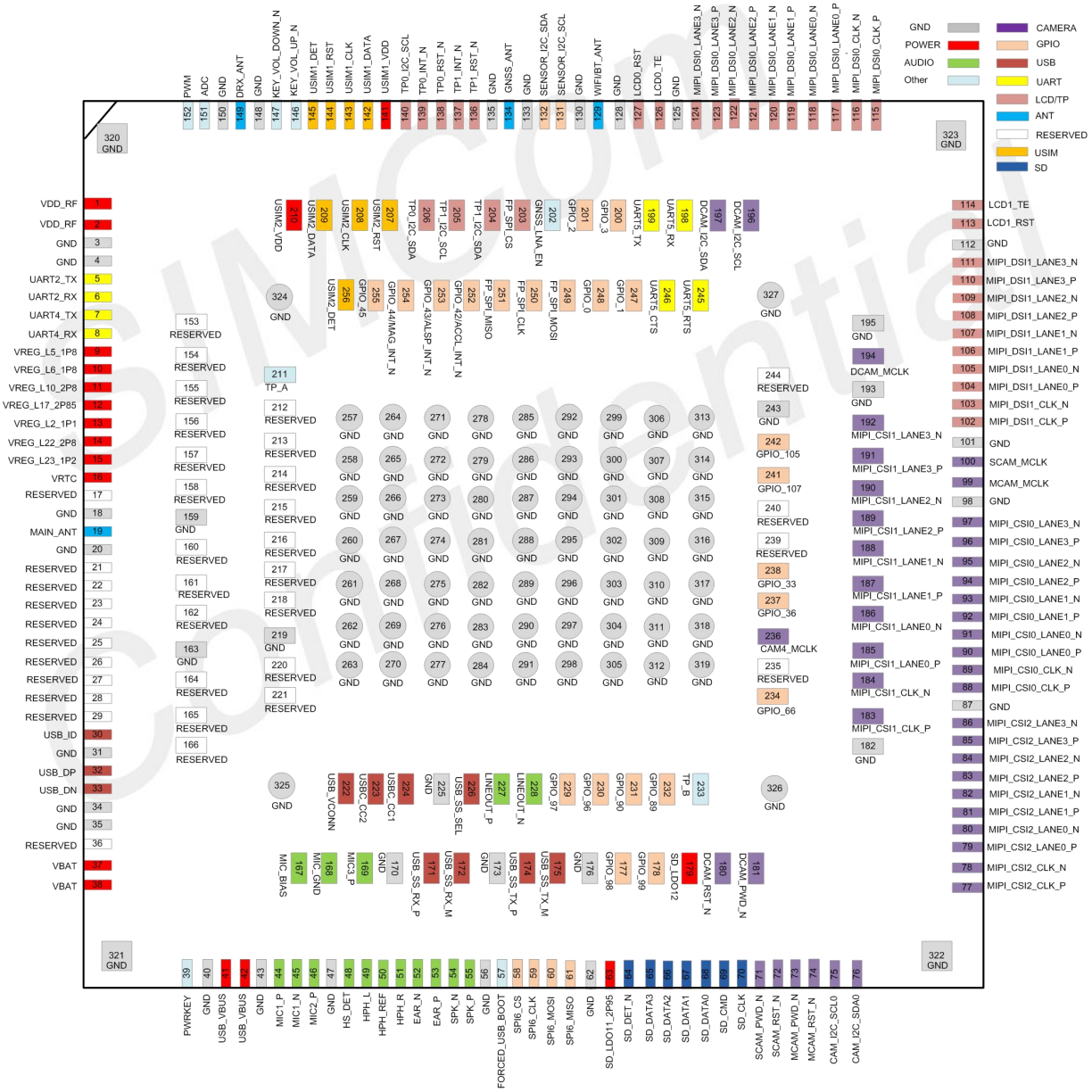

Figure 2: Pin assignment overview

2.2 Pin Description

Table 3: Pin Characters

Pin#	Pin Name	Voltage	SDM450 Platform	Pin#	Pin Name	Note
1	VDD_RF					
2	VDD_RF					
3	GND					
4	GND					
5	UART2_TX	1.8V	GPIO_4	I-PD		
6	UART2_RX	1.8V	GPIO_5	I-PD		
7	UART4_TX	1.8V	GPIO_12	I-PD		
8	UART4_RX	1.8V	GPIO_13	I-PD	√	
9	VREG_L5_1P8	1.8V				
10	VREG_L6_1P8	1.8V				
11	VREG_L10_2P8	2.8V				
12	VREG_L17_2P85	2.85V				
13	VREG_L2_1P1	1.1V				
14	VREG_L22_2P8	2.8V				
15	VREG_L23_1P2	1.2V				
16	VRTC	3V				
17	RESERVED					
18	GND					
19	MAIN_ANT					
20	GND					
21	RESERVED					
22	RESERVED					
23	RESERVED					
24	RESERVED					
25	RESERVED					
26	RESERVED					
27	RESERVED					
28	RESERVED					
29	RESERVED					
30	USB_ID					
31	GND					
32	USB_DP					
33	USB_DN					
34	GND					
35	GND					

36	RESERVED					
37	VBAT	3.4~4.4V				
38	VBAT	3.4~4.4V				
39	PWRKEY	1.8V				
40	GND					
41	USB_VBUS	5V				
42	USB_VBUS	5V				
43	GND					
44	MIC1_P					
45	MIC1_N					
46	MIC2_P					
47	GND					
48	HS_DET					
49	HPH_L					
50	HPH_REF					
51	HPH_R					
52	EAR_N					
53	EAR_P					
54	SPK_N					
55	SPK_P					
56	GND					
57	FORCED_USB_BOOT	1.8V	GPIO_37	I-PD	√	
58	SPI6_CS	1.8V	GPIO_22	I-PD		
59	SPI6_CLK	1.8V	GPIO_23	I-PD		
60	SPI6_MOSI	1.8V	GPIO_20	I-PD		
61	SPI6_MISO	1.8V	GPIO_21	I-PD	√	
62	GND					
63	SD_LDO11_2P95	2.95V				
64	SD_DET_N	1.8V	GPIO_133	I-PD	√	
65	SD_DATA3	1.8/2.95		BH-P		
66	SD_DATA2	1.8/2.95 V		BH-P D		
67	SD_DATA1	1.8/2.95 V		BH-P D		
68	SD_DATA0	1.8/2.95 V		BH-P D		
69	SD_CMD	1.8/2.95 V		BH-P D		
70	SD_CLK	1.8/2.95 V		BHNP		
71	SCAM_PWD_N	1.8V	GPIO_130	I-PD	√	
72	SCAM_RST_N	1.8V	GPIO_129	I-PD	√	
73	MCAM_PWD_N	1.8V	GPIO_39	I-PD		

74	MCAM_RST_N	1.8V	GPIO_40	I-PD		
75	CAM_I2C_SCL0	1.8V	GPIO_30	I-PD		
76	CAM_I2C_SDA0	1.8V	GPIO_29	I-PD		
77	MIPI_CSI2_CLK_P					
78	MIPI_CSI2_CLK_N					
79	MIPI_CSI2_LANE0_P					
80	MIPI_CSI2_LANE0_N					
81	MIPI_CSI2_LANE1_P					
82	MIPI_CSI2_LANE1_N					
83	MIPI_CSI2_LANE2_P					
84	MIPI_CSI2_LANE2_N					
85	MIPI_CSI2_LANE3_P					
86	MIPI_CSI2_LANE3_N					
87	GND					
88	MIPI_CSI0_CLK_P					
89	MIPI_CSI0_CLK_N					
90	MIPI_CSI0_LANE0_P					
91	MIPI_CSI0_LANE0_N					
92	MIPI_CSI0_LANE1_P					
93	MIPI_CSI0_LANE1_N					
94	MIPI_CSI0_LANE2_P					
95	MIPI_CSI0_LANE2_N					
96	MIPI_CSI0_LANE3_P					
97	MIPI_CSI0_LANE3_N					
98	GND					
99	MCAM_MCLK	1.8V	GPIO_26	I-PD		
100	SCAM_MCLK	1.8V	GPIO_27	I-PD		
101	GND					
102	MIPI_DSI1_CLK_P					
103	MIPI_DSI1_CLK_N					
104	MIPI_DSI1_LANE0_P					
105	MIPI_DSI1_LANE0_N					
106	MIPI_DSI1_LANE1_P					
107	MIPI_DSI1_LANE1_N					
108	MIPI_DSI1_LANE2_P					
109	MIPI_DSI1_LANE2_N					
110	MIPI_DSI1_LANE3_P					
111	MIPI_DSI1_LANE3_N					
112	GND					
113	LCD1_RST	1.8V	GPIO_87	I-PD	√	
114	LCD1_TE	1.8V	GPIO_25	I-PD	√	

115	MIPI_DSI0_CLK_P					
116	MIPI_DSI0_CLK_N					
117	MIPI_DSI0_LANE0_P					
118	MIPI_DSI0_LANE0_N					
119	MIPI_DSI0_LANE1_P					
120	MIPI_DSI0_LANE1_N					
121	MIPI_DSI0_LANE2_P					
122	MIPI_DSI0_LANE2_N					
123	MIPI_DSI0_LANE3_P					
124	MIPI_DSI0_LANE3_N					
125	GND					
126	LCD0_TE	1.8V	GPIO_24	I-PD		
127	LCD0_RST	1.8V	GPIO_61	I-PD	√	
128	GND					
129	WIFI/BT_ANT					
130	GND					
131	SENSOR_I2C_SCL	1.8V	GPIO_15	I-PD		
132	SENSOR_I2C_SDA	1.8V	GPIO_14	I-PD		
133	GND					
134	GNSS_ANT					
135	GND					
136	TP1_RST_N	1.8V	GPIO_8	I-PD		
137	TP1_INT_N	1.8V	GPIO_9	I-PD	√	
138	TP0_RST_N	1.8V	GPIO_64	I-PD		
139	TP0_INT_N	1.8V	GPIO_65	I-PD	√	
140	TP0_I2C_SCL	1.8V	GPIO_11	I-PD		
141	USIM1_VDD	1.8 / 2.95 V				
142	USIM1_DATA	1.8 / 2.95 V	GPIO_51	I-PD		Can not be used as GPIO
143	USIM1_CLK	1.8 / 2.95 V	GPIO_52	I-PD		
144	USIM1_RST	1.8 / 2.95 V	GPIO_53	I-PD		
145	USIM1_DET	1.8V	GPIO_54	I-PD	√	
146	KEY_VOL_UP_N	1.8V	GPIO_85	I-PD	√	Cannot be pull down externally
147	KEY_VOL_DOWN_N	1.8V				
148	GND					
149	DRX_ANT					
150	GND					

151	ADC		PM8953_MPP2		
152	PWM		PM8953_MPP4		
153	RESERVED				
154	RESERVED				
155	RESERVED				
156	RESERVED				
157	RESERVED				
158	RESERVED				
159	GND				
160	RESERVED				
161	RESERVED				
162	RESERVED				
163	GND				
164	RESERVED				
165	RESERVED				
166	RESERVED				
167	MIC_BIAS	1.6~2.85V			
168	MIC_GND				
169	MIC3_P				
170	GND				
171	USB_SS_RX_P				
172	USB_SS_RX_M				
173	GND				
174	USB_SS_TX_P				
175	USB_SS_TX_M				
176	GND				
177	GPIO_98	1.8V	GPIO_98	I-PD	
178	GPIO_99	1.8V	GPIO_99	I-PD	
179	SD_LDO12	1.8 / 2.95 V			
180	DCAM_RST_N	1.8V	GPIO_131	I-PD	√
181	DCAM_PWD_N	1.8V	GPIO_132	I-PD	√
182	GND				
183	MIPI_CSI1_CLK_P				
184	MIPI_CSI1_CLK_N				
185	MIPI_CSI1_LANE0_P				
186	MIPI_CSI1_LANE0_N				
187	MIPI_CSI1_LANE1_P				
188	MIPI_CSI1_LANE1_N				
189	MIPI_CSI1_LANE2_P				
190	MIPI_CSI1_LANE2_N				

191	MIPI_CSI1_LANE3_P					
192	MIPI_CSI1_LANE3_N					
193	GND					
194	DCAM_MCLK	1.8V	GPIO_28	I-PD	√	
195	GND					
196	DCAM_I2C_SCL	1.8V	GPIO_32	I-PD		
197	DCAM_I2C_SDA	1.8V	GPIO_31	I-PD	√	
198	UART5_RX	1.8V	GPIO_17	I-PD	√	
199	UART5_TX	1.8V	GPIO_16	I-PD		
200	GPIO_3	1.8V	GPIO_3	I-PD		
201	GPIO_2	1.8V	GPIO_2	I-PD		
202	GNSS_LNA_EN	1.8V	GPIO_116	I-PD		
203	FP_SPI_CS	1.8V	GPIO_136	I-PD		
204	TP1_I2C_SDA	1.8V	GPIO_6	I-PD		
205	TP1_I2C_SCL	1.8V	GPIO_7	I-PD		
206	TP0_I2C_SDA	1.8V	GPIO_10	I-PD		
207	USIM2_RST	1.8 / 2.95 V	GPIO_57	I-PD		Can not be used as GPIO
208	USIM2_CLK	1.8 / 2.95 V	GPIO_56	I-PD		
209	USIM2_DATA	1.8 / 2.95 V	GPIO_55	I-PD		
210	USIM2_VDD	1.8 / 2.95 V				
211	TP_A					
212	RESERVED					
213	RESERVED					
214	RESERVED					
215	RESERVED					
216	RESERVED					
217	RESERVED					
218	RESERVED					
219	GND					
220	RESERVED					
221	RESERVED					
222	USB_VCONN					
223	USBC_CC2					
224	USBC_CC1					
225	GND					
226	USB_SS_SEL	1.8V	GPIO_139	I-PD	√	
227	LINEOUT_P					
228	LINEOUT_N					

229	GPIO_97	1.8V	GPIO_97	I-PD	√	
230	GPIO_96	1.8V	GPIO_96	I-PD		
231	GPIO_90	1.8V	GPIO_90	I-PD	√	
232	GPIO_89	1.8V	GPIO_89	I-PD		
233	TP_B					
234	GPIO_66	1.8V	GPIO_66	I-PD		
235	RESERVED					
236	CAM4_MCLK	1.8V	GPIO_128	I-PD		
237	GPIO_36	1.8V	GPIO_36	I-PD	√	
238	GPIO_33	1.8V	GPIO_33	I-PD		
239	RESERVED					
240	RESERVED					
241	GPIO_107	1.8V	GPIO_107	I-PD		
242	GPIO_105	1.8V	GPIO_105	I-PD		Cannot be pull up externally
243	GND					
244	RESERVED					
245	UART5_RTS	1.8V	GPIO_19	I-PD		
246	UART5_CTS	1.8V	GPIO_18	I-PD		
247	GPIO_1	1.8V	GPIO_1	I-PD	√	
248	GPIO_0	1.8V	GPIO_0	I-PD		
249	FP_SPI_MOSI	1.8V	GPIO_137	I-PD	√	
250	FP_SPI_CLK	1.8V	GPIO_135	I-PD		
251	FP_SPI_MISO	1.8V	GPIO_138	I-PD	√	
252	GPIO_42/ACCL_INT_N	1.8V	GPIO_42	I-PD	√	
253	GPIO_43/ALSP_INT_N	1.8V	GPIO_43	I-PD	√	
254	GPIO_44/MAG_INT_N	1.8V	GPIO_44	I-PD	√	
255	GPIO_45	1.8V	GPIO_45	I-PD	√	
256	USIM2_DET	1.8V	GPIO_58	I-PD	√	
257	GND					
258	GND					
259	GND					
260	GND					
261	GND					
262	GND					
263	GND					
265	GND					
264	GND					
266	GND					
267	GND					

268	GND		
269	GND		
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316	GND		
317	GND		
318	GND		
319	GND		
320	GND		
321	GND		
322	GND		
323	GND		
324	GND		
325	GND		
326	GND		
327	GND		

NOTE

1. NP = no-pull, PD = pull down, PU = pull up, KP = keeper
2. PM8953_XX means that it is a pin of PM8953

2.3 Pin Description

Table 4: I/O parameter definitions

Symbol	Description
Pad attribute	
PI	Power input
PO	Power input
AI	Analog input
AO	Analog output
DI	Digital input
DO	Digital output

OD	Open drain
Pad pull details for digital I/Os	
NP	No internal pull
PU	Internal pullup
PD	Internal pulldown

Table 5: Pin description

Pin Name	Pin No.	I/O	Description	Note
Power Supply				
VBAT	37，38	PI	Main power supply for the module	TVS is recommended for surge protection.
VDD_RF	1，2	PO	Main power supply for the RF. External filter capacitor shall be reserved.	TVS is recommended for surge protection. Cannot be used for other peripheral
VREG_L5_1P8	9	PO	LDO 5 output, should not be changed and turned off.	Power supply for external GPIO's pull up and level shift circuits. If unused, keep it open.
VREG_L6_1P8	10	PO	LDO 6 output , could be turned off in sleep mode	Power supply for external circuit. A parallel 2.2uF~4.7uf capacitance is required. If unused, keep it open.
VREG_L10_2P8	11	PO	LDO 10 output for Sensors and touchscreen	Power supply for external circuit. A parallel 2.2uF~4.7uf capacitance is required. If unused, keep it open.
VREG_L17_2P85	12	PO	LDO 17 output for display and camera VCM	Power supply for external circuit. A parallel 2.2uF~4.7uf capacitance is required. If unused, keep it open.
VREG_L2_1P1	13	PO	LDO 2 output for camera DVDD	Power supply for external circuit. A parallel 2.2uF~4.7uf capacitance is

				required. If unused, keep it open.
VREG_L22_2P8	14	PO	LDO 22 output for camera AVDD	Power supply for external circuit. A parallel 2.2uF~4.7uf capacitance is required. If unused, keep it open.
VREG_L23_1P2	15	PO	LDO 23 output for camera DVDD	Power supply for external circuit. A parallel 2.2uF~4.7uf capacitance is required. If unused, keep it open.
VRTC	16	PI/PO	Coin cell or backup-battery charger supply and input	If unused, keep it open.
GND	3，4，18，20，31，34，35，40，43，47，56，62，87，98，101，112，125，128，130，133，135，148，150，159，163，170，173，176，182，193，195，219，225，243，257~327	P	Ground	
USB TYPE-C				
USB_VBUS	41，42	PI/PO		USB insertion interrupt detection
USB_DN	33	AI/AO	USB high-speed data	Require differential impedance of 90ohm.
USB_DP	32	AI/AO		
USB_ID	30	AI	USB_ID interrupt detection	Default high-level
USB_VCONN	222	AI	Power input pin (5 V, 210 mA from VBUS) to drive active cables during the DFP mode.	
USB_SS_SEL	226	DO	USB Type-C switch control,	

			cannot be pull up externally	
USBC_CC2	223	AI/AO	USB Type-C connector configuration channel 1	
USBC_CC1	224	AI/AO	USB Type-C connector configuration channel 2	
USB_SS_RX_P	171	AI	USB super-speed receive – plus	
USB_SS_RX_M	172	AI	USB super-speed receive –minus	
USB_SS_TX_P	174	AO	USB super-speed transmit – plus	
USB_SS_TX_M	175	AO	USB super-speed transmit – minus	
UIM Interface				
USIM2_VDD	210	PO	LDO 15 output for UIM2	The 1.8V or 2.95v USIM card is automatically identified
USIM2_DATA	209	DI/DO	UIM2 data	Cannot be used as GPIO
USIM2_CLK	208	DO	UIM2 clock	
USIM2_RST	207	DO	UIM2 reset	
USIM2_DET	256	DI	UIM2 presence detection	1.8V power domain. External pull-up resistor is required. If unused, keep it open.
USIM1_DET	145	DI	UIM1 presence detection	1.8V power domain. External pull-up resistor is required. If unused, keep it open.
USIM1_RST	144	DO	UIM1 reset	Cannot be used as GPIO
USIM1_CLK	143	DO	UIM1 clock	
USIM1_DATA	142	DI/DO	UIM1 data	
USIM1_VDD	141	PO	LDO 14 output for UIM1	The 1.8V or 2.95v USIM card is automatically identified
SDIO/SD Interface				
SD_CLK	70	DO	Secure digital controller clock	
SD_CMD	69	DI/DO	Secure digital controller command	
SD_DATA0	68	DID/O	Secure digital controller data bit 0	

SD_DATA1	67	DI/DO	Secure digital controller data bit 1	
SD_DATA2	66	DI/DO	Secure digital controller data bit 2	
SD_DATA3	65	DI/DO	Secure digital controller data bit 3	
SD_DET_N	64	DI	Secure digital card detection	
SD_LDO11_2P95	63	PO	LDO 11 output for SD card	
SD_LDO12	179	PO	SD card pull-up power supply;1.8v/2.95v	SD card pull-up only
Touch Screen				
TP0_I2C_SDA	206	OD	Touch0 screen I2C data	1.8V power domain.
TP0_I2C_SCL	140	OD	Touch0 screen I2C clock	External pull-up resistors are required.
TP0_RST_N	138	DO	Touch0 screen reset	1.8V
TP0_INT_N	139	DI	Touch0 screen interrupt	1.8V
TP1_I2C_SDA	204	OD	Touch1 screen I2C data	1.8V power domain.
TP1_I2C_SCL	205	OD	Touch1 screen I2C clock	External pull-up resistors are required.
TP1_INT_N	137	DI	Touch1 screen interrupt	1.8V
TP1_RST_N	136	DO	Touch1screen reset	1.8V
LCD Interface				
PWM	152	DO	PWM control for external WLED driver	1.8V
LCD0_RST	127	DO	LCD0 reset	1.8V
LCD0_TE	126	DI	LCD0 tearing effect	1.8V
LCD1_RST	113	DO	LCD1 reset	1.8V
LCD1_TE	114	DI	LCD1 tearing effect	1.8V
MIPI_DSI0_CLK_P	115	AO		
MIPI_DSI0_CLK_N	116	AO		
MIPI_DSI0_LANE0_P	117	AI/AO		
MIPI_DSI0_LANE0_N	118	AI/AO		
MIPI_DSI0_LANE1_P	119	AI/AO	Primary display serial interface 0	
MIPI_DSI0_LANE1_N	120	AI/AO		
MIPI_DSI0_LANE2_P	121	AI/AO		
MIPI_DSI0_LANE2_N	122	AI/AO		
MIPI_DSI0_LANE3_P	123	AI/AO		
MIPI_DSI0_LANE3_N	124	AI/AO		
MIPI_DSI1_CLK_P	102	AO		
MIPI_DSI1_CLK_N	103	AO	Secondary display serial interface 1	
MIPI_DSI1_LANE0_P	104	AI/AO		
MIPI_DSI1_LANE0_N	105	AI/AO		

MIPI_DSI1_LANE1_P	106	AI/AO		
MIPI_DSI1_LANE1_N	107	AI/AO		
MIPI_DSI1_LANE2_P	108	AI/AO		
MIPI_DSI1_LANE2_N	109	AI/AO		
MIPI_DSI1_LANE3_P	110	AI/AO		
MIPI_DSI1_LANE3_N	111	AI/AO		
Camera Interface				
MIPI_CSI0_CLK_P	88	AI		
MIPI_CSI0_CLK_N	89	AI		
MIPI_CSI0_LANE0_P	90	AI/AO		
MIPI_CSI0_LANE0_N	91	AI/AO		
MIPI_CSI0_LANE1_P	92	AI/AO	Primary camera serial interface 0	
MIPI_CSI0_LANE1_N	93	AI/AO		
MIPI_CSI0_LANE2_P	94	AI/AO		
MIPI_CSI0_LANE2_N	95	AI/AO		
MIPI_CSI0_LANE3_P	96	AI/AO		
MIPI_CSI0_LANE3_N	97	AI/AO		
MIPI_CSI1_CLK_P	183	AI		
MIPI_CSI1_CLK_N	184	AI		
MIPI_CSI1_LANE0_P	185	AI/AO		
MIPI_CSI1_LANE0_N	186	AI/AO		
MIPI_CSI1_LANE1_P	187	AI/AO		
MIPI_CSI1_LANE1_N	188	AI/AO		
MIPI_CSI1_LANE2_P	189	AI/AO	Camera serial interface 1	Camera 4 MIPI lane0 – positive
MIPI_CSI1_LANE2_N	190	AI/AO		Camera 4 MIPI lane0 –negative
MIPI_CSI1_LANE3_P	191	AI/AO		Camera 4 MIPI clock – positive
MIPI_CSI1_LANE3_N	192	AI/AO		Camera 4 MIPI clock – negative
MIPI_CSI2_CLK_P	77	AI		
MIPI_CSI2_CLK_N	78	AI		
MIPI_CSI2_LANE0_P	79	AI/AO		
MIPI_CSI2_LANE0_N	80	AI/AO		
MIPI_CSI2_LANE1_P	81	AI/AO	Secondary camera serial interface 2	
MIPI_CSI2_LANE1_N	82	AI/AO		
MIPI_CSI2_LANE2_P	83	AI/AO		
MIPI_CSI2_LANE2_N	84	AI/AO		
MIPI_CSI2_LANE3_P	85	AI/AO		
MIPI_CSI2_LANE3_N	86	AI/AO		

MCAM_RST_N	74	DO	Primary Camera reset	1.8V
MCAM_PWD_N	73	DO	Primary Camera power down	1.8V
SCAM_RST_N	72	DO	Secondary Camera reset	1.8V
SCAM_PWD_N	71	DO	Secondary Camera power down, cannot be pull up externally	1.8V
CAM_I2C_SDA0	76	OD	DedicatedCamera I2C data	1.8V power domain.
CAM_I2C_SCL0	75	OD	Dedicated Camera I2C clock	External pull-up resistors are required.
SCAM_MCLK	100	DO	Secondary Camera master clock	1.8V
MCAM_MCLK	99	DO	Primary Camera master clock	1.8V
DCAM_MCLK	194	DO	Depth Camera master clock	1.8V
CAM4_MCLK	236	DO	Camera 4 master clock	1.8V
DCAM_RST_N	180	DO	Depth Camera reset	1.8V
DCAM_PWD_N	181	DO	Depth Camera power down	1.8V
DCAM_I2C_SDA	197	OD	Depth Camera I2C data	1.8V power domain.
DCAM_I2C_SCL	196	OD	Depth Camera I2C clock	External pull-up resistors are required.
Keypad				
KEY_VOL_UP_N	146	DI	Volume up keypad	If unused, keep it open.
KEY_VOL_DOWN_N	147	DI	Volume down keypad	If unused, keep it open.
PWRKEY	39	DI	Power on keypad	
Sensors				
SENSOR_I2C_SCL	131	OD	Sensors I2C clock	1.8V power domain.
SENSOR_I2C_SDA	132	OD	Sensors I2C data	External pull-up resistors are required.
GPIO_42/ ACCL_INT_N	252	DI	Accelerate sensor interrupt	
GPIO_43/ ALSP_INT_N	253	DI	Ambient light and proximity sensor interrupt	
GPIO_44/ MAG_INT_N	254	DI	Magnetic sensor interrupt	
GPIO_45	255	DI	Gyroscope sensor interrupt	
Audio				
SPK_P	55	AO	Speaker driver output, positive	
SPK_N	54	AO	Speaker driver output, negative	

EAR_P	53	AO	Earpiece output, positive	
EAR_N	52	AO	Earpiece output, negative	
HPH_L	49	AO	Headphone output, left channel	
HPH_REF	50	AI	Headphone ground reference	
HPH_R	51	AO	Headphone output, right channel	
HS_DET	48	AI	Headset detection	
MIC2_P	46	AI	Microphone input 2, positive	
MIC1_N	45	AI	Microphone input 1, negative	
MIC1_P	44	AI	Microphone input 1, positive	
MIC_GND	168		MIC ground	
MIC3_P	169	AI	Microphone input 3, positive	
MIC_BIAS	167	PO	Microphone bias1	Bias for external MEMS Microphone；ECM: keep MIC_BIAS open
LINEOUT_P	227	AO	LINEOUT output, positive	
LINEOUT_N	228	AO	LINEOUT output, negative	
Antenna				
MAIN_ANT	19	AI/AO	2G/3G/4G main antenna port	
DRX_ANT	149	AI	4G diversity antenna port	
GNSS_ANT	134	AI	GNSS antenna port	
WIFI/BT_ANT	129	AI/AO	WIFI/BT antenna port	
UART				
UART2_TX	5	DO	UART2 data transmit for debug	1.8V
UART2_RX	6	DI	UART2 data receive for debug	1.8V
UART4_TX	7	DO	UART4 data transmit	1.8V
UART4_RX	8	DI	UART4 data receive	1.8V
UART5_TX	199	DO	UART5 data transmit	1.8V
UART5_RX	198	DI	UART5 data receive	1.8V
UART5_RTS	245	DO	UART5 Ready-for-receive	1.8V
UART5_CTS	246	DI	UART5 Clear-to-send	1.8V
SPI				
SPI6_CS	58	DO	SPI6 chip select	
SPI6_CLK	59	DO	SPI6 clock	
SPI6_MOSI	60	DO	SPI6 master out slave in	
SPI6_MISO	61	DI	SPI6 master in slave out	

FP_SPI_CS	203	DO	SPI chip select	Reusable as I2S_WS
FP_SPI_CLK	250	DO	SPI clock	Reusable as I2S_SCK
FP_SPI_MOSI	249	DO	SPI master out slave in	Reusable as I2S_D0
FP_SPI_MISO	251	DI	SPI master in slave out	Reusable as I2S_D1
GPIO				
GPIO_0	248	DI/DO	GPIO	
GPIO_1	247	DI/DO	GPIO	
GPIO_2	201	DI/DO	GPIO	
GPIO_3	200	DI/DO	GPIO	
GPIO_33	238	DI/DO	GPIO	
GPIO_36	237	DI/DO	GPIO	
GPIO_66	234	DI/DO	GPIO	
GPIO_89	232	DI/DO	GPIO	
GPIO_90	231	DI/DO	GPIO	
GPIO_96	230	DI/DO	GPIO	
GPIO_97	229	DI/DO	GPIO	
GPIO_98	177	DI/DO	GPIO	
GPIO_99	178	DI/DO	GPIO	
GPIO_105	242	DI/DO	GPIO	Cannot be pull up externally
GPIO_107	241	DI/DO	GPIO	
Emergency Download Interface				
FORCED_USB_BOOT	57	DI	Force boot from USB interface	
ADC Interface				
ADC	151	AI	ADC	Maximum input voltage is 1.7V.
Others				
GNSS_LNA_EN	202	DO	GPS LNA enable control	Only for testing. Please keep open
TP_A	211		only used for module testing	TP_A and TP_B are directly connected inside the module
TP_B	233		only used for module testing	
NC				
NC	17，21~29，36，153~158，160~162，164~166，212~218，220，221，235，239，		Do not connect	

	240，244			

NOTE

1. Leave unused pins floating unless otherwise specified.

3 Interface Application

3.1 Power Supply

The power supply of SIM8960x ranges from 3.4V to 4.4V, and 3.9V is recommended. It must be able to provide sufficient current up to 3A for the high-power transmitting.

3.1.1 Recommended power supply resolutions

For battery-powered applications, the external charging IC is needed.

For non-battery applications, if the DC input voltage is +5V and users do not care about the power efficiency, a high-current low-dropout regulator is recommended. The reference design is shown in Figure 3.

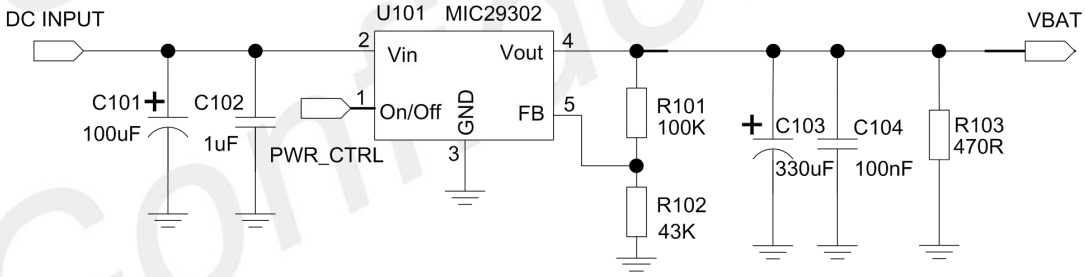

Figure 3: LDO power supply reference circuit

NOTE

1. To ensure a proper behavior of the regulator under light load, an extra minimum load (R103 in Figure 3) is required, because the current SIM8960x consumed is very small in sleep mode and power off mode. For more details about minimum load, please refer to specification of MIC29302.

To increase power efficiency, the switching mode DC-DC converter is preferable, especially when DC input

voltage is quite high. The reference design is shown in Figure 4, and it is recommended to reserve a proper ferrite bead (FB101 in Figure 4) in series for EMI suppression.

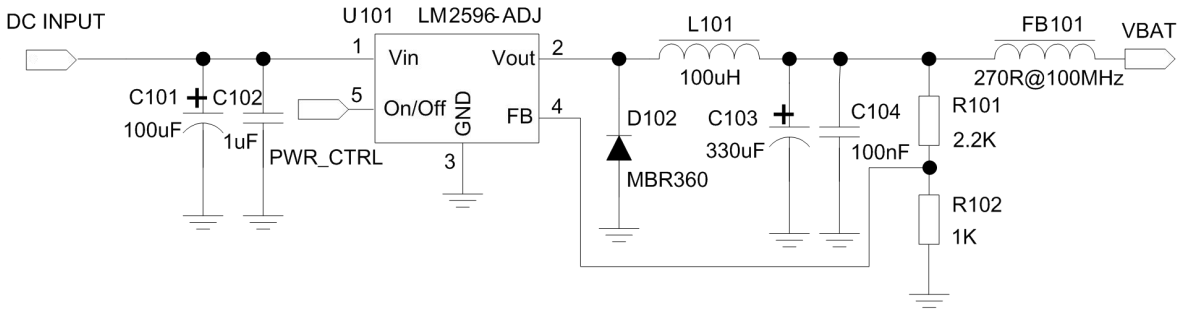

Figure 4: DC-DC power supply reference circuit

3.1.2 Enhance power stability

To enhance power stability, it is recommended to add some bypass capacitors and TVS closed to VBAT pins. The reference design is shown in Figure 5, where C101 and C102 are two110uF tantalum capacitors with low ESR, C103 could be a 1~10uF ceramic capacitor, 33pFand 10pF capacitors are used for eliminating the high frequency interference, 5V/1600W TVS can protect the module against voltage surge.

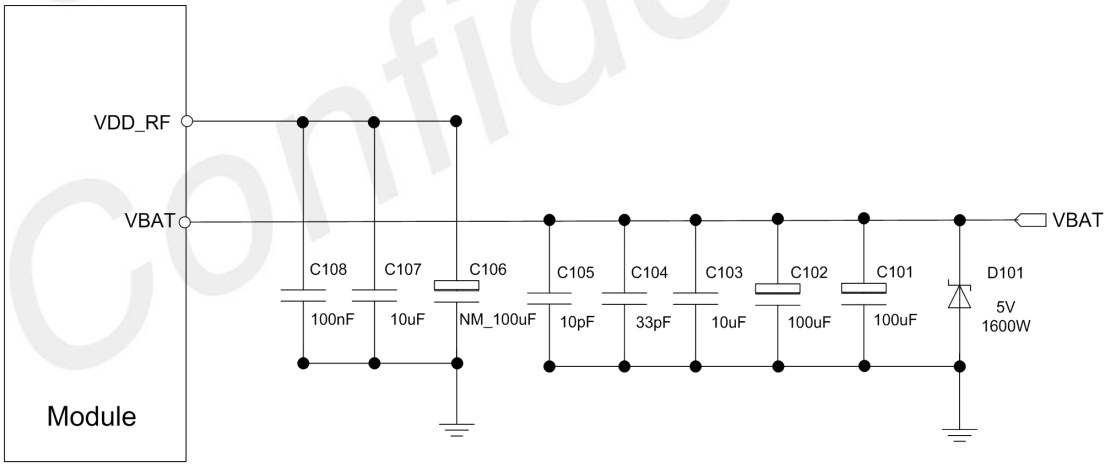

Figure 5: VBAT input reference circuit

Table 6: Recommended TVS diode

No.	Vendor	Part number	Power(watts)	Packages
1	Prisemi	PTVSHC3N4V8U	3200W	DFN2×2-3L
2	Prisemi	PTVSHC2EN5VU	1600W	DFN1610-2L

3.2 Power On/off

3.2.1 Power on

Users can power on SIM8960x by pulling down the PWRKEY pin for more than 2 second then release. This pin is already pulled up to 1.8V internally, so external pull up is not necessary. The electrical characteristics are listed in Table 7, and reference circuits are shown in the following figures:

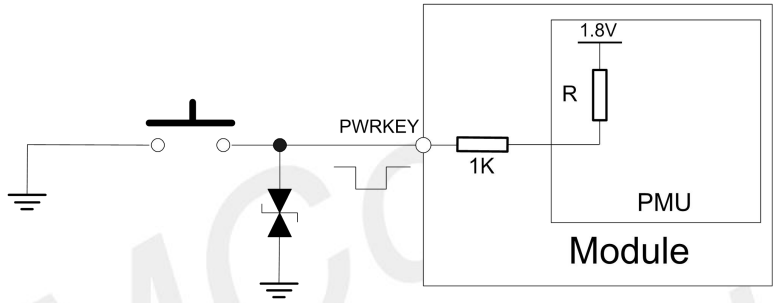

Figure 6: Powered on/off module using button

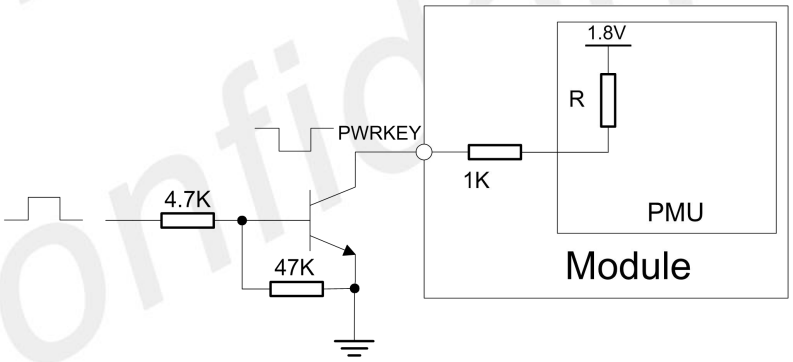

Figure 7: Powered on/off module using transistor

Table 7: PWRKEY characteristics

Parameters	Description	Min	Typ	Max	Unit
V_{IH}	High-level input voltage	1.4	-	-	V
V_{IL}	Low-level input voltage	-	-	0.6	V

3.2.2 Power-on sequence

The power-on sequence is shown in Figure 8.

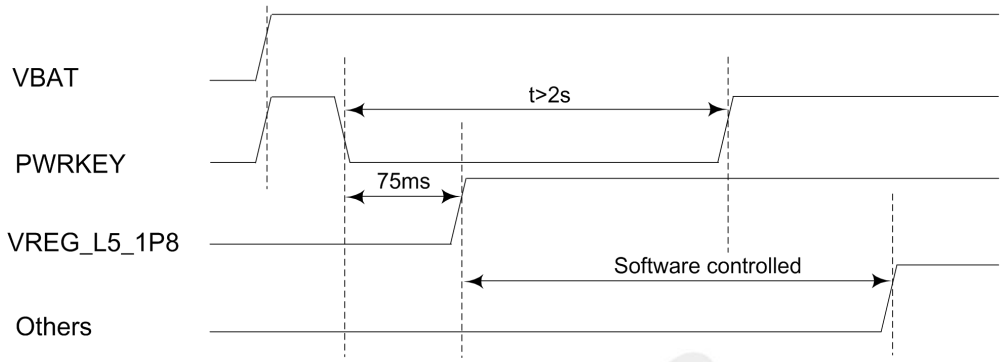

Figure 8: Power-on sequence

NOTE

1. Make sure that VBAT is stable before pulling down PWRKEY pin. The time between them is no less than 50ms.
2. PWRKEY pin cannot be pulled down all the time.

3.2.3 Power off

Users can turn off SIM8960x by pulling down the PWRKEY pin for more than 1 second. After the module detects that the PWRKEY is low level, a prompt window will pop up on the screen to confirm whether to execute the shutdown action.
Module can also be forced to shut down by pulling down PWRKEY for more than 8 seconds.

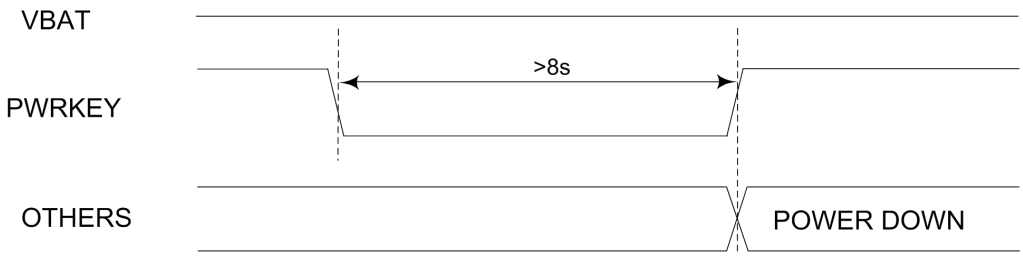

Figure 9: Power-off sequence

NOTE

1. The VBAT power supply circuit of the module can be cut off in the customer's hardware design.
2. It is recommended to add a low-cost MCU, which can control the PWRKEY to power on and power off the module, as well as the hardware watchdog to protect the normal operation.
3. Do not directly cut off the power supply VBAT of the module when the module is working normally, otherwise the internal flash of the module will be damaged. It is strongly recommended to shut down the module through PWRKEY or AT command before disconnecting the power supply VBAT of the module.

3.3 VRTC

VRTC is the power supply for RTC circuit and charger output for coin cell or backup battery. If RTC support is needed when the battery is removed, a qualified coin cell or keep-alive capacitor is required on the VRTC pin. When VBAT is present and valid, coin cell charging is enabled through software control and powered from VBAT.
Reference circuits are shown in the following figures:

Keep-alive capacitor:

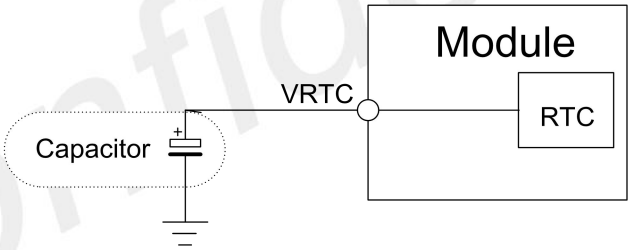

Figure 10: Keep-alive capacitor

Non-rechargeable battery:

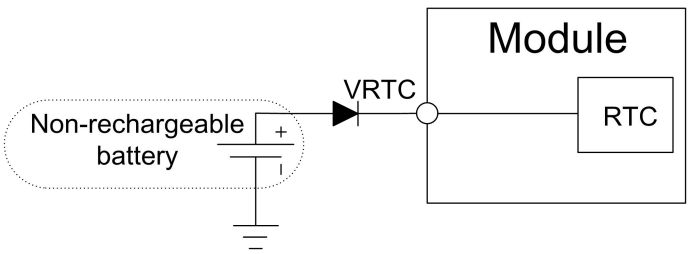

Figure 11: Non-rechargeable battery

Rechargeable battery:

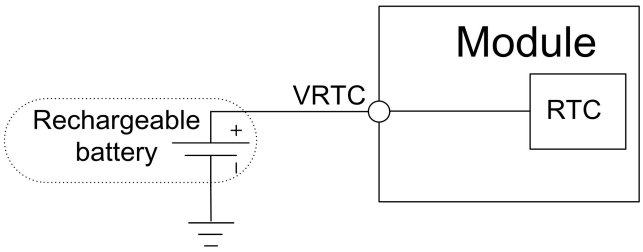

Figure 12: Rechargeable battery

VRTC typical voltage is 3.0V, and the current consumption is about 18uA when VBAT is absence. VRTC electrical characteristics are listed in the following table.

Table 8: VRTC characteristic

Parameter	Description	Min	Typ	Max	Unit
$VRTC_{-IN}$	VRTC input voltage	2.0	3.0	3.25	V
I_{RTC-IN}	VRTC current consumption	-	18	20	uA
$VRTC_{-OUT}$	VRTC output voltage	2.5	3.1	3.2	V
$I_{RTC-OUT}$	VRTC output current	-		2	mA

3.4 Output Power Management

Table 9: Output power management summary

Pin Name	Pin#	Specified	Pin Name	Pin#	Specified
VREG_L5_1P8	9	1.8	N/A	50	Force USB boot, level shifter
VREG_L6_1P8	10	1.8	N/A	300	Display, camera, sensors
VREG_L10_2P8	11	2.8	1.750–3.3375	150	Sensors and touch screen
VREG_L17_2P85	12	2.85	1.750–3.3375	300	display and camera VCM
VREG_L2_1P1	13	1.1	0.375–1.5375	1200	camera DVDD
VREG_L22_2P8	14	2.8	1.750–3.3375	150	camera AVDD
VREG_L23_1P2	15	1.2	0.375–1.5375	600	camera DVDD
SD_LDO11_2P95	63	1.8V/2.95V		800	SD/MMC card
SD_LDO12	179	1.8V/2.95V	N/A	50	SD card pull-up power supply;

USIM1_VDD	141	1.8V/2.95V	N/A	50	UIM1
USIM2_VDD	210	1.8V/2.95V	N/A	50	UIM2

3.5 USB Type-C Interface

SIM8960x module provides one USB 3.0/2.0 interface used for software upgrading, debugging, etc. Moreover, SIM8960x has integrated Type-C interface to provide multiple Type-C features, including mode configuration, channel configuration, current advertisement, and active cable support.

Table 10: USB interface Pin definition

PIN name	Pin#	I/O	Description	Note
USB_VBUS	41, 42	PI/PO	VBUS insertion detection	Vmin=4.35V Vnorm=5.0V Vmax=10V
USB_DP	32	AI/AO	USB high-speed data	Require differential impedance of 90ohm.
USB_DN	33	AI/AO		
USB_ID	30	AI	USB_ID interrupt detection	Default high-level
USB_VCONN	222	AI	Power input pin (5 V, 210 mA from VBUS) to drive active cables during the DFP mode.	Vmin=4.75V Vmax=5.25V
USB_SS_SEL	226	DO	USB Type-C switch control, cannot be pull up externally	
USBC_CC2	223	AI/AO	USB Type-C connector configuration channel 2	
USBC_CC1	224	AI/AO	USB Type-C connector configuration channel 1	
USB_SS_RX_P	171	AI	USB super-speed receive – plus	Require differential impedance of 90ohm.
USB_SS_RX_M	172	AI	USB super-speed receive –minus	
USB_SS_TX_P	174	AO	USB super-speed transmit – plus	Require differential impedance of 90ohm.
USB_SS_TX_M	175	AO	USB super-speed transmit – minus	

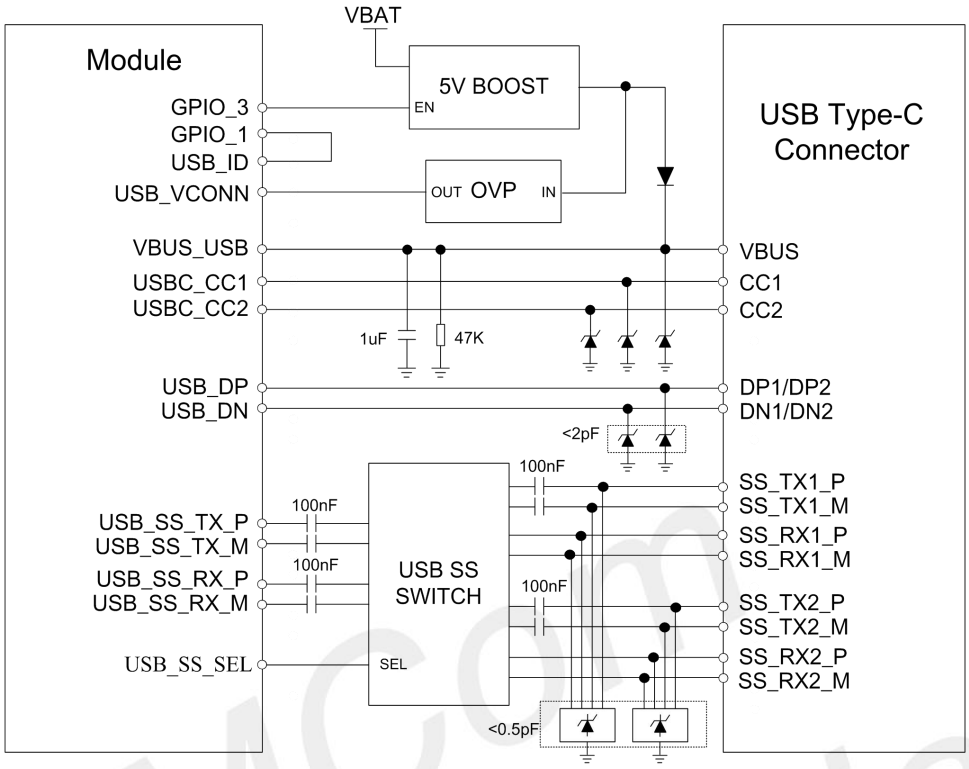

Figure 13: USB Type-C reference circuit

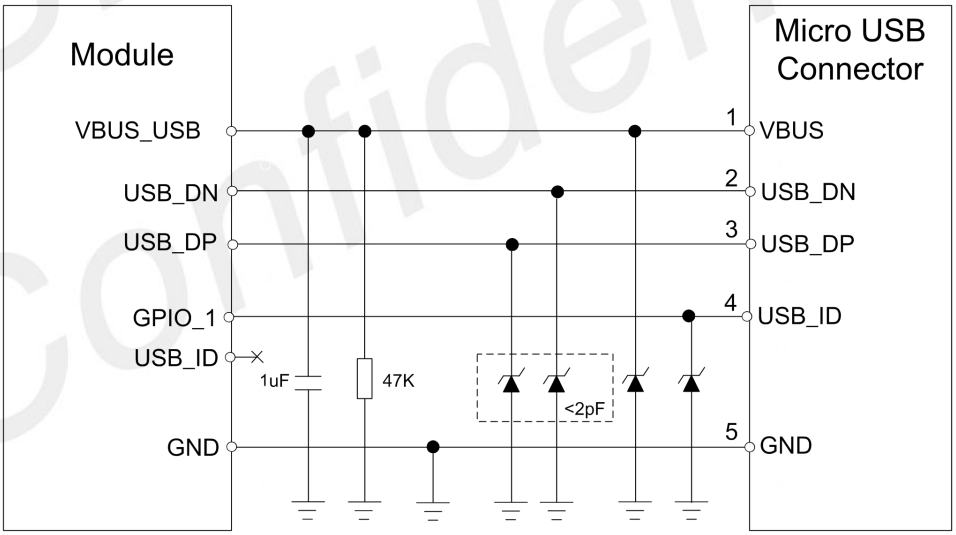

Figure 14: Micro USB reference circuit

In order to ensure the performance of USB, it is recommended to follow the following design principles:

- 90 Ω differential, ± 10% trace impedance
- Differential data pair matching <6.6 mm (50 ps)
- USB data traces layout requires GND protection. It need keep away from crystals, power,

magnetic devices, and RF-sensitive signals.

- Reserve ESD protection devices close to the USB interface. External components should be located near the USB connector.
- The parasitic capacitance requirements of USB 2.0 ESD protection devices are not more than 2pF;
- The parasitic capacitance requirements of the USB 3.0 ESD protection device do not exceed 0.5pF.
- USB 2.0 differential signal lines, USB 3.0 TX difference signals, and USB 3.0RX differential signal lines require equal length processing.
- If there are test points, place them on the trace to keep branches as short as possible

Table 11: Length of USB traces inside the module

Pin#	Net Name	Length (mm)	Difference(mm)
32	USB_DP	42.13	0.05
33	USB_DN	42.08	
171	USB_SS_RX_P	26.85	-0.02
172	USB_SS_RX_M	26.87	
174	USB_SS_TX_P	23.99	-0.15
175	USB_SS_TX_M	24.14	

3.6 UART/SPI/I2C

SIM8960x provides several sets of GPIOs which are available as BLSP (BAM-enabled low-speed peripheral) interfaces that can be configured to support various interface combinations, as shown in Table 12.

UART: Support 4*UART; up to 4 Mbps
SPI: Supports 7*SPI; master-only mode; up to 52 MHz
I2C: Support 10*I2C; master-only mode; up to 3.4 MHz, 2.2Kohm pull-up resistors are needed externally;

NOTE

1. CAM_I2C is a dedicated camera control interface, which cannot be used as general-purpose I2C ports.
2. I2C: 2.2Kohm pull-up resistors are needed externally.

Table 12: UART/SPI/I2Cfunctional assignments

Pin Name	Pin#	GPIO	Alternative Function 1	Alternative Function 2	Alternative Function 3
GPIO_0	248	GPIO_0		SPI1_MOSI	
GPIO_1	247	GPIO_1		SPI1_MISO	
GPIO_2	201	GPIO_2		SPI1_CS	I2C1_SDA
GPIO_3	200	GPIO_3		SPI1_CLK	I2C1_SCL
UART2_TX	5	GPIO_4	UART2_TX		
UART2_RX	6	GPIO_5	UART2_RX		
TP1_I2C_SDA	204	GPIO_6	UART2_CTS		I2C2_SDA
TP1_I2C_SCL	205	GPIO_7	UART2_RTS		I2C2_SCL
TP1_RST_N	136	GPIO_8		SPI3_MOSI	
TP1_INT_N	137	GPIO_9		SPI3_MISO	
TP0_I2C_SDA	206	GPIO_10		SPI3_CS	I2C3_SDA
TP0_I2C_SCL	140	GPIO_11		SPI3_CLK	I2C3_SCL
UART4_TX	7	GPIO_12	UART4_TX	SPI4_MOSI	
UART4_RX	8	GPIO_13	UART4_RX	SPI4_MISO	
SENSOR_I2C_SDA	132	GPIO_14	UART4_CTS	SPI4_CS	I2C4_SDA
SENSOR_I2C_SCL	131	GPIO_15	UART4_RTS	SPI4_CLK	I2C4_SCL
UART5_TX	199	GPIO_16	UART5_TX	SPI5_MOSI	
UART5_RX	198	GPIO_17	UART5_RX	SPI5_MISO	
UART5_CTS	246	GPIO_18	UART5_CTS	SPI5_CS	I2C5_SDA
UART5_RTS	245	GPIO_19	UART5_RTS	SPI5_CLK	I2C5_SCL
SPI6_MOSI	60	GPIO_20	UART6_TX	SPI6_MOSI	
SPI6_MISO	61	GPIO_21	UART6_RX	SPI6_MISO	
SPI6_CS	58	GPIO_22	UART6_CTS	SPI6_CS	I2C6_SDA
SPI6_CLK	59	GPIO_23	UART6_RTS	SPI6_CLK	I2C6_SCL
GPIO_96	230	GPIO_96		SPI8_MOSI	
GPIO_97	229	GPIO_97		SPI8_MISO	
GPIO_98	177	GPIO_98		SPI8_CS	I2C8_SDA
GPIO_99	177	GPIO_99		SPI8_CLK	I2C8_SCL
FP_SPI_CLK	250	GPIO_135	MI2S_2_SCK	SPI7_CLK	I2C7_SCL
FP_SPI_CS	203	GPIO_136	MI2S_2_WS	SPI7_CS	I2C7_SDA
FP_SPI_MOSI	249	GPIO_137	MI2S_2_D0	SPI7_MOSI	
FP_SPI_MISO	251	GPIO_138	MI2S_2_D1	SPI7_MISO	
CAM_I2C_SDA0	76	GPIO_29			CAM_I2C_SDA0
CAM_I2C_SCL0	75	GPIO_30			CAM_I2C_SCL0
DCAM_I2C_SDA	197	GPIO_31			DCAM_I2C_SDA

DCAM_I2C_SCL	196	GPIO_32			DCAM_I2C_SCL

3.7 Secure Digital Interface

SIM8960x provides one 4-bit secure digital interface, which supports SD 3.0 specifications.

Table 13: SD interface pin definitions

Pin Name	Pin#	I/O	Description	Note
SD_LDO11_2P95	63	PO	LDO 11 output for SD card	Vnorm=2.95V Maximum current: 800mA
SD_LDO12	179	PO	SD card pull-up power supply	Maximum current: 50mA
SD_CLK	70	DO	Secure digital controller clock	Require impedance of 50ohm.
SD_CMD	69	DI/DO	Secure digital controller command	
SD_DATA0	68	DID/O	Secure digital controller data bit 0	
SD_DATA1	67	DI/DO	Secure digital controller data bit 1	
SD_DATA2	66	DI/DO	Secure digital controller data bit 2	
SD_DATA3	65	DI/DO	Secure digital controller data bit 3	
SD_DET_N	64	DI	Secure digital card detection	

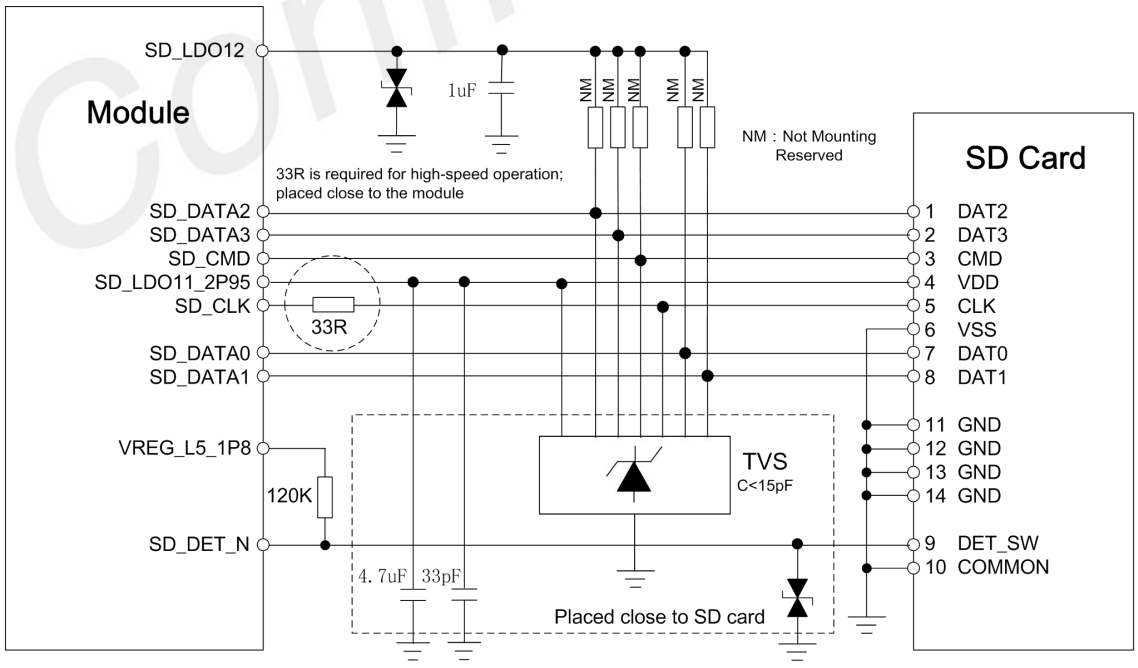

Figure 15: SD card reference circuit

NOTE

1. SDC signal cannot be pulled up to SD_LDO11_2P95.

In order to ensure the performance of SD, it is recommended to follow the following design principles:

- Protect other sensitive signals/circuits from SDC corruption.
- Protect SDC signals from noisy signals (clocks, SMPS, etc.).
- Up to 200 MHz clock rate
- 50 Ω nominal, ±10% trace impedance
- CLK to DATA/CMD length matching <1 mm
- 30–35 Ω termination resistor on clock lines near the module
- Total routing length <50 mm recommended
- Spacing to all other signals = 2x line width
- Bus capacitance < 15 pF

Table 14: Length of SD traces inside the module

Pin#	Net Name	Length (mm)
70	SD_CLK	25.30
69	SD_CMD	25.41
68	SD_DATA0	25.40
67	SD_DATA1	25.19
66	SD_DATA2	25.16
65	SD_DATA3	25.56

3.8 LCD Interface

SIM8960x provides two 4-lane MIPI_DSI, with 2.1 Gbps per lane high-speed mode bandwidth, to support dual LCDs with FHD (1920 × 1200 @ 60 fps) resolution.

NOTE

1. MIPI_DSI0 must be used for primary display.

Table 15: Display interface pin definitions

Pin Name	Pin#	I/O	Description
MIPI_DSI0_CLK_P	115	AO	Primary display serial interface 0
MIPI_DSI0_CLK_N	116	AO	
MIPI_DSI0_LANE0_P	117	AI/AO	
MIPI_DSI0_LANE0_N	118	AI/AO	
MIPI_DSI0_LANE1_P	119	AI/AO	
MIPI_DSI0_LANE1_N	120	AI/AO	
MIPI_DSI0_LANE2_P	121	AI/AO	
MIPI_DSI0_LANE2_N	122	AI/AO	
MIPI_DSI0_LANE3_P	123	AI/AO	
MIPI_DSI0_LANE3_N	124	AI/AO	
MIPI_DSI1_CLK_P	102	AO	Secondary display serial interface 1
MIPI_DSI1_CLK_N	103	AO	
MIPI_DSI1_LANE0_P	104	AI/AO	
MIPI_DSI1_LANE0_N	105	AI/AO	
MIPI_DSI1_LANE1_P	106	AI/AO	
MIPI_DSI1_LANE1_N	107	AI/AO	
MIPI_DSI1_LANE2_P	108	AI/AO	
MIPI_DSI1_LANE2_N	109	AI/AO	
MIPI_DSI1_LANE3_P	110	AI/AO	
MIPI_DSI1_LANE3_N	111	AI/AO	
VREG_L6_1P8	10	PO	LDO 6 output for LCM IO
VREG_L17_2P85	12	PO	LDO 17 output for display
PWM	152	DO	PWM control for external WLED driver
LCD0_RST	127	DO	LCD0 reset
LCD0_TE	126	DI	LCD0 tearing effect
LCD1_RST	113	DO	LCD1 reset
LCD1_TE	114	DI	LCD1 tearing effect

If only 2-lane MIPI_DSI is needed, just leave LANE2 and LANE3 floating.Common mode filters is recommended for EMI issue, and it may be omitted if best EMI practices are followed.

LCM0 can adopt external backlight drive also. The PWM pin of module is used to adjust backlight brightness. The reference circuit is shown as follows.

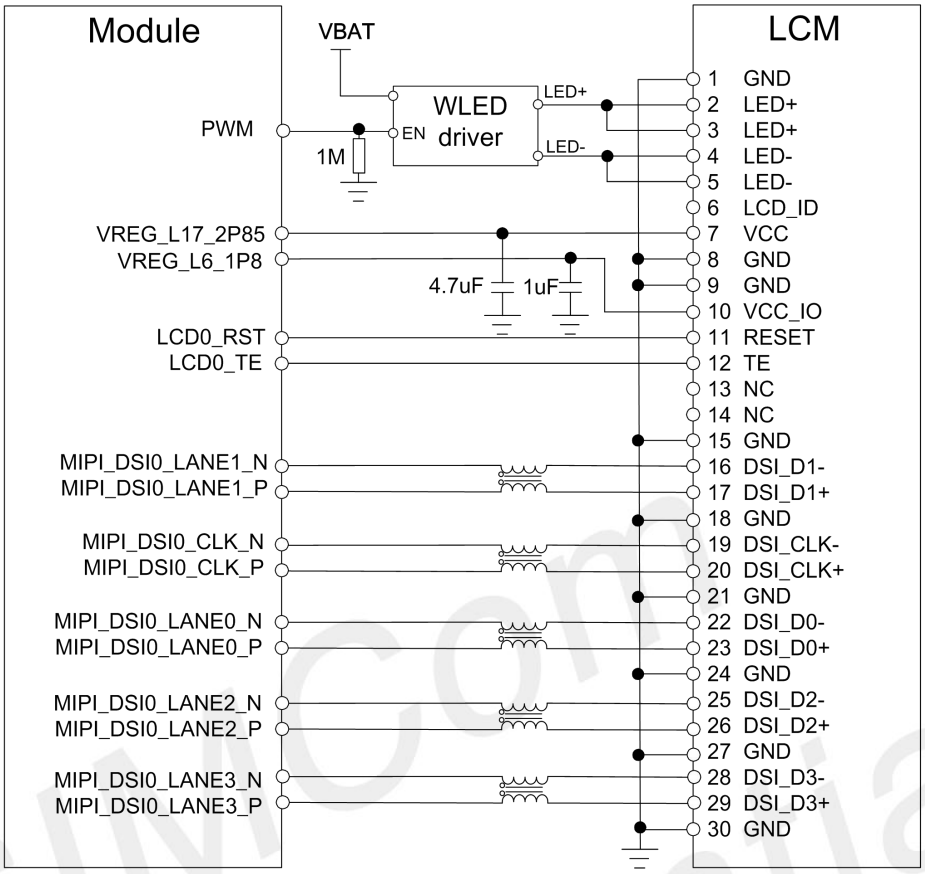

Figure 16: LCM0 Display reference circuit (external backlight drive)

LCM1 can adopt external backlight drive also. The reference circuit is shown as follows.

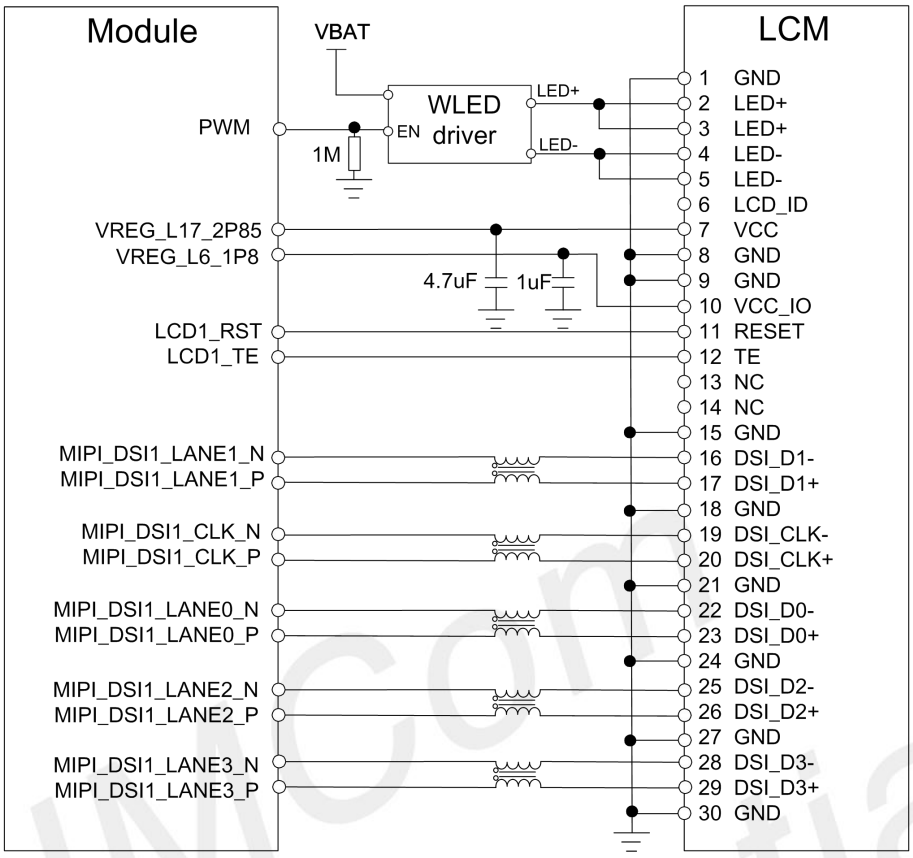

Figure 17: LCM1 Display reference circuit

In order to ensure the performance of MIPI_DSI, it is recommended to follow the following design principles:

- Protect MIPI_DSI signals from noisy signals (clocks, SMPS, etc.)
- Differential pairs, 100 Ω nominal, ±10%
- Total routing length <305 mm
- Intra-pair length matching < 5 ps (0.67 mm)
- Inter-pair length matching < 10 ps (1.3 mm)
- Lane-to-lane trace spacing = 3x line width
- Spacing to all other signals = 4x line width
- Maintain a solid ground reference for clocks to provide a low-impedance path for return currents
- Each trace needs to be next to a ground plane
- Minimize the number of via on the trace

Table 16: Length of MIPI_DSI traces inside the module

Pin#	Net Name	Length (mm)	Difference(mm)
115	MIPI_DSI0_CLK_P	21.26	-0.36
116	MIPI_DSI0_CLK_N	21.62	
117	MIPI_DSI0_LANE0_P	21.12	-0.26

118	MIPI_DSI0_LANE0_N	21.38	
119	MIPI_DSI0_LANE1_P	21.62	0.02
120	MIPI_DSI0_LANE1_N	21.60	
121	MIPI_DSI0_LANE2_P	23.75	0.14
122	MIPI_DSI0_LANE2_N	23.61	
123	MIPI_DSI0_LANE3_P	23.87	0.16
124	MIPI_DSI0_LANE3_N	23.71	
102	MIPI_DSI1_CLK_P	15.46	-0.08
103	MIPI_DSI1_CLK_N	15.54	
104	MIPI_DSI1_LANE0_P	15.44	-0.14
105	MIPI_DSI1_LANE0_N	15.58	
106	MIPI_DSI1_LANE1_P	15.56	0.13
107	MIPI_DSI1_LANE1_N	15.43	
108	MIPI_DSI1_LANE2_P	15.59	-0.11
109	MIPI_DSI1_LANE2_N	15.70	
110	MIPI_DSI1_LANE3_P	15.47	0.01
111	MIPI_DSI1_LANE3_N	15.46	

3.9 Touch Screen Interface

The module provides two I2C interfaces for connecting the touch screen, as well as the interrupt and reset pins of the touch panel. The interface pins are defined as follows:

Table 17: Touch screen interface pin definitions

Pin Name	Pin#	I/O	Description	Note
TP0_I2C_SDA	206	OD	Touch screen I2C data	
TP0_I2C_SCL	140	OD	Touch screen I2C clock	
TP0_RST_N	138	DO	Touch screen reset	
TP0_INT_N	139	DI	Touch screen interrupt	
TP1_I2C_SDA	204	OD	Touch screen I2C data	
TP1_I2C_SCL	205	OD	Touch screen I2C clock	
TP1_INT_N	137	DI	Touch screen interrupt	
TP1_RST_N	136	DO	Touch screen reset	
VREG_L6_1P8	10	PO	LDO 6 output for Touch screen	Maximum current: 300mA
VREG_L10_2P8	11	PO	LDO 10 output for Touch screen	Maximum current: 150mA

NOTE

1. I2C requires external pull-up to 1.8V, pull-up resistor 2.2Kohm

3.10 Camera Interface

The SIM8960x module video input interface is based on the MIPI_CSI standard.

■Three 4-lane CSI (4 + 4 + 4 or 4 + 4 + 2 + 1), 2.1 Gbps per lane.
■Three 4-lane CSI interfaces support three (4-lane+4-lane+4-lane) or four (4-lane+4-lane+2-lane+1-lane) cameras.
■ Support dual ISP (image signal processing), up to 21M pixels (dual ISP).
■Hardware support for up to four MCLKs, two CCI I2C for camera control.

Table 18: Camera interface pin definitions

Pin Name	Pin#	I/O	Description	Note
VREG_L2_1P1	13	PO	LDO 2 output for camera DVDD	The maximum output current is 1200mA
VREG_L6_1P8	10	PO	LDO 6 output for camera IO VDD	The maximum output current is 300mA
VREG_L17_2P85	12	PO	LDO 17 output for camera VCM	The maximum output current is 300mA
VREG_L22_2P8	14	PO	LDO 22 output for camera AVDD	The maximum output current is 150mA
VREG_L23_1P2	15	PO	LDO 23 output for camera DVDD	The maximum output current is 600mA
MIPI_CSI0_CLK_P	88	AI	Primary camera serial interface 0	
MIPI_CSI0_CLK_N	89	AI		
MIPI_CSI0_LANE0_P	90	AI/AO		
MIPI_CSI0_LANE0_N	91	AI/AO		
MIPI_CSI0_LANE1_P	92	AI/AO		
MIPI_CSI0_LANE1_N	93	AI/AO		
MIPI_CSI0_LANE2_P	94	AI/AO		
MIPI_CSI0_LANE2_N	95	AI/AO		
MIPI_CSI0_LANE3_P	96	AI/AO		
MIPI_CSI0_LANE3_N	97	AI/AO		

MIPI_CSI1_CLK_P	183	AI	Camera serial interface 1	Camera 4 MIPI lane0 – positive
MIPI_CSI1_CLK_N	184	AI		
MIPI_CSI1_LANE0_P	185	AI/AO		
MIPI_CSI1_LANE0_N	186	AI/AO		
MIPI_CSI1_LANE1_P	187	AI/AO		
MIPI_CSI1_LANE1_N	188	AI/AO		
MIPI_CSI1_LANE2_P	189	AI/AO		Camera 4 MIPI lane0 –negative
MIPI_CSI1_LANE2_N	190	AI/AO		Camera 4 MIPI clock – positive
MIPI_CSI1_LANE3_P	191	AI/AO		Camera 4 MIPI clock – negative
MIPI_CSI1_LANE3_N	192	AI/AO		
MIPI_CSI2_CLK_P	77	AI	Secondary camera serial interface 2	
MIPI_CSI2_CLK_N	78	AI		
MIPI_CSI2_LANE0_P	79	AI/AO		
MIPI_CSI2_LANE0_N	80	AI/AO		
MIPI_CSI2_LANE1_P	81	AI/AO		
MIPI_CSI2_LANE1_N	82	AI/AO		
MIPI_CSI2_LANE2_P	83	AI/AO		
MIPI_CSI2_LANE2_N	84	AI/AO		
MIPI_CSI2_LANE3_P	85	AI/AO		
MIPI_CSI2_LANE3_N	86	AI/AO		
MCAM_RST_N	74	DO	Primary Camera reset	1.8V
MCAM_PWD_N	73	DO	Primary Camera power down	1.8V
SCAM_RST_N	72	DO	Secondary Camera reset	1.8V
SCAM_PWD_N	71	DO	Secondary Camera power down, cannot be pull up externally	1.8V
CAM_I2C_SDA0	76	OD	Dedicated Camera I2C data	1.8V
CAM_I2C_SCL0	75	OD	Dedicated Camera I2C clock	1.8V
SCAM_MCLK	100	DO	Secondary Camera master clock	1.8V
MCAM_MCLK	99	DO	Primary Camera master clock	1.8V
DCAM_MCLK	194	DO	Depth Camera master clock	1.8V
CAM4_MCLK	236	DO	Camera 4 master clock	1.8V
DCAM_RST_N	180	DO	Depth Camera reset	1.8V
DCAM_PWD_N	181	DO	Depth Camera power down	1.8V
DCAM_I2C_SDA	197	OD	Depth Camera I2C data	1.8V
DCAM_I2C_SCL	196	OD	Depth Camera I2C clock	1.8V

The reference circuit is shown in the following figures.

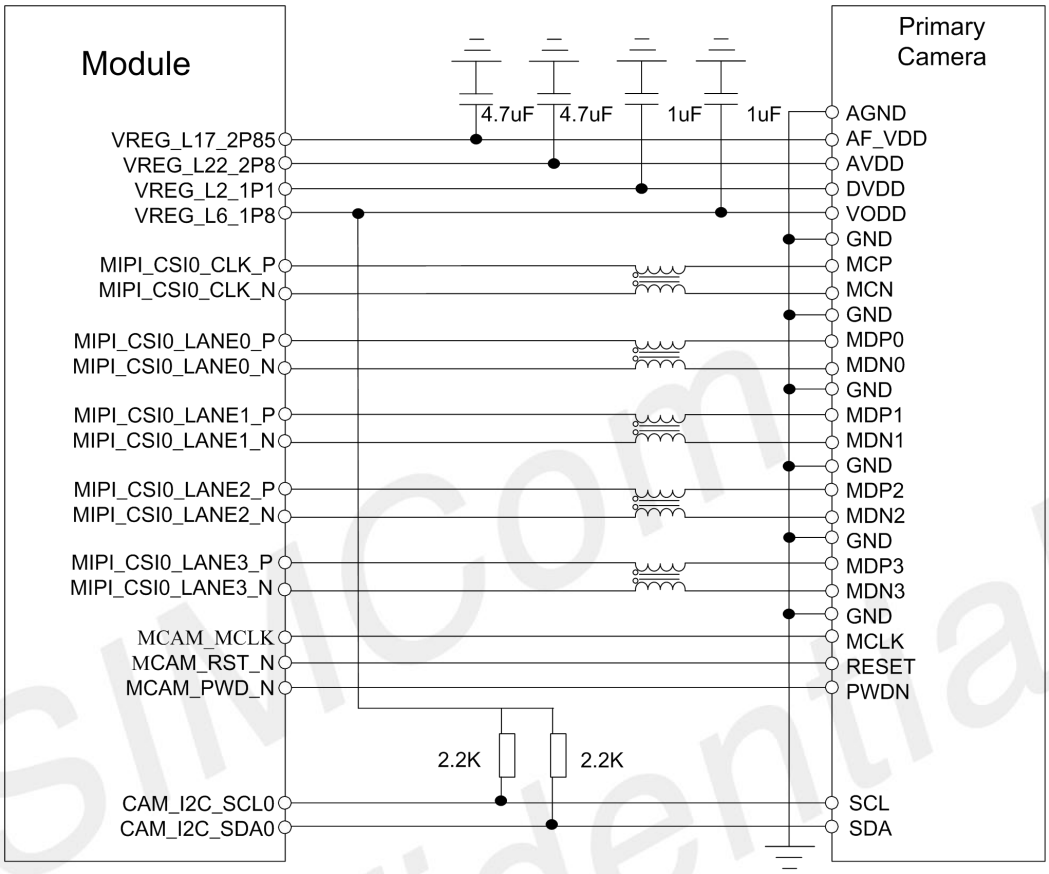

Figure 18: Primary camera reference circuit

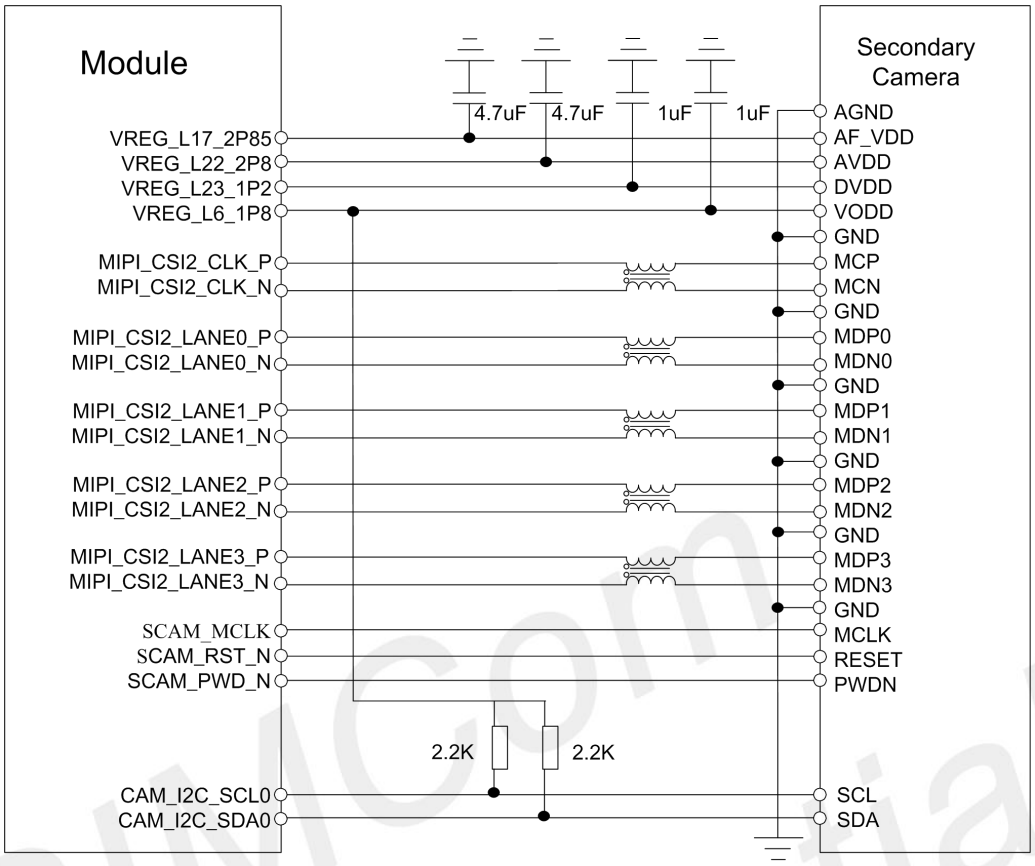

Figure 19: Secondary camera reference circuit

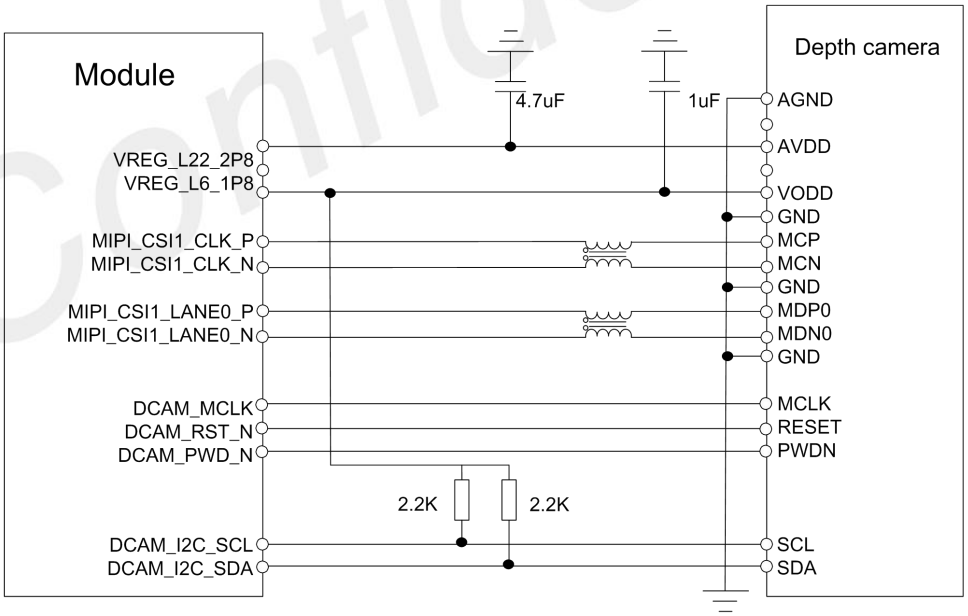

Figure 20: Depth camera reference circuit

NOTE

1. CSI0 is used for the rear camera, CSI1 for the depth camera and CSI2 for the front camera.
2. MIPI_CSI1_LANE2_P、MIPI_CSI1_LANE2_N、MIPI_CSI1_LANE3_P and MIPI_CSI1_LANE3_N can be reused as MIPI signal lines of camera 4.
3. I2C requires external pull-up to 1.8V, pull-up resistor 2.2Kohm

In order to ensure the performance of MIPI_CSI, it is recommended to follow the following design principles:

- Protect MIPI_DSI signals from noisy signals (clocks, SMPS, etc.)
- Differential pairs, 100 Ω nominal, ±10%
- Total routing length <305 mm
- Intra-pair length matching < 5 ps (0.67 mm)
- Inter-pair length matching < 10 ps (1.3 mm)
- Lane-to-lane trace spacing = 3x line width
- Spacing to all other signals = 4x line width
- Maintain a solid ground reference for clocks to provide a low-impedance path for return currents
- Each trace needs to be next to a ground plane
- Minimize the number of via on the trace

Table 19: Length of MIPI_CSI traces inside the module

Pin#	Net Name	Length (mm)	Difference(mm)
88	MIPI_CSI0_CLK_P	16.10	0.17
89	MIPI_CSI0_CLK_N	15.93	
90	MIPI_CSI0_LANE0_P	15.83	0.31
91	MIPI_CSI0_LANE0_N	15.52	
92	MIPI_CSI0_LANE1_P	15.50	-0.22
93	MIPI_CSI0_LANE1_N	15.72	
94	MIPI_CSI0_LANE2_P	15.52	-0.04
95	MIPI_CSI0_LANE2_N	15.56	
96	MIPI_CSI0_LANE3_P	15.54	0.27
97	MIPI_CSI0_LANE3_N	15.27	
183	MIPI_CSI1_CLK_P	15.23	-0.03
184	MIPI_CSI1_CLK_N	15.26	
185	MIPI_CSI1_LANE0_P	11.88	0.37
186	MIPI_CSI1_LANE0_N	11.51	
187	MIPI_CSI1_LANE1_P	6.29	-0.32

188	MIPI_CSI1_LANE1_N	6.61	
189	MIPI_CSI1_LANE2_P	4.89	0.33
190	MIPI_CSI1_LANE2_N	4.56	
191	MIPI_CSI1_LANE3_P	7.69	-0.03
192	MIPI_CSI1_LANE3_N	7.72	
77	MIPI_CSI2_CLK_P	23.24	0.46
78	MIPI_CSI2_CLK_N	22.78	
79	MIPI_CSI2_LANE0_P	22.72	0.12
80	MIPI_CSI2_LANE0_N	22.60	
81	MIPI_CSI2_LANE1_P	22.67	0.09
82	MIPI_CSI2_LANE1_N	22.58	
83	MIPI_CSI2_LANE2_P	22.43	-0.17
84	MIPI_CSI2_LANE2_N	22.60	
85	MIPI_CSI2_LANE3_P	22.53	-0.17
86	MIPI_CSI2_LANE3_N	22.70	

3.11 Audio

SIM8960x provides three microphone inputs and four outputs including earpiece, stereo headphones, mono class-D speaker driver and LINEOUT.

Table 20: Audio interface pin definitions

Pin Name	Pin#	I/O	Description
SPK_P	55	AO	Speaker driver output, positive
SPK_N	54	AO	Speaker driver output, negative
EAR_P	53	AO	Earpiece output, positive
EAR_N	52	AO	Earpiece output, negative
HPH_L	49	AO	Headphone output, left channel
HPH_REF	50	AI	Headphone ground reference
HPH_R	51	AO	Headphone output, right channel
HS_DET	48	AI	Headset detection
MIC2_P	46	AI	Microphone input 2, positive
MIC1_N	45	AI	Microphone input 1, negative
MIC1_P	44	AI	Microphone input 1, positive
MIC_GND	168		MIC ground.
MIC3_P	169	AI	Microphone input 3, positive
MIC_BIAS	167	PO	Microphone bias

LINEOUT_P	227	AO	LINEOUT output, positive
LINEOUT_N	228	AO	LINEOUT output, negative

3.11.1 Microphone

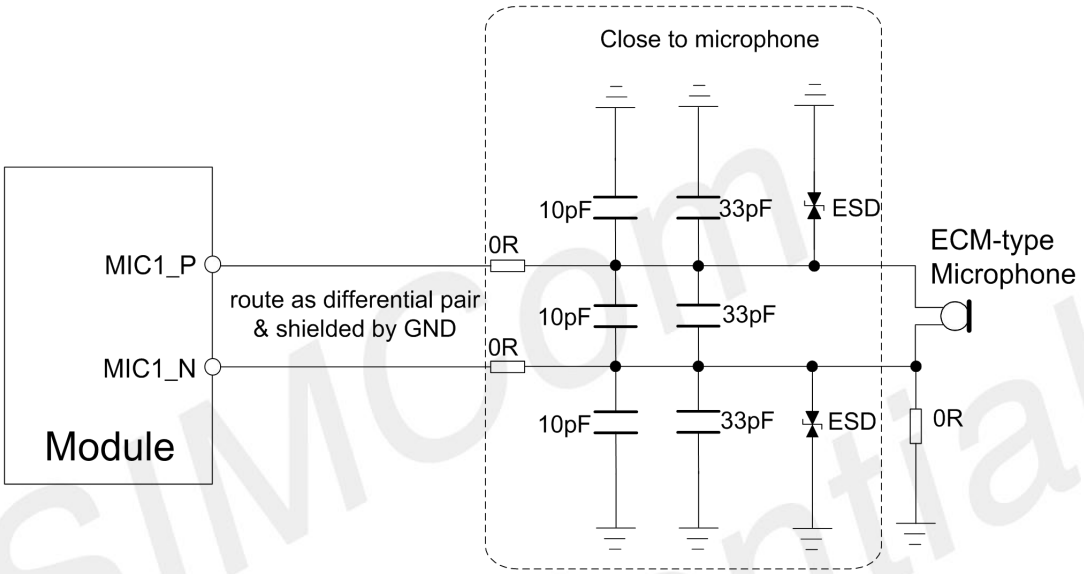

Figure 21: ECM-type microphonereference circuit

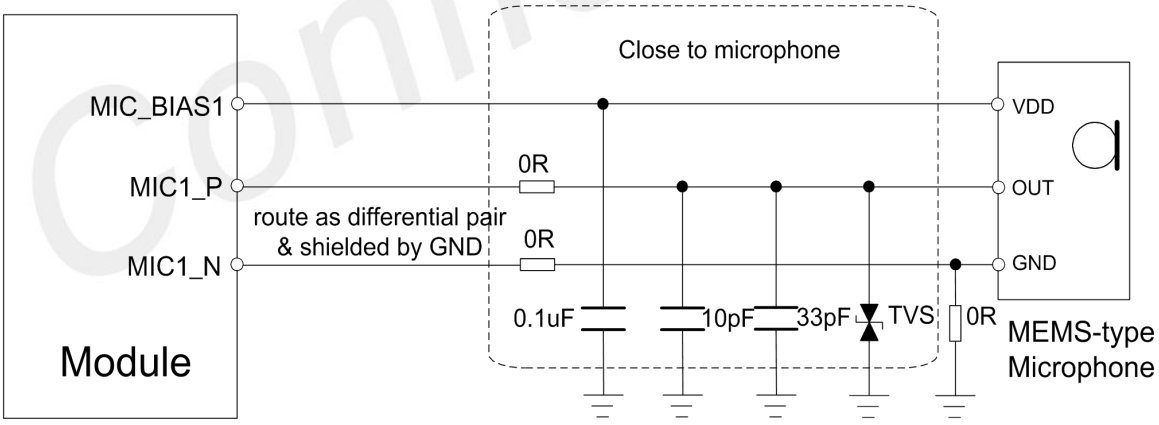

Figure 22: MEMS-type microphone reference circuit

3.11.2 Headset

Stereo class-AB headphone supports 16 Ω, 32 Ω, and up to 50 KΩ loads. Its typical output power at 1.02

KHz and THD + N ≤ 1% is:

- 62 mW with 16 Ω loads, 0 dBFS and 0 dB gain
- 30 mW with 32 Ω loads, 0 dBFS and 0 dB gain

A 100KΩ pull-down resistor is integrated at HPH_L pin, which could be used for mechanical insertion or removal detection through HS_DET pin. Figure 23 shows the reference circuit for normally-closed (NC) type headset jack.

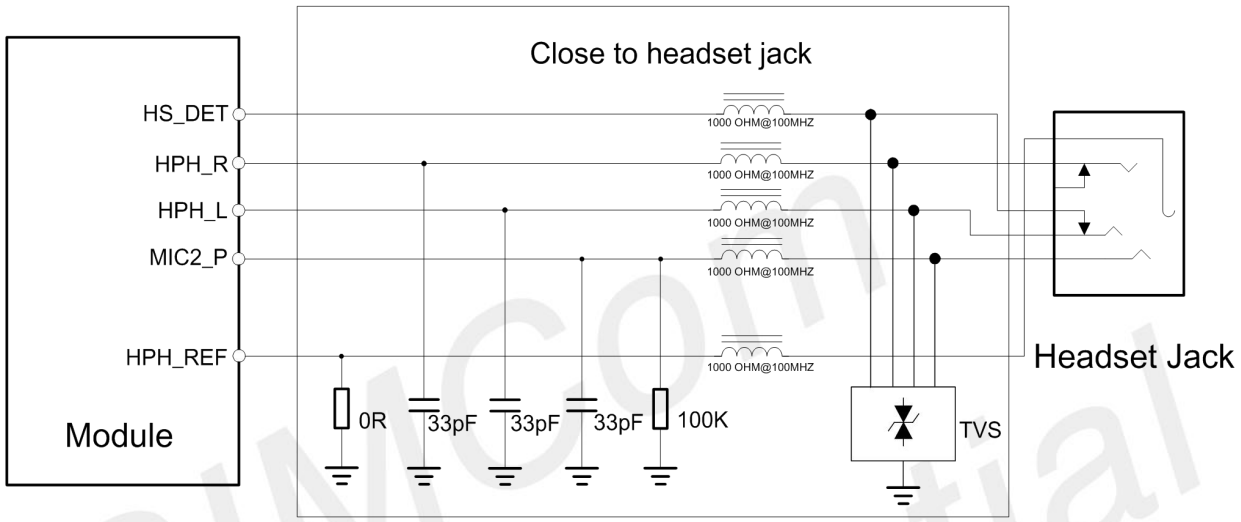

Figure 23: Headset reference circuit

Table 21: Headphone output performance specifications

Parameter	Test conditions	Min	Typ	Max	Units
Output power	16 Ω load f = 1.02 kHz, 0 dB FS;	54	62	-	mW
	32 Ω load f = 1.02 kHz, 0 dB FS;	-	30	-	mW
Full-scale output Voltage	16 Ω load f = 1.02 kHz, 0 dB FS;	0.9	1.0		Vrms
	32 Ω load f = 1.02 kHz, 0 dB FS;	0.9	1.0	-	Vrms
Output load		13.0	16/32	-	Ω
Disabled output impedance	Measured externally, with amplifier disabled	1.0	-	-	MΩ

NOTE

1. SIM8960x also supports NO/NC type headset jack with detect pin on HPH_L or GND.
2. HPH has a negative swing and requires a bi-directional TVS diode.

3.11.3 Earpiece

Class AB earpiece driver supports 10.67 Ω, 16 Ω, 32 Ω, and up to 50 KΩ loads. The typical output power at 1.02 KHz,6 dB gain, and THD + N ≤ 1% is:

- 126 mW with 32 Ω loads and 0 dBFS input
- 243 mW with 16 Ω loads and -1.5 dBFS input
- 320 mW with 10.67 Ω loads and -3.5 dBFS input

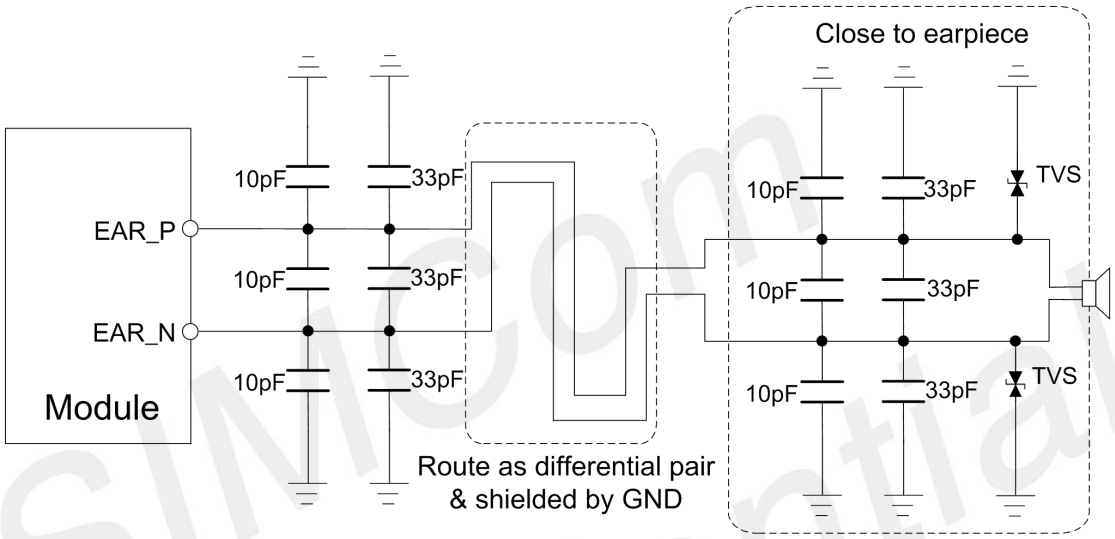

Figure 24: Earpiece reference circuit

Table 22: Earpiece output performance specifications

Parameter	Test conditions	Min	Typ	Max	Units
Output power	32 Ω load f = 1.02 kHz, 6 dB gain THD+N < 1%	115.0	126.0	-	mW
	16 Ω load f = 1.02 kHz, 6 dB gain THD+N < 1%	235.0	243.0	-	mW
Full-scale output Voltage	6 dB gain mode f = 1.02 kHz	1.94	1.98	-	Vrms
	1.5 dB gain mode f = 1.02 kHz	1.14	1.16	-	Vrms
Output load		10	32	-	Ω
Disabled output impedance		1.0	-	-	MΩ

3.11.4 Speaker

Class-D mono differential loud speaker driver supports 4 Ω and 8 Ω loads. The driver is powered from internal 5 V Boost (VDD_SPKR). Its typical output power at 1.02 KHz,12 dB gain, and THD + N ≤ 1% is:

- 1500 mW with 4 Ω loads and VDD_SPKR= 5V
- 2000 mW with 8 Ω loads and VDD_SPKR= 5.5V

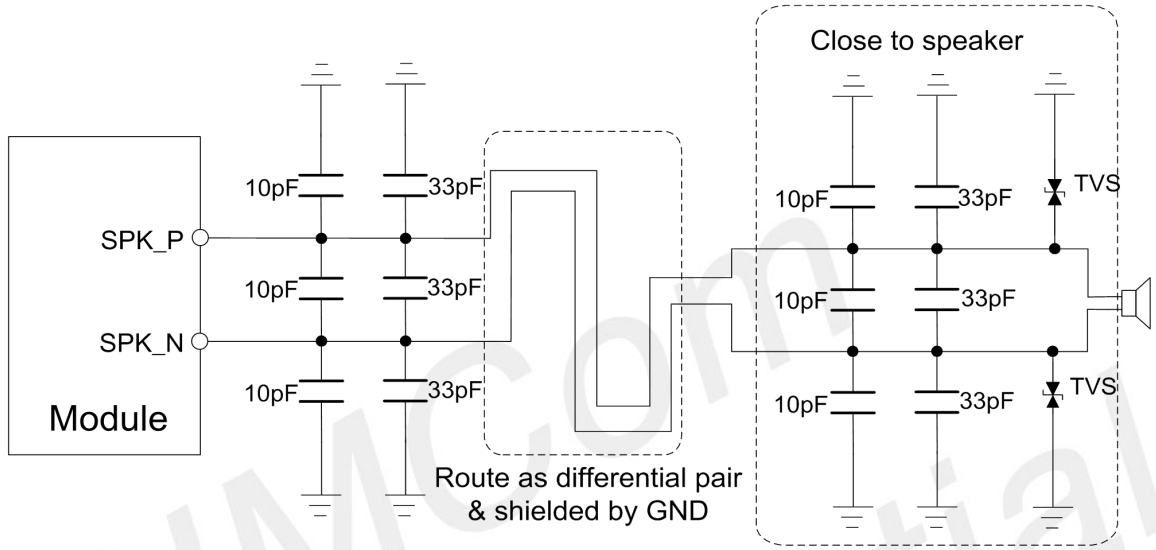

Figure 25: Speaker reference circuit

Table 23: speaker driver output performance specifications

Parameter	Test conditions	Min	Typ	Max	Units
Output power (Pout) (f = 1 kHz, THD+N≤ 1%)	15 μH + 4Ω + 15 μH, Vdd = 5V	1200	1500	-	mW
	15 μH + 8 Ω + 15 μH, Vdd = 5.5 V	1500	2000	-	mW
THD+N (1 kHz)	1.5 W Pout, VDD_SPKR = 5.5 V	-	-85.0	-	dB
	1.2 W Pout, VDD_SPKR = 5 V	-	-86.0	-	dB
Efficiency （Vdd = 3.7 V）	1 W Pout, 15 μH + 8 Ω + 15 μH	73.0	81.0	-	%
	1 W Pout, 15 μH + 4 Ω + 15 μH	60.0	72.0	-	%
output impedance		25	-	-	kΩ
Shutdown		-	2	16.0	μA
Turn on time		-	0.2	10.0	ms

NOTE

1. The maximum breakdown voltage of TVS for SPKR should not be less than 6 V.

3.11.5 LINEOUT

LINEOUT is a differential class-AB output to drive external speaker amplifier for loudspeaker.

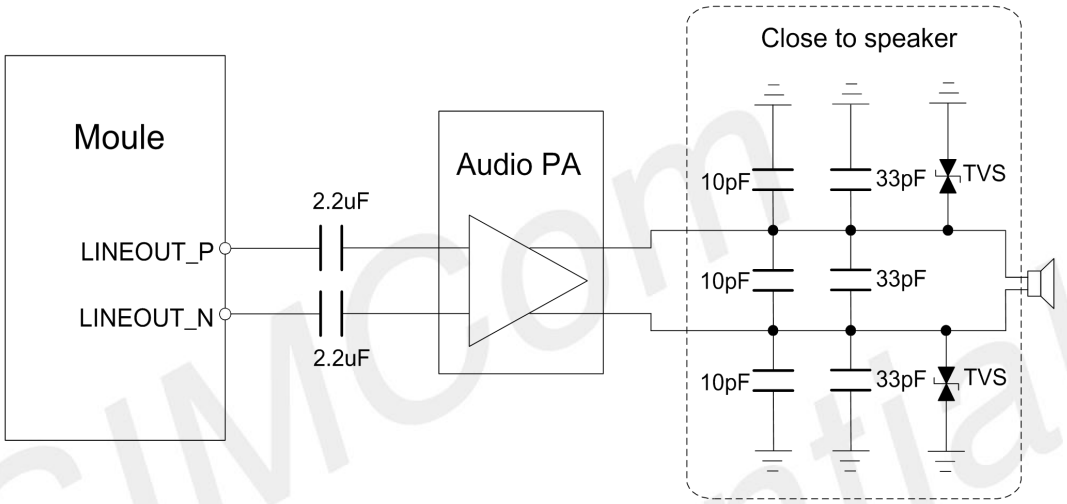

Figure 26: LINEOUT reference circuit

Table 24: LINEOUT output performance specifications

Parameter	Test conditions	Min	Typ	Max	Units
Maximum output voltage	f = 1.02 kHz, 0 dBFS	0.9	1.0	-	Vrms
Output common mode voltage	6 dB gain mode f = 1.02 kHz	1.52	1.6	1.68	Vrms
Output load		1	10	-	KΩ
Disabled output impedance		37.5	-	-	KΩ

3.11.6 Microphone bias

SIM8960x provides one microphone bias outputs: MIC_BIAS. The microphone bias cannot be used for ECM-type microphone. MIC_BIAS could be used for External MEMS microphone as power supply.
The microphone bias output performance specifications are shown in the following table:

Table 25: Microphone bias output performance specifications

Parameter	Test conditions	Min	Typ	Max	Units
Output voltage	No load	1.60	-	2.85	V
Output voltage error	No load	-3.00	0.00	3.00	%
Output current	2 microphone loads of 1.0 to 1.5 mA each	2.0	3.0	-	mA
Output switch to ground	On resistance	-	-	20	Ω
	Sink current	2.0	-	-	mA
Output noise	0.1 μF bypass	0.0	2.0	4.0	μVrms
PSRR-Power supply rejection ratio	at 20 Hz	80	-	-	dB
	at 200 Hz to 1 kHz	80	-	-	dB
	at 5 kHz	80	-	-	dB
	at 10 kHz	80	-	-	dB
	at 20 kHz	75	-	-	dB
Output capacitor value [2]	External bypass mode [1]	0.1	0.1	0.5	μF

3.12 I2S Interface

SIM8960x supports one I2S port, the pin definitions are shown in the following table:

Table 26: I2S interface pin definitions

Pin Name	Pin#	Alternative Function (I2S)	I/O	Description
LCD1_TE	114	I2S_MCLK_A	DI	I2S main clock A
GPIO_66	234	I2S_MCLK_B	DO	I2S main clock B
FP_SPI_CS	203	I2S_WS	DI/DO	I2S bit clock
FP_SPI_CLK	250	I2S_SCK	DI/DO	I2S word select
FP_SPI_MOSI	249	I2S_D0	DI/DO	I2S data0
FP_SPI_MISO	251	I2S_D1	DI/DO	I2S data1

3.13 UIM Interface

SIM8960x supports dual cards dual standby, and card presence detection.

NOTE

1. The standard software provided by SIMCom only supports single UIM card configuration.

Table 27: UIM interface pin definitions

Pin Name	Pin#	I/O	Description	Note
USIM2_VDD	210	PO	LDO 15 output for UIM2, 1.8V/2.95V	
USIM2_DATA	209	DI/DO	UIM2 data	Pull up USIM2_DATA to USIM2_VDD by the external 10K resistor
USIM2_CLK	208	DO	UIM2 clock	
USIM2_RST	207	DO	UIM2 reset	
USIM2_DET	256	DI	UIM2 presence detection	1.8V power domain. External pull-up resistor is required. If unused, keep it open.
USIM1_DET	145	DI	UIM1 presence detection	1.8V power domain. External pull-up resistor is required. If unused, keep it open.
USIM1_RST	144	DO	UIM1 reset	
USIM1_CLK	143	DO	UIM1 clock	
USIM1_DATA	142	DI/DO	UIM1 data	Pull up USIM1_DATA to USIM1_VDD by the external 10K resistor
USIM1_VDD	141	PO	LDO 14 output for UIM1, 1.8V/2.95V	

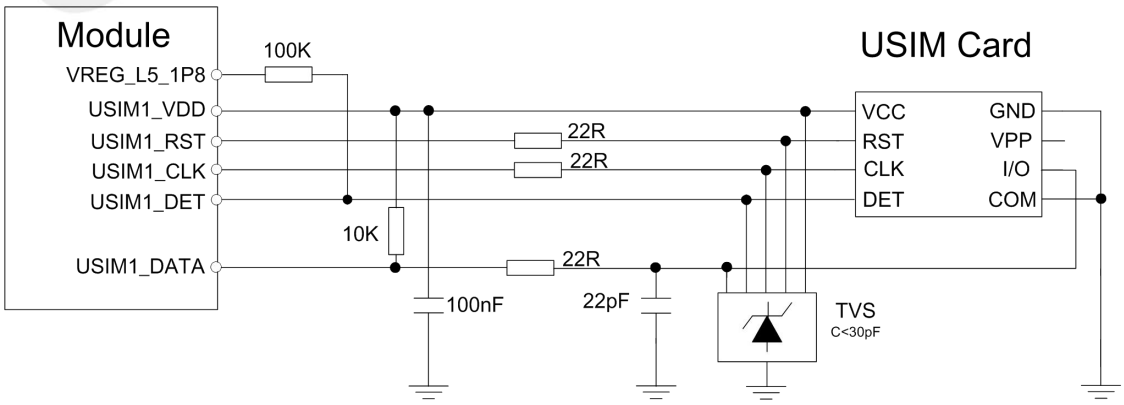

Figure 27: UIM card reference circuit

3.14 ADC

SIM8960x provides one 15bits ADC. Its performance parameters are shown in the following table:

Table 28: ADC performance parameters

Parameter	Test conditions	Min	Typ	Max	Units
Input voltage range	Programmable	0.1 0.3	- -	1.7 4.5	V
Resolution		-	15	-	bits
Analog input bandwidth		-	100	-	kHz
Sample rate	XO/8	-	2.4	-	MHz
INL	15-bit output	-	-	±8	LSB
DNL	15-bit output	-	-	±4	LSB
Offset error	Relative to full-scale	-	-	±1	%
Gain error	Relative to full-scale	-	-	±1	%

Table 29: ADC interface pin definitions

Pin Name	Pin#	I/O	Description	Note
ADC	151	AI	ADC	Maximum input voltage is 1.7V.

3.15 Forced USB BOOT Interface

FORCED_USB_BOOT is the emergency download interface. FORCED_USB_BOOT is pulled up to VREG_L5_1P8, and the module can enter the emergency download mode. Used when the product does not start properly. To facilitate subsequent software upgrades and debugging, please reserve test points.

Table 30: FORCED USB BOOT definitions

Pin Name	Pin#	I/O	Description	Note
FORCED_USB_BOOT	57	DI	USB forced download signal, short-circuit to VREG_L5_1P8 at power-on to enter forced download mode.	Reserved test point
VREG_L5_1P8	9	PO	1.8V power supply of GPIO port, normally open, voltage is not adjustable	

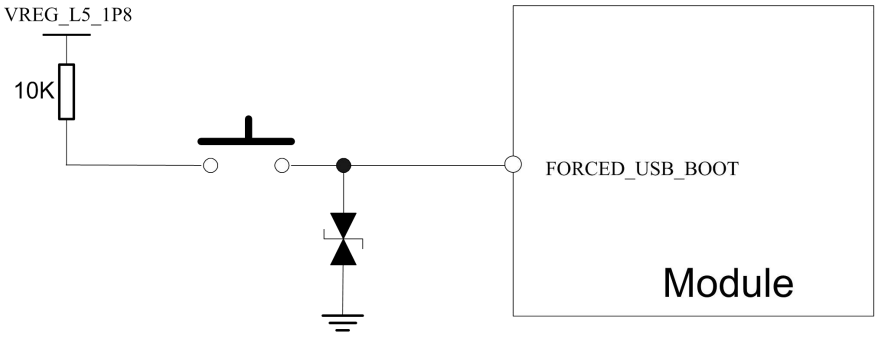

Figure 28: Emergency download reference circuit

3.16 Antenna Interface

SIM8960x provides four antenna interfaces including MAIN antenna, DRX antenna, GNSS antenna, and WiFi/BT antenna. To ensure good RF performance, users should meet the following requirements:

- Keep the RF traces at 50Ω.
- Maintain a complete and continuous reference ground plane from antenna pin to the RF connector.
- The RF traces should be away from any other noisy traces.
- Keep the RF traces as short as possible.

3.16.1 MAIN Antenna reference circuit

The recommended circuit is shown in the following figures:

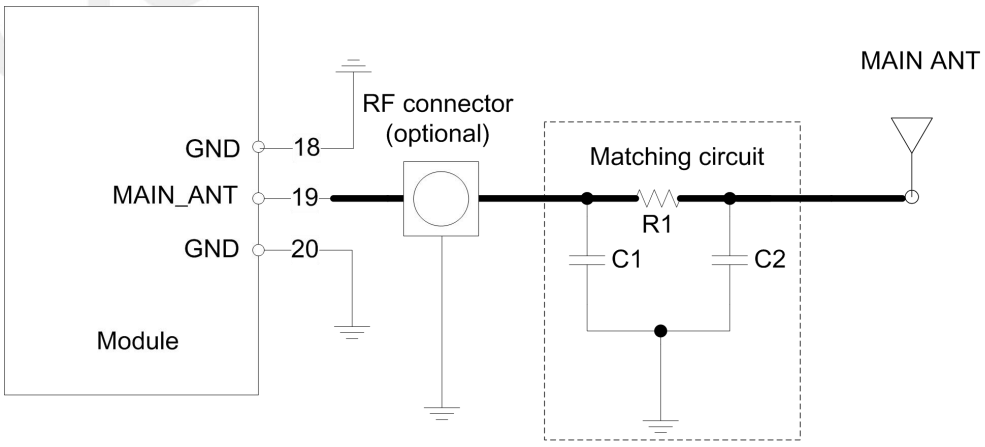

Figure 29: MAIN antenna recommended circuit

R1, C1 and C2 are antenna matching components in Figure 29, the value of these components are determined according to the antenna tuning results. By default, R1 is 0Ω, C1 and C2 are reserved. The RF connector in Figure 29 is used to ensure the accuracy and convenience of the conduction testing, so SIMCOM suggest keeping it. If considering Low-Cost BOM, user can cancel the connector.

3.16.2 DRX Antenna reference circuit

The recommended circuit is shown in the following figures:

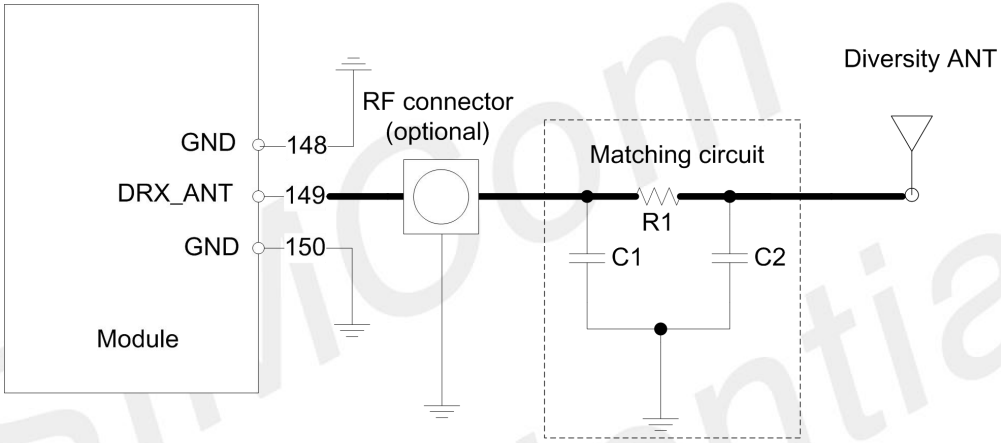

Figure 30: DRX antenna recommended circuit

R1, C1 and C2 are antenna matching components in Figure 30, the value of these components are determined according to the antenna tuning results. By default, R1 is 0Ω, C1 and C2 are reserved.The RF connector in Figure 30 is used to ensure the accuracy and convenience of the conduction testing, so SIMCOM suggest keeping it. If considering Low-Cost BOM, user can cancel the connector.

3.16.3 GNSS Antenna reference circuit

The recommended circuit is shown in the following figures:

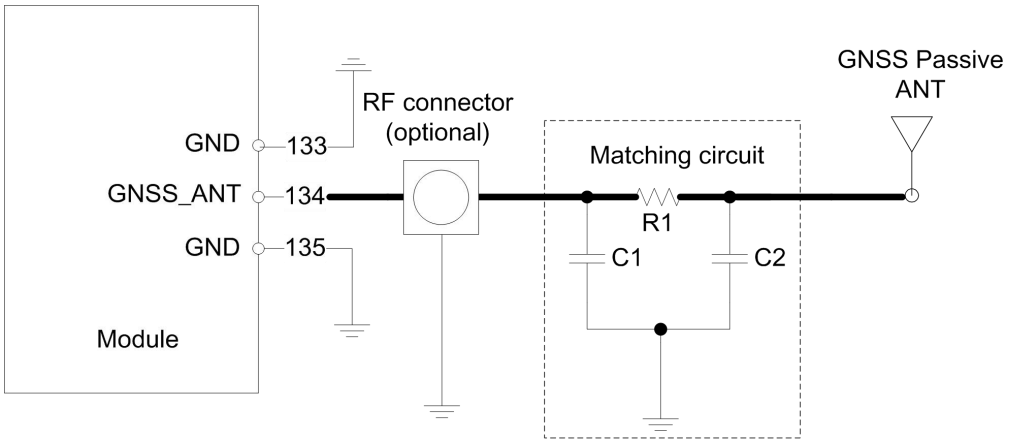

Figure 31: GNSS antenna recommended circuit

R1, C1 and C2 are antenna matching components in Figure 31, the value of these components are determined according to the antenna tuning results. By default, R1 is 0Ω, C1 and C2 are reserved. The RF connector in Figure 31 is used to ensure the accuracy and convenience of the conduction testing, so SIMCOM suggest keeping it. If considering Low-Cost BOM, user can cancel the connector.

The module has internal LAN, so there is no need for external active antenna. But if the antenna is far away the module and need a long cable to connect, users can use external active antenna, the recommended circuit is shown as Figure 32:

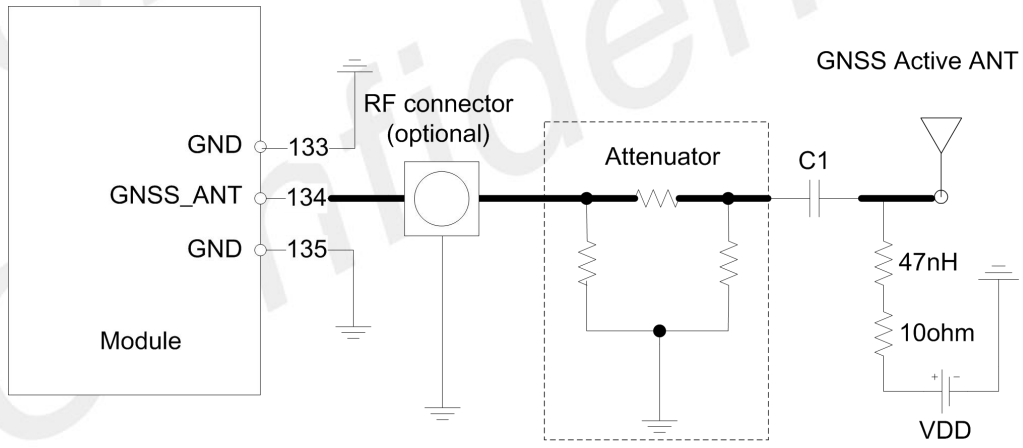

Figure 32: GNSS active antenna circuit

The attenuator in Figure 32 must be added as required and attenuation value is determined according to the active antenna gain. Normally, the relationship between the attenuation value and the gain satisfies the following formula:

Antenna gain=Attenuation value + Cable Losses

In Figure 32, the VDD is used to provide voltage to the external active antenna and its value should be taken according to antenna characteristic; C1 is used for DC blocking and its value is 33pF by default. The RF connectors used to ensure the accuracy and convenience of the conduction testing, if considering

LOW-Cost BOM, users can cancel it.

3.16.4 WiFi/BT Antenna reference circuit

The recommended circuit is shown in the following figures:

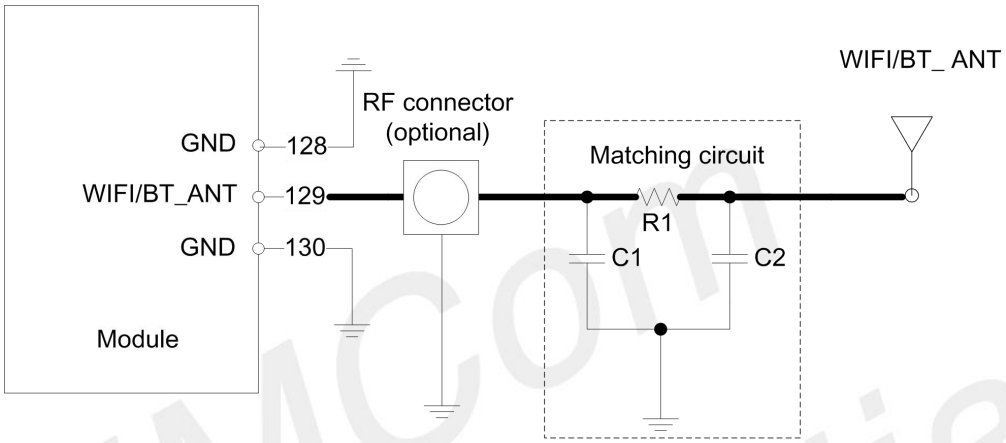

Figure 33: WIFI/BT antenna recommended circuit

R1, C1 and C2 are antenna matching components in Figure 33, the value of these components are determined according to the antenna tuning results. By default, R1 is 0Ω, C1 and C2 are reserved. The RF connector in Figure 33 is used to ensure the accuracy and convenience of the conduction testing, so SIMCOM suggest keeping it. If considering Low-Cost BOM, user can cancel the connector.

3.16.5 RF traces layout guidance

The characteristic impedance of RF signals should be controlled at 50 ohm. In general, the impedance of RF signal is determined by the Permittivity (ER) of PCB material, line width (W), ground clearance (S), height of reference ground plane (H) and other factors.

Microstrip line and coplanar waveguide are usually used to control the characteristic impedance of RF wiring. The following illustrations show the structure design of microstrip line and coplanar waveguide.

- **Microstrip line structure**

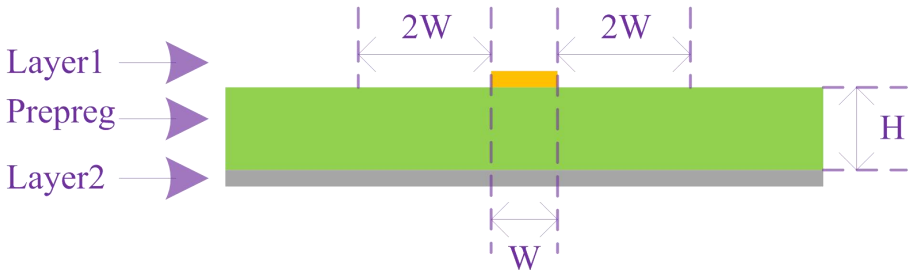

Figure 34: Two layer PCB microstrip structure

Table 31: Example of impedance control of microstrip line structure

PCB thickness	Permittivity (ER)	Line thickness	Layer	Reference plane	Target impedance	Expected linewidth W
1mm	4.2	0.035mm	Layer1	Layer2	50 ohm	1.7mm (67 mil)
1.6mm	4.2	0.035mm	Layer1	Layer2	50 ohm	3mm (118 mil)

- Coplanar waveguide (CPW) structure (recommended)

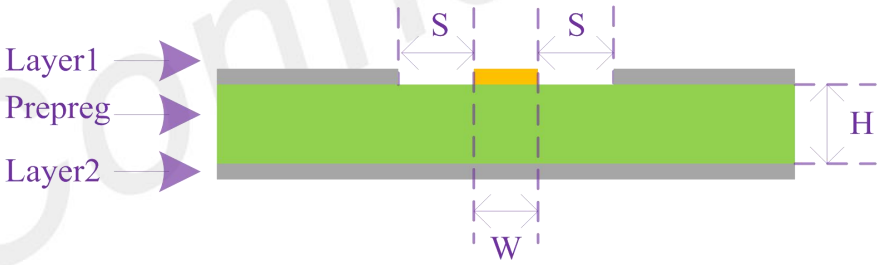

Figure 35: Two layer PCB coplanar waveguide structure

Table 32: Example of impedance control of coplanar waveguide structure

PCB thickness	Permittivity (ER)	Line thickness	Layer	Reference plane	Target impedance	Expected gap to ground S	Expected linewidth W
1mm	4.2	0.035mm	Layer 1	Layer2	50 ohm	0.65mm (25.6 mil)	0.2mm (7.8 mil)

1.6mm	4.2	0.035mm	Layer 1	Layer2	50 ohm	0.65mm (25.6 mil)	0.15mm (5.9 mil)

Four layer PCB coplanar waveguide structure 1# is shown in following figure. The third layer is reference layer.

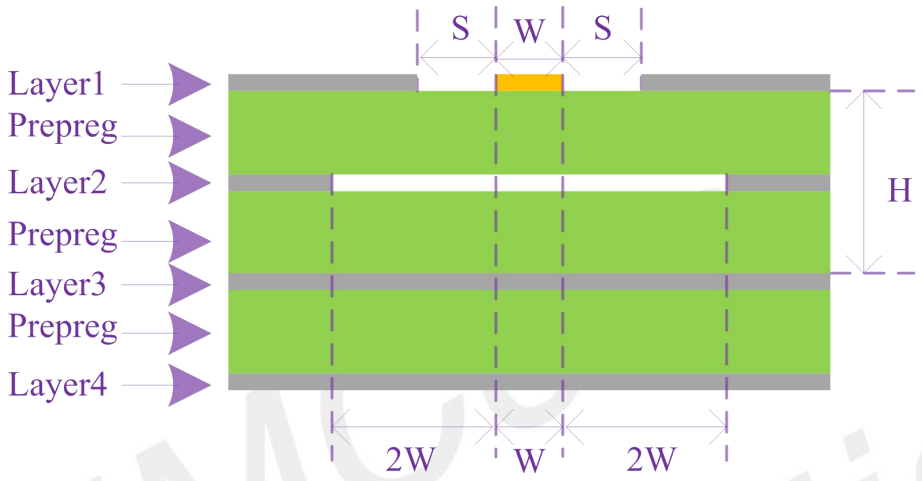

Figure 36: Four layer PCB coplanar waveguide structure 1#

Four layer PCB coplanar waveguide structure 2# is shown in following figure. The fourth layer is reference layer.

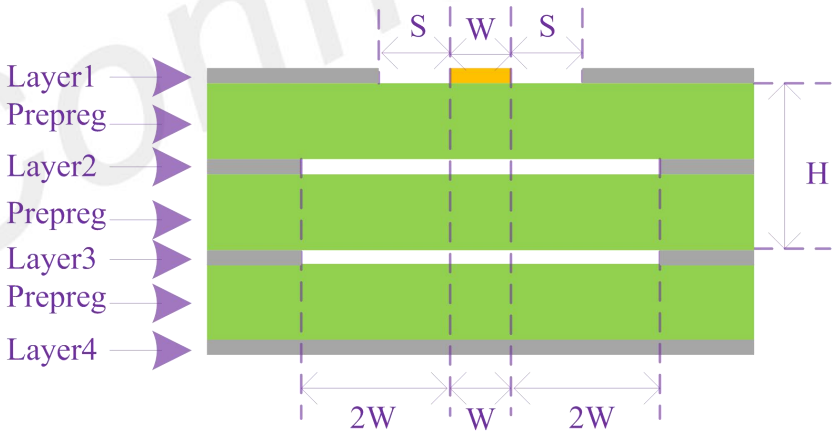

Figure 37: Four layer PCB coplanar waveguide structure 2#

3.16.6 Antenna Requirement

The following table shows the requirements on main antenna, Rx-diversity antenna and GNSS antenna.

Table 33: Antenna Requirement

Antenna	Requirements
GSM/WCDMA/TD-SCDMA/LTE	VSWR: ≤ 2 Gain (dBi): >1 Max Input Power (W): 50 Input Impedance (ohm): 50 Polarization Type: Vertical
Wi-Fi/BT	VSWR: ≤ 2 Gain (dBi): 1 Max Input Power (W): 50 Input Impedance (ohm): 50 Polarization Type: Vertical
GNSS	Frequency range: 1565 - 1607MHz Polarization: RHCP or linear VSWR: < 2 (Typ.) Passive antenna gain: > 0dBi Active antenna noise figure: < 1.5dB Active antenna gain: > 0dBi Active antenna embedded LNA gain: <17dB

3.16.7 Install the Antenna with RF Connector

The recommended RF connector is HIROSE UF.L-R-SMT. The antenna installation with RF connector is shown in following figure.

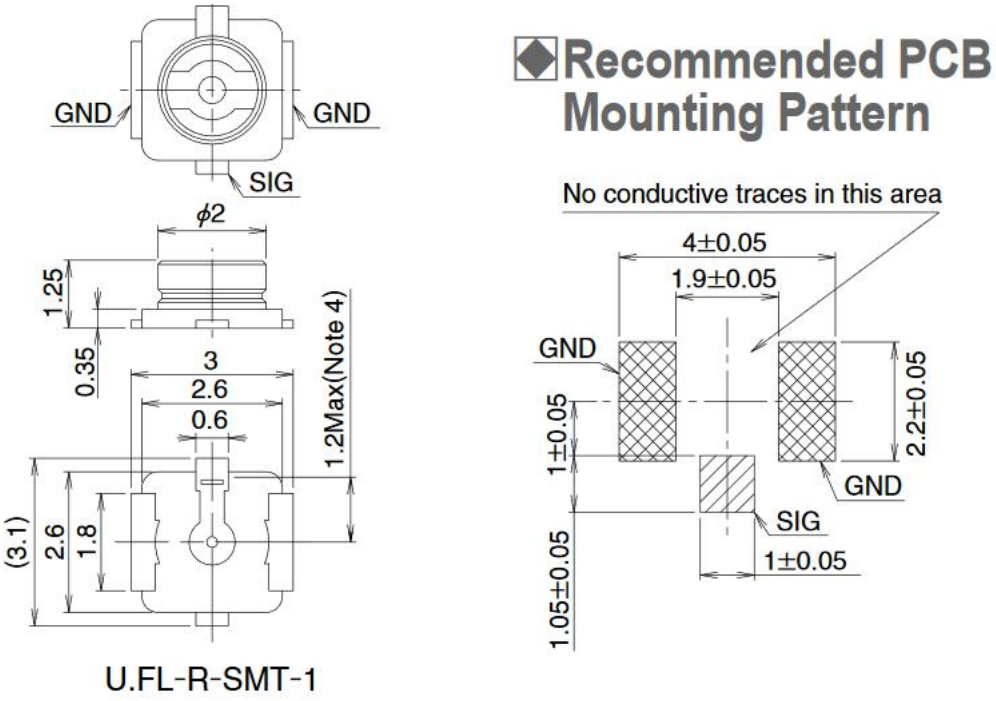

Figure 38: Dimensions of the UF.L-R-SMT Connector (Unit: mm)

4 PCB Layout

This section provides PCB layout guidelines for SIM8960x users to ensure their production against lots of issues, and achieve the optimum performance.

4.1 Stack-up Options

At least, 4-layer through-hole PCB should be chosen for good impedance control and signal shielding.

4.2 General Placement Guidelines

- Digital devices and traces should not be placed near sensitive signals like RF and clock.
- Keep SPKR and MIC away from sensitive RF lines.

4.3 PCB Layout Guideline Details

4.3.1 RF Trace

- RF connector should be placed close to the module's antenna pin.
- Antenna matching circuit should be placed close to the antenna.
- Keep the RF traces at 50Ω.
- Maintain a complete and continuous reference ground plane from antenna pin to the RF connector.
- The RF traces should be far away from any other noisy traces.
- Keep the RF traces as short as possible.
- If using a coaxial RF cable to connect the antenna, please avoid spanning on UIM cards, power circuits and high-speed digital circuits to minimize the impact of each other.

4.3.2 Power/GND

- Both VBAT and return path should be as short and wide as possible to minimize the IR drop
- The VBAT current should go through Zener diode, capacitors, then VBAT pins
- Must have a solid ground plane throughout the board as the primary reference plane for most signals

4.3.3 UIM Card

- Ensure UIM card holder is far way from antenna or RF signal
- ESD component and bypass caps should be placed closed to UIM Card
- UIM card signals should be far away from other high-speed signal

4.3.4 MIPI_DSI/CSI

- Protect MIPI_DSI/CSI signals from noisy signals (clocks, SMPS, etc.)
- Differential pairs, 100 Ω nominal, ±10%
- Total routing length <305 mm
- Intra-pair length matching < 5 ps (0.67 mm)
- Inter-pair length matching < 10 ps (1.3 mm)
- Lane-to-lane trace spacing = 3x line width
- Spacing to all other signals = 4x line width
- Maintain a solid ground reference for clocks to provide a low-impedance path for return currents
- Each trace needs to be next to a ground plane
- Minimize the number of via on the trace

4.3.5 USB

- 90 Ω differential, ± 10% trace impedance
- Differential data pair matching <6.6 mm (50 ps)
- External components should be located near the USB connector.
- Should be routed away from sensitive circuits and signals.
- If there are test points, place them on the trace to keep branches as short as possible

4.3.6 SDC

- Protect other sensitive signals/circuits from SDC corruption.
- Protect SDC signals from noisy signals (clocks, SMPS, etc.).
- Up to 200 MHz clock rate
- 50 Ω nominal, ±10% trace impedance
- CLK to DATA/CMD length matching <1 mm
- 30–35 Ω termination resistor on clock lines near the module
- Total routing length <50 mm recommended
- Spacing to all other signals = 2x line width
- Bus capacitance < 15 pF

4.3.7 Audio

Analog input

- 4 to 5 mil trace widths; 4 to 5 mil spacing between traces

- Differential route for MIC1P with MIC1N and MIC2P with GND_MIC;
- Isolate from noise sources, such as antenna, RF signals, SMPS, clocks, and other digital signals with fast transients

Analog output

- Coplanar ground fill on both sides (of traces or pair as appropriate); in between ground planes – grounds above and below
- Isolate from noise sources such as antenna, RF signals, SMPS, clocks, and other digital signals with fast transients.
- EAR output signal – route as differential pair with 10 mil trace widths.
- SPKR output signals – route as differential pair with 20 mil trace widths with 8 Ω load and 25 mil trace widths with 4 Ω load
- HPH output signals – not a differential pair; 10 mil trace widths for HPH_L and HPH_R; 15 mil trace widths for HPH_REF
- Connect HPH_REF to the ground pin of the jack connector and route HPH_REF in between HPH_L and HPH_R for best crosstalk minimization

5 Electrical and Reliability

5.1 Absolute Maximum Ratings

Absolute maximum ratings reflect the stress levels that, if exceeded, may cause permanent damage to the device. Functionality and reliability are only guaranteed within the operating conditions.

Table 34: Absolute maximum ratings

Parameter	Min	Max	Unit
VBAT	-0.3	5	V
VBUS	-0.3	16	V
VRTC	-	3.5	V

5.2 Temperature Range

Table 35: Temperature range

Parameter	Min	Typ	Max	Unit
Operating temperature	-35	25	+75	℃
Storage temperature	-40		+90	℃

5.3 Operating Voltage

Table 36: Operating voltage

Parameter	Min	Typ	Max	Unit
VBAT	3.4	3.9	4.4	V
VBUS	4.35	5	10	V
VRTC	2.0	3.0	3.25	V

5.4 Digital-logic Characteristics

Table 37: 1.8 V digital I/O characteristics

Parameter	Description	Min	Typ	Max	Unit
V_{IH}	High-level input voltage	1.17	-	-	V
V_{IL}	Low-level input voltage	-	-	0.63	V
V_{OH}	High-level output voltage	1.35	-	-	V
V_{OL}	Low-level output voltage	-	-	0.45	V

Table 38: USIM interface characteristics (USIM_VDD=1.8V/2.95V)

Parameter	Description	Min	Typ	Max	Unit
V_{IH}	High-level input voltage	0.7* USIM_VDD	-	USIM_VDD+0.3	V
V_{IL}	Low-level input voltage	-0.3	-	0.2* USIM_VDD	V
V_{OH}	High-level output voltage	0.8*USIM_VDD	-	USIM_VDD	V
V_{OL}	Low-level output voltage	0	-	0.4	V

Table 39: SD interface characteristics (SD_LDO11 =1.8V)

Parameter	Description	Min	Typ	Max	Unit
V_{IH}	High-level input voltage	1.27	-	2	V
V_{IL}	Low-level input voltage	-0.3	-	0.58	V
V_{OH}	High-level output voltage	1.4	-	-	V
V_{OL}	Low-level output voltage	0	-	0.45	V

Table 40: SD interface characteristics (SD_LDO11 =2.95V)

Parameter	Description	Min	Typ	Max	Unit
V_{IH}	High-level input voltage	1.84	-	3.25	V
V_{IL}	Low-level input voltage	-0.3	-	0.74	V
V_{OH}	High-level output voltage	2.21	-	2.95	V
V_{OL}	Low-level output voltage	0	-	0.37	V

5.5 Current Consumption (VBAT=3.9V)

Table 41: Current consumption(TBD)

Parameter	Conditions	Typ.	Max	Unit
Leakage current	Off mode	29	80	uA
Standby current	Flight mode	3.5	3.7	mA
	GSM@BS-PA-MFRMS=2	2.53	5	mA
	WCDMA @DRX=8	3.29	5	mA
	TD-SCDMA @DRX=7	3.14	5	mA
	LTE-FDD @standby 1.28s	3.95	5	mA
	LTE-TDD @standby 1.28s	4.0	5	mA
GSM Voice call	GSM850 @PCL5 32.4dBm Ch=189	256	300	mA
	DCS1800 @PCL0 29.3dBm Ch=698	191	250	mA
WCDMA Voice call	Band 1 @max power 22.8dBm Ch=10700	585	600	mA
	Band 5 @max power 23dBm Ch=4408	560	570	mA
	Band 8 @max power 22.4dBm Ch=3012	500	570	mA
FDD-LTE	B1 power@ 23dBm BW=20MHZ Ch=18300	690	700	mA
	B3 power@ 22.3dBm BW=20MHZ Ch=19575	664	700	mA
	B5 power@ 22.5dBm BW=10MHZ Ch=20525	486	600	mA
	B7 power@ 22.2dBm BW=10MHZ Ch=21100	600	700	mA
	B8 power@ 22.8dBm BW=20MHZ Ch=21625	547	600	mA
	B20 power@ 22.1dBm BW=20MHZ Ch=24300	526	600	mA
TDD-LTE	B34 power@ 22.8dBm BW=15MHZ Ch=36275	290	600	mA
	B38 power@ 23dBm BW=20MHZ Ch=38000	300	600	mA
	B39 power@ 22.3dBm BW=20MHZ Ch=38450	297	600	mA
	B40 power@ 23dBm BW=20MHZ Ch=39150	340	600	mA
	B41 power@ 23dBm BW=20MHZ Ch=40740	307	600	mA
Peak current			3	A

5.6 Electro-Static Discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, it may result in destructive damage.

SIM8960x must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, Protection of Electrical and Electronic Parts, Assemblies, and Equipment.

Table 42: ESD performance parameters（Temperature: 25℃, Humidity: 45%）

Pin	Contact discharge	Air discharge
VBAT	±5KV	±10 KV
GND	±6KV	±12KV
Antenna	±5KV	±10KV
PWRKEY	±4KV	±6KV

5.7 Module Operating Frequencies

Table 43: Module operating frequencies

Frequency	Receive	Transmit	Physical channel
GSM850	869-894MHz	824-849MHz	128-251
EGSM900	925-960MHz	880-915MHz	0-124, 975-1023
DCS1800	1805-1880MHz	1710-1785MHz	512-885
PCS1900	1930-1990MHz	1850-1910MHz	512-810
WCDMA B1	2110-2170 MHz	1920-1980 MHz	TX: 9612-9888 RX: 10562-10838
WCDMA B2	1930-1990MHz	1850-1910MHz	TX: 9262-9538 RX: 9662-9938
WCDMA B4	2110-2155MHz	1710-1755MHz	TX: 1312-1862 RX: 1537-2087
WCDMA B5	869-894MHz	824-849MHz	TX: 4132-4233 RX: 4357-4458
WCDMA B8	925-960MHz	880-915 MHz	TX: 2712-2863 RX: 2937-3088
TDSCDMA B39	1880-1920 MHz	1880-1920MHz	9400-9600
TDSCDMA B34	2010-2025 MHz	2010-2025MHz	10054-10121
LTE B1	2110-2170 MHz	1920-1980 MHz	TX: 18000-18599 RX: 0-599
LTE B2	1930-1990MHz	1850-1910MHz	TX: 18600-19199 RX: 600-1199
LTE B3	1805-1880 MHz	1710-1785 MHz	TX: 19200-19949 RX: 1200-1949
LTE B4	2110-2155MHz	1710-1755MHz	TX: 19950-20399 RX: 1950-2399
LTE B5	869-894 MHz	824-849MHz	TX: 20400-20649 RX: 2400-2649
LTE B7	2620-2690 MHz	2500-2570 MHz	TX: 20750-21449 RX: 2750-3449
LTE B8	925-960 MHz	880-915 MHz	TX: 21450-21799 RX: 3450-3799
LTE B12	729-746MHz	699-716MHz	TX: 23010-23179 RX: 5010-5179
LTE B13	746-756MHz	777-787MHz	TX: 23180-23279 RX: 5180-5279
LTE B17	734-746MHz	704-716MHz	TX: 23730-23849 RX: 5730-5849
LTE B20	791-821MHz	832-862MHz	TX: 24150-24449 RX: 6150-6449
LTE B25	1850-1915MHz	1930-1995MHz	TX: 26040-26689 RX:8040-8689
LTE B26	859-894MHz	814-849MHz	TX: 26690-27039 RX: 8690-9039
LTE B34	2010-2025 MHz	2010-2025 MHz	36200-36349
LTE B38	2570-2620 MHz	2570-2620 MHz	37750-38249
LTE B39	1880-1920 MHz	1880-1920 MHz	38250-38649

LTE B40	2300-2400 MHz	2300-2400 MHz	38650-39649
LTE B41	2555-2655 MHz	2555-2655MHz	40240-41240

5.8 Module Output power

Table 44: Conducted transmission power

Frequency	Power	Min.
GSM850	33dBm ±2dB	5dBm ± 5dB
E-GSM900	33dBm ±2dB	5dBm ± 5dB
DCS1800	30dBm ±2dB	0dBm ± 5dB
PCS1900	30dBm ±2dB	0dBm ± 5dB
GSM850(8-PSK)	27dBm ±3dB	5dBm ± 5dB
E-GSM900 (8-PSK)	27dBm ±3dB	5dBm ± 5dB
DCS1800 (8-PSK)	26dBm +3/-4dB	0dBm ±5dB
PCS1900(8-PSK)	26dBm +3/-4dB	0dBm ±5dB
WCDMA B1	24dBm +1/-3dB	<-50dBm
WCDMA B2	24dBm +1/-3dB	<-50dBm
WCDMA B4	24dBm +1/-3dB	<-50dBm
WCDMA B5	24dBm +1/-3dB	<-50dBm
WCDMA B8	24dBm +1/-3dB	<-50dBm
TDSCDMA B34	24dBm +1/-3dB	<-50dBm
TDSCDMA B39	24dBm +1/-3dB	<-50dBm
LTE-FDD B1	23dBm +/-2.7dB	<-40dBm
LTE-FDD B2	23dBm +/-2.7dB	<-40dBm
LTE-FDD B3	23dBm +/-2.7dB	<-40dBm
LTE-FDD B4	23dBm +/-2.7dB	<-40dBm
LTE-FDD B5	23dBm +/-2.7dB	<-40dBm
LTE-FDD B7	23dBm +/-2.7dB	<-40dBm
LTE-FDD B8	23dBm +/-2.7dB	<-40dBm
LTE-FDD B12	23dBm +/-2.7dB	<-40dBm
LTE-FDD B13	23dBm +/-2.7dB	<-40dBm
LTE-FDD B17	23dBm +/-2.7dB	<-40dBm
LTE-FDD B20	23dBm +/-2.7dB	<-40dBm
LTE-FDD B25	23dBm +/-2.7dB	<-40dBm
LTE-FDD B26	23dBm +/-2.7dB	<-40dBm
LTE-TDD B34	23dBm +/-2.7dB	<-40dBm
LTE-TDD B38	23dBm +/-2.7dB	<-40dBm
LTE-TDD B39	23dBm +/-2.7dB	<-40dBm

LTE-TDD B40	23dBm +/-2.7dB	<-40dBm
LTE-TDD B41	23dBm +/-2.7dB	<-40dBm

5.9 Module Receiving Sensitivity

Table 45: Conducted receiving sensitivity

Band	Receiving sensitivity（Typ）	Receiving sensitivity（Max）
GSM850	< -108dBm	3GPP standard
EGSM900	< -108dBm	3GPP standard
DCS1800	< -108dBm	3GPP standard
PCS1900	< -108dBm	3GPP standard
WCDMA B1	<-109dBm	3GPP standard
WCDMA B2	<-109dBm	3GPP standard
WCDMA B4	<-109dBm	3GPP standard
WCDMA B5	<-109dBm	3GPP standard
WCDMA B8	<-109dBm	3GPP standard
TDSCDMA B34	<-110dBm	3GPP standard
TDSCDMA B39	<-110dBm	3GPP standard
LTE FDD/TDD	Table 46	3GPP standard

Table 46: Reference sensitivity QPSk PREFSENS(LTE)

E-UTRA Band number	1.4 MHz	3 MHz	5 MHz	10 MHz	15 MHz	20 MHz	Duplex mode
1	-	-	-100	-97	-95.2	-94	FDD
2	-102.7	-99.7	-98	-95	-93.2	-92	FDD
3	-101.7	-98.7	-97	-94	-92.2	-91	FDD
4	-104.7	-101.7	-100	-97	-95.2	-94	FDD
5	-103.2	-100.2	-98	-95			FDD
6	-	-	-100	-97			FDD
7	-	-	-98	-95	-93.2	-92	FDD
8	-102.2	-99.2	-97	-94			FDD
9	-	-	-99	-96	-94.2	-93	FDD
10	-	-	-100	-97	-95.2	-94	FDD
11	-	-	-100	-97			FDD
12	-101.7	-98.7	-97	-94			FDD

13			-97	-94			FDD
14		-	-97	-94			FDD
17	-	-	-97	-94			FDD
18	-	-	-100	-97	-95.2	-	FDD
19	-	-	-100	-97	-95.2	-	FDD
20			-97	-94	-91.2	-90	FDD
21			-100	-97	-95.2		FDD
22			-97	-94	-92.2	-91	FDD
23	-104.7	-101.7	-100	-97			FDD
24			-100	-97			FDD
25	-101.2	-98.2	-96.5	-93.5	-91.7	-90.5	FDD
33	-	-	-100	-97	-95.2	-94	TDD
34	-	-	-100	-97	-95.2	-	TDD
35	-106.2	-102.2	-100	-97	-95.2	-94	TDD
36	-106.2	-102.2	-100	-97	-95.2	-94	TDD
37	-	-	-100	-97	-95.2	-94	TDD
38	-	-	-100	-97	-95.2	-94	TDD
39	-	-	-100	-97	-95.2	-94	TDD
40	-	-	-100	-97	-95.2	-94	TDD
41	-	-	-99	-96	-94.2	-93	TDD
42	-	-	-99	-96	-94.2	-93	TDD
43	-	-	-99	-96	-94.2	-93	TDD

5.10 WIFI Main RF Characteristics

Table 47: 2.4GWIFI main RF Characteristics

Transmission performance			
	802.11B（11M）	802.11G（54M）	802.11N (MCS7)
Output power	17dBm±2dB	15dBm±2dB	13dBm±2dB
EVM	<35%	<-25dB	<-27dB
Receiving performance			
	802.11B（11M）	802.11G（54M）	802.11N (MCS7)
Receiving sensitivity	≤-88dBm	≤-73dBm	≤-72dBm

Table 48: 5G WIFI main RF Characteristics

Transmission performance			
	802.11A（54M）	802.11N (MCS7)	802.11AC (MCS8)
Output power	15dBm±2dB	14dBm±2dB	13dBm±2dB
EVM	<-25dB	<-27dB	<-30dB
Receiving performance			
	802.11A（54M）	802.11N (MCS7)	802.11AC (MCS8)
Receiving sensitivity	≤-71dBm	≤-70dBm	≤-65dBm

5.11 BT Main RF Characteristics

Table 49: BT Main RF Characteristics

Transmission performance			
	DH5	2DH5	3DH5
Output power	11dBm±2dB	10dBm±2dB	9dBm±2dB
Receiving performance			
	DH5	2DH5	3DH5
Receiving sensitivity	≤-90dBm	≤-80dBm	≤-80dBm

5.12 GNSS Main RF Characteristics

Table 50: GNSS Main RF Characteristics

Receiver type	GPS,GLANOSS,BEIDOU	
CNo	40dB/Hz@-130dBm	
Sensitivity	Tracking & Navigation	-160dBm
	Reacquisition	-156dBm
	Cold start	-148dBm
TTFF	Cold start	<35s
	Warm start	<15s
	Hot start	<5s

6 Manufacturing

6.1 Top and Bottom View of SIM8960x

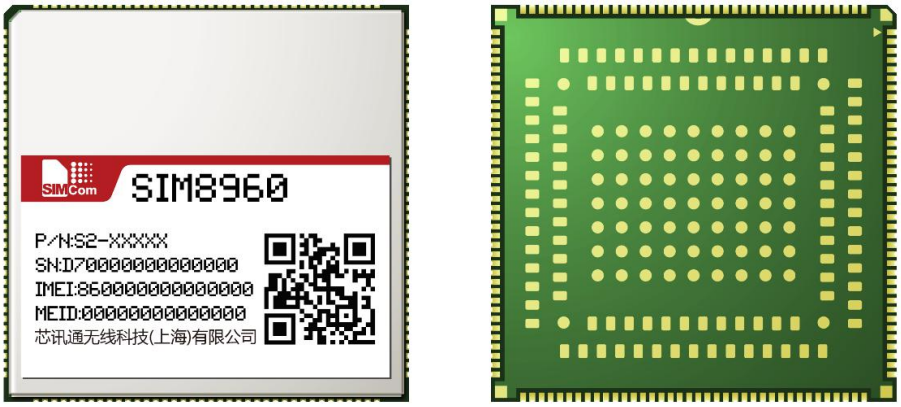

Figure 39: Top and bottom view of SIM8960x

6.2 Physical Dimensions

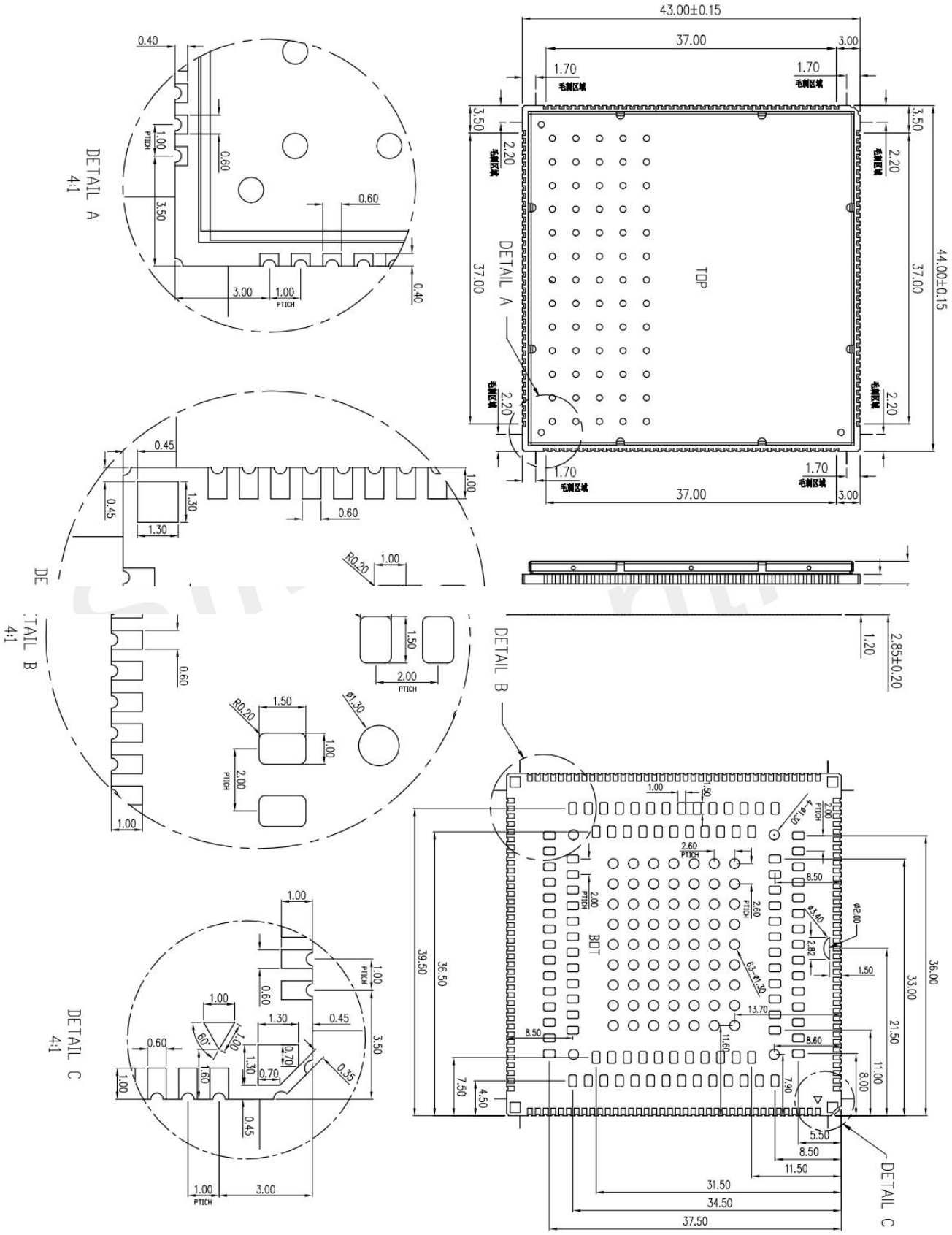

Figure 40: Outline drawing (unit: mm)

6.3 Recommended PCB footprint

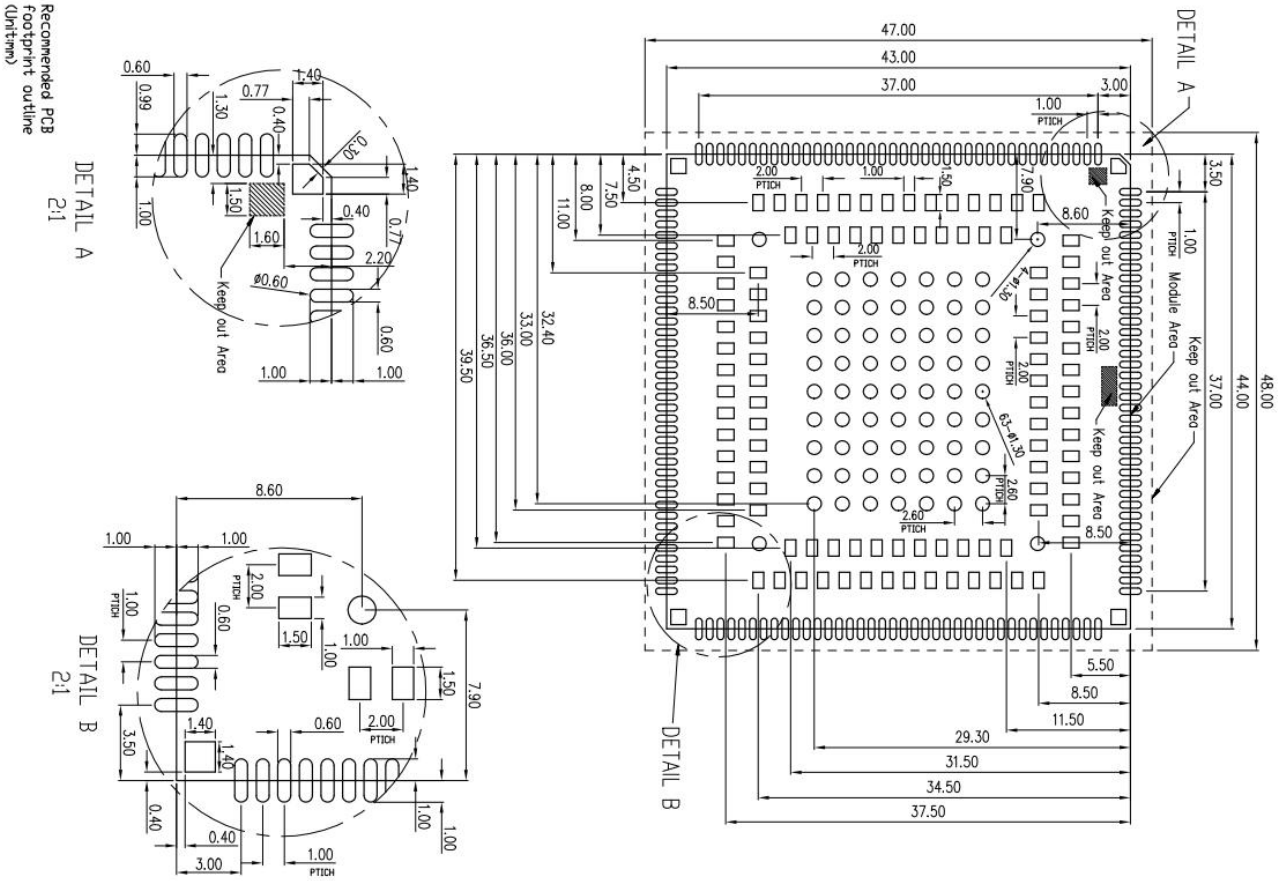

Figure 41: Recommended PCB footprint

6.4 Recommended SMT Stencil

Stencil thickness requirement：

- The stencil thickness of outer circle’ s pin need 0.18mm

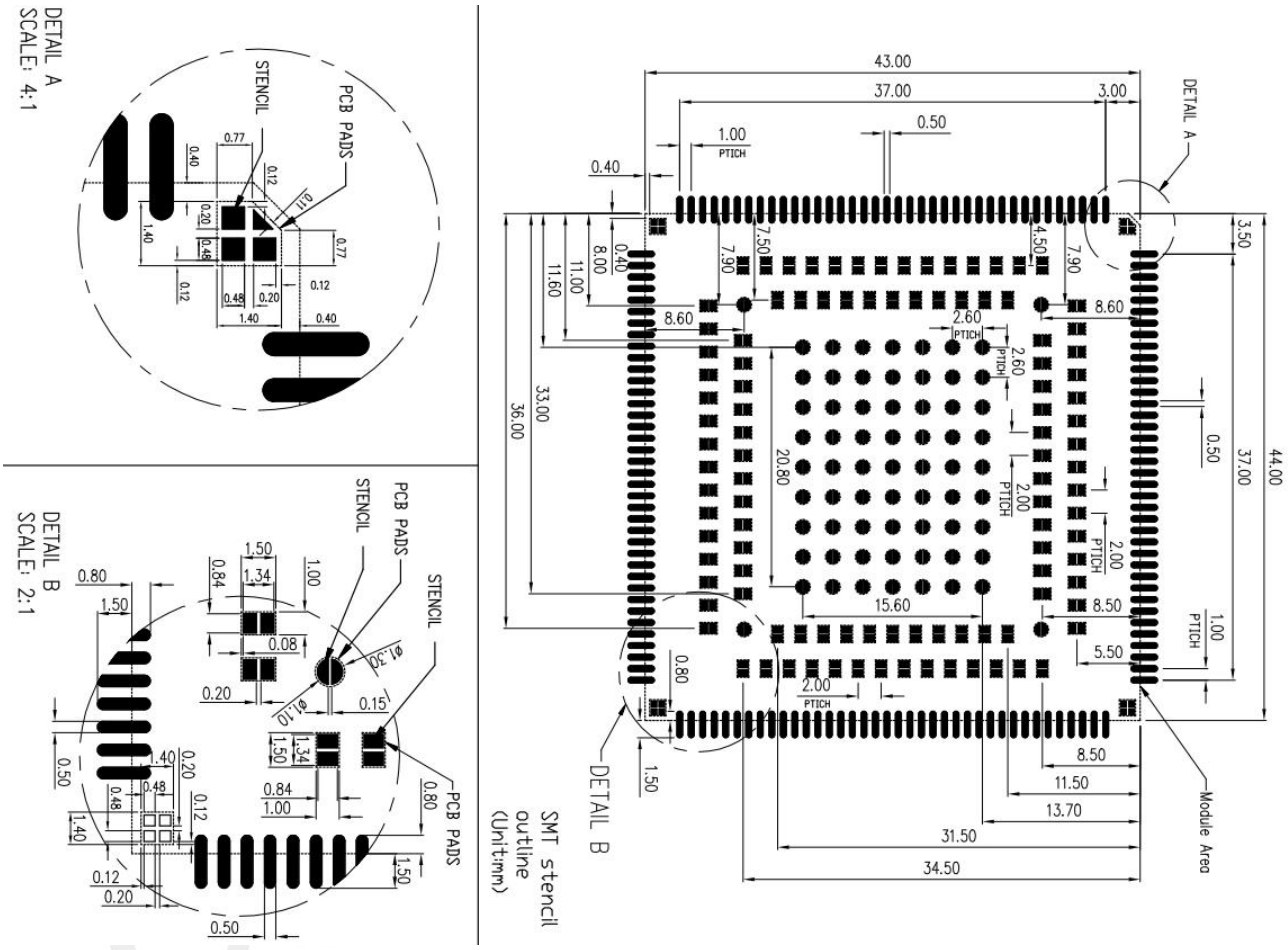

Figure 42: Recommended SMT stencil

6.5 Typical SMT Reflow Profile

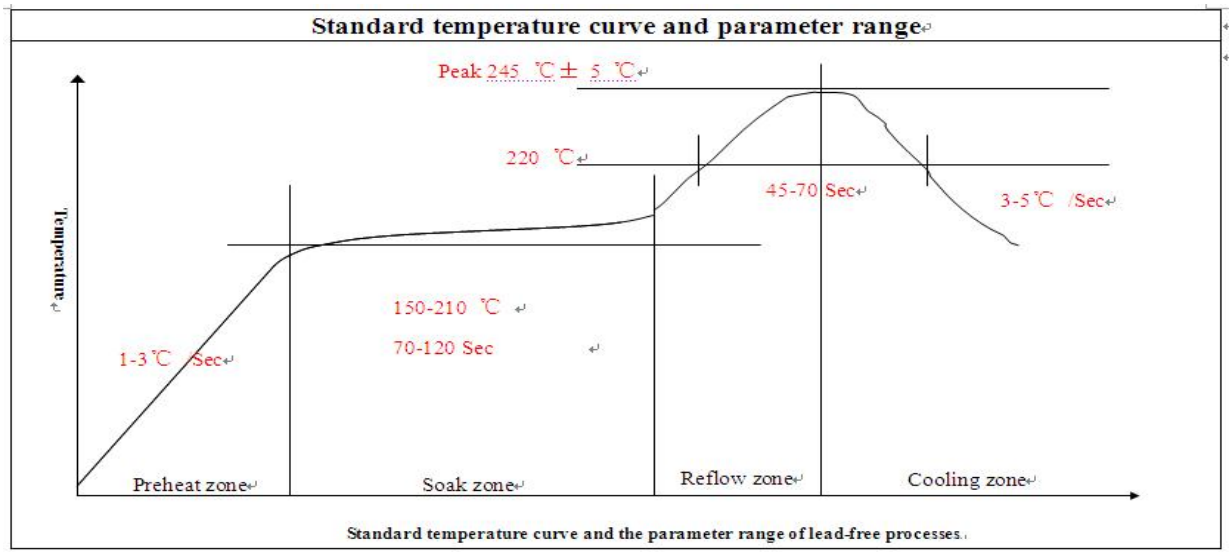

Figure 43: Typical SMT reflow profile

NOTE

1. Refer to “Module secondary-SMT-UGD” for more information about the module shipping and manufacturing.

6.6 Moisture Sensitivity Level (MSL)

SIM8960x is susceptible to damage induced by absorbed moisture and high temperature. A package's moisture-sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in Table 51.

Table 51: MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤+30℃/85% RH
2	1 year	≤+30℃/60% RH
2a	4 weeks	≤+30℃/60% RH
3	168 hours	≤+30℃/60% RH
4	72 hours	≤+30℃/60% RH
5	48 hours	≤+30℃/60% RH
5a	24 hours	≤+30℃/60% RH
6	Mandatory bake before use. After bake, it must be reflowed within the time limit specified on the label.	≤+30℃/60% RH

The SDM450 device samples are currently classified as **MSL4** at 255 (+5, -0)°C, following the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification This qualification temperature (255°C) should not be confused with the peak temperature within the recommended solder reflow profile.

6.7 Baking Requirements

It is necessary to bake modules if the prescribed time limit has been exceeded. The baking conditions are specified in Table 55. Note that if baking is required, the devices must be transferred into trays that can be baked to at least 125°C.

Table 52: Baking requirements

Baking conditions options	Duration
40°C±5°C, <5% RH	192 hours
120°C±5°C, <5% RH	4 hours

7 Packing System

SIM8960x module supports tray packaging. The packaging process is shown in the following figures.

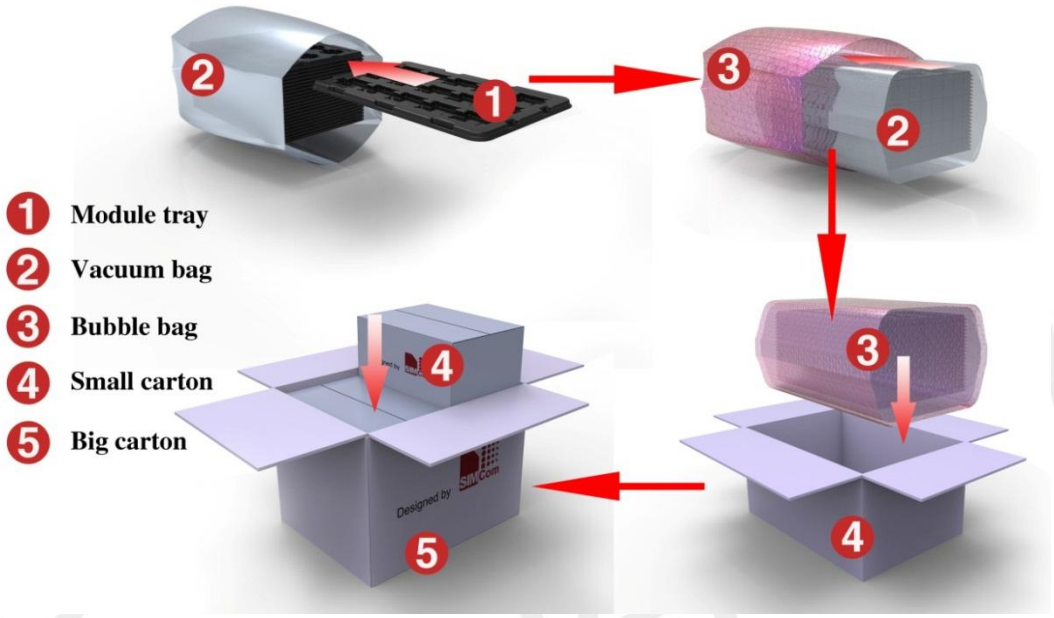

Figure 44: Packaging process

Module tray drawing：

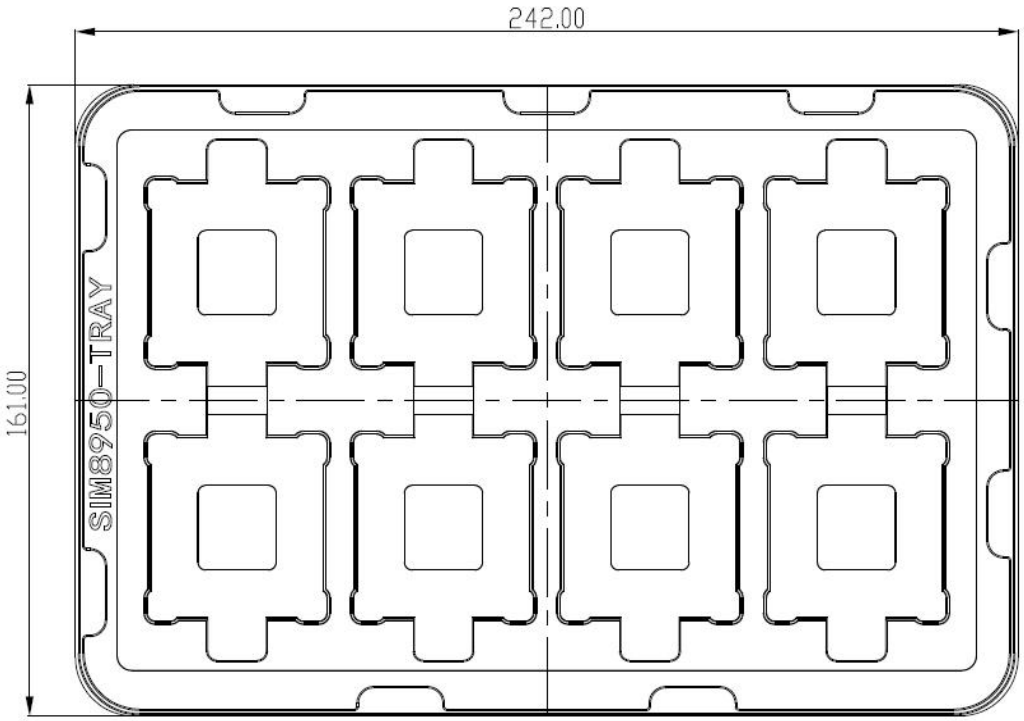

Figure 45: Module tray drawing

Table 53: Module tray information

Length（±3mm）	Width（±3mm）	Units per tray
242.0	161.0	8

Small carton drawing：

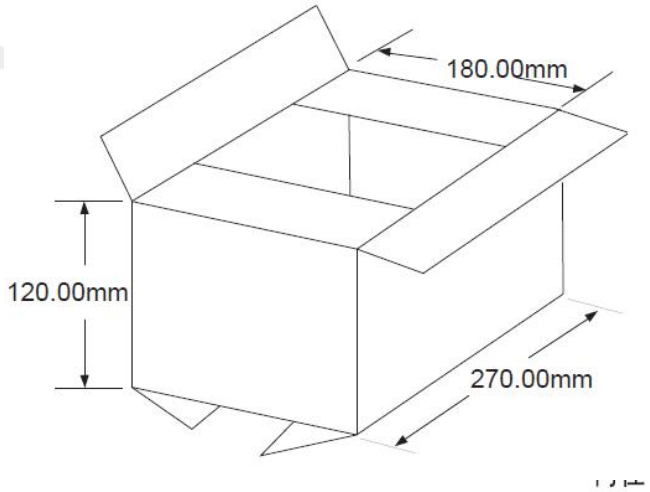

Figure 46: Small carton drawing

Table 54: Small carton information

Length（±10mm）	Width（±10mm）	Height（±10mm）	Units per carton
270	180	120	8*19-2=150

Big carton drawing：

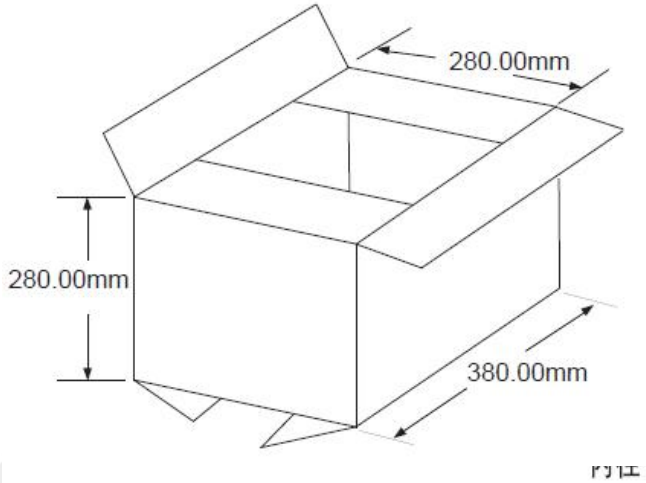

Figure 47: Big carton drawing

Table 55: Big carton information

Length（±10mm）	Width（±10mm）	Height（±10mm）	Count of small carton
380	280	280	150*4=600

8 List of Recommended Devices

Table 56: Recommended Camera Sensor List

	Resolution	Part Number	Sensor Vendor
Primary camera/ Secondary camera	2M	OV2680	OmniVision
	5M	OV5675	OmniVision
		OV5695	OmniVision
		S5K5E8	SAMSUNG
	8M	OV8856	OmniVision
		OV8858	OmniVision
		OV8865	OmniVision
		S5K4H8	SAMSUNG
Primary camera	12M	OV12890	OmniVision
		S5K2L7	SAMSUNG
		IMX362	SONY
	13M	AR1337	ON Semiconductor
		OV13853(PDAF)	OmniVision
		OV13855	OmniVision
		OV13870	OmniVision
		MN34153	Panasonic
		S5K2M8	SAMSUNG
		S5K3M2XM(PDAF)	SAMSUNG
		IMX258(PDAF)	SONY
	16M	OV16860	OmniVision
		OV16880	OmniVision
		S5K2P7	SAMSUNG
		S5K3P3	SAMSUNG
		S5K3P8	SAMSUNG
		IMX298 (PDAF)	SONY
	20M	IMX230	SONY
	23M	IMX318	OmniVision

Table 57: Recommended LCD Driver IC List

LCD Driver IC	Vendor	Resolution
OTM1902A	FocalTech	FHD
OTM1906C	FocalTech	FHD
HX8399-C	Himax	FHD
ILI7807E	Ilitek	FHD
ILI9885	Ilitek	FHD
NT35532	Novatek	FHD
NT35596	Novatek	FHD
NT35695	Novatek	FHD
R63417	SYNAPTICS	FHD

Table 58: Recommended Accelerometer & Gyroscope List

No.	Part Number	Vendor	Accelerometer	Gyroscope
1	BMA222E	Bosch	√	√
2	BMA250E	Bosch	√	√
3	BMA253	Bosch	√	√
4	BMA255	Bosch	√	√
5	BMA421	Bosch	√	
6	BMA422	Bosch	√	
7	BMA424	Bosch	√	
8	BMG160	Bosch		√
9	BMI120	Bosch	√	√
10	BMI160	Bosch	√	√
11	BMI260	Bosch	√	√
12	ICM-20600	InvenSense	√	√
13	ICM-20602	InvenSense	√	√
14	ICM-20607	InvenSense	√	√
15	ICM-20608-D	InvenSense	√	√
16	ICM-20608-G	InvenSense	√	√
17	ICM-20609	InvenSense	√	√
18	ICM-20621	InvenSense	√	√
19	ICM-20622	InvenSense	√	√
20	ICM-20690	InvenSense	√	√
21	ICM-40602	InvenSense	√	√

22	ICM-40604	InvenSense	√	√
23	ICM-40605	InvenSense	√	√
24	ICM-42602	InvenSense	√	√
25	ICM-42605	InvenSense	√	√
26	ICM-42605-M	InvenSense	√	√
27	ICM-42608	InvenSense	√	√
28	MPU-6500	InvenSense	√	√
29	MPU-6881	InvenSense	√	√
30	KX022-1020	Kionix	√	
31	KX023-1025	Kionix	√	
32	KX122-1037	Kionix	√	
33	KXTJ2-1009	Kionix	√	
34	KXTJ2-1029	Kionix	√	
35	KXTJ3	Kionix	√	
36	MC3413-P	mCube	√	
37	MC3416-P	mCube	√	
38	MXC4005XC	MEMSIC	√	
39	STK8BA53	Sensortek	√	
40	LIS2DH12TR	ST	√	
41	LIS2DS12TR	ST	√	
42	LIS2HH12	ST	√	
43	LIS3DH	ST	√	
44	LIS3DHTR	ST	√	
45	LSM6DS3TR	ST	√	√
46	LSM6DS3TR-C	ST	√	√
47	LSM6DSLTR	ST	√	√
48	LSM6DSMTR	ST	√	√

Table 59: Recommended E-Compass List

No.	Part Number	Vendor
1	AK09911C	AKM
2	AK09915C	AKM
3	AK09915D	AKM
4	AK09916C	AKM
5	AK09918C	AKM
6	HSCDTD008A	Alps
7	BMM150	Bosch
8	GMC306	Globalmems

9	IST8305	iSentek
10	IST8306	iSentek
11	IST8307	iSentek
12	IST8310	iSentek
13	MXG4300	MagnaChip
14	MMC3530	MEMSIC
15	MMC3630	MEMSIC
16	MMC3630KJ	MEMSIC
17	MMC5603NJ	MEMSIC
18	STM350MC	Senodia
19	STM480MW	Senodia
20	LIS2MDL	ST
21	AF6133	Voltafield
22	AF6133E	Voltafield
23	AF8133J	Voltafield
24	AF9133	Voltafield
25	YAS539	Yamaha

Table 60: Recommended Proximity&Ambient Light List

No.	Part Number	Vendor	Proximity	Ambient Light
1	TMD26203	ams	√	
2	CM36686	Capella	√	√
3	AP3426	Dyna Image	√	√
4	EPL2590KTWJP	Elan	√	√
5	MN66213	Elan	√	√
6	LTR-578ALS	Lite-On	√	√
7	BH1745NUC	ROHM		√
8	RPR-0521RS	ROHM	√	√
9	RPR-0531	ROHM	√	√
10	RPR-0531RS	ROHM	√	√
11	STK3321	Sensortek	√	√
12	PA12200001	TXC	√	√
13	PA22401001	TXC	√	
14	PA22A00001	TXC	√	√
15	TMD26203	ams	√	

9 Appendix

9.1 Related Documents

Table 61: Related Documents

No.	Document name	Remark
[1]	GSM 07.07：	Digital cellular telecommunications (Phase 2+); AT command set for GSM Mobile Equipment (ME)
[2]	GSM 07.10：	Support GSM 07.10 multiplexing protocol
[3]	GSM 07.05：	Digital cellular telecommunications (Phase 2+); Use of Data Terminal Equipment – Data Circuit terminating Equipment (DTE – DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)
[4]	GSM 11.14：	Digital cellular telecommunications system (Phase 2+); Specification of the SIM Application Toolkit for the Subscriber Identity Module – Mobile Equipment (SIM – ME) interface
[5]	GSM 11.11：	Digital cellular telecommunications system (Phase 2+); Specification of the Subscriber Identity Module – Mobile Equipment (SIM – ME) interface
[6]	GSM 03.38：	Digital cellular telecommunications system (Phase 2+); Alphabets and language-specific information
[7]	GSM 11.10	Digital cellular telecommunications system (Phase 2); Mobile Station (MS) conformance specification; Part 1: Conformance specification
[8]	3GPP TS 51.010-1	Digital cellular telecommunications system (Release 5); Mobile Station (MS) conformance specification
[9]	3GPP TS 34.124	Electromagnetic Compatibility (EMC) for mobile terminals and ancillary equipment.
[10]	3GPP TS 34.121	Electromagnetic Compatibility (EMC) for mobile terminals and ancillary equipment.
[11]	3GPP TS 34.123-1	Technical Specification Group Radio Access Network; Terminal conformance specification; Radio transmission and reception (FDD)
[12]	3GPP TS 34.123-3	User Equipment (UE) conformance specification; Part 3: Abstract Test Suites.
[13]	EN 301 908-02 V2.2.1	Electromagnetic compatibility and Radio spectrum Matters (ERM); Base Stations (BS) and User Equipment (UE) for IMT-2000. Third Generation cellular networks; Part 2: Harmonized EN for IMT-2000, CDMA Direct Spread (UTRA FDD) (UE) covering essential requirements of article 3.2 of the R&TTE Directive

[14]	EN 301 489-24 V1.2.1	Electromagnetic compatibility and Radio Spectrum Matters (ERM); Electromagnetic Compatibility (EMC) standard for radio equipment and services; Part 24: Specific conditions for IMT-2000 CDMA Direct Spread (UTRA) for Mobile and portable (UE) radio and ancillary equipment
[15]	IEC/EN60950-1(2001)	Safety of information technology equipment (2000)
[16]	GCF-CC V3.23.1	Global Certification Forum - Certification Criteria
[17]	2002/95/EC	Directive of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS)

9.2 Terms and Abbreviations

Table 62: Terms and abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-Rate
BOM	Bill of materials
bps	Bits per second
BT	Bluetooth
CDMA	Code division multiple access
CS	Coding Scheme
CSD	Circuit Switched Data
CSI	Camera serial interface
CTS	Clear to Send
DAC	Digital-to-analog converter
DDR	Double data rate
DSDA	Dual SIM dual active
DSDS	Dual SIM dual standby
DSP	Digital signal processor
DTE	Data Terminal Equipment (typically computer, terminal, printer)
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
ESD	Electrostatic Discharge

ESR	Effective series resistance
ETS	European Telecommunication Standard
EVDO	Evolution data optimized
FDD	Frequency division duplex
FR	Full Rate
GNSS	Global navigation satellite system
GPIO	General-purpose input/output
GPRS	General Packet Radio Service
GPU	Graphics processing unit
GSM	Global Standard for Mobile Communications
HR	Half Rate
HSPA	High-speed packet access
I2C	Inter-integrated circuit
IMEI	International Mobile Equipment Identity
ISP	Image signal processing
Kbps	kilobits per second
LCD	Liquid crystal display
LDO	Low dropout (linear regulator)
LPDDR	Low-power DDR
MIC	Microphone
MIPI	Mobile industry processor interface
PA	Power amplifier
PBCCH	Packet Broadcast Control Channel
PCB	Printed Circuit Board
PCL	Power Control Level
PCS	Personal Communication System, also referred to as GSM 1900
PDU	Protocol Data Unit
RF	Radio Frequency
PM	Power management
RoHS	Restriction of hazardous substances
PPP	Point-to-point protocol
PWM	Pulse-width modulator
RMS	Root Mean Square (value)
RTC	Real-time clock
RX	Receive Direction
SD	Secure digital

SDC	Secure digital controller
SIM	Subscriber Identification Module
SMS	Short Message Service
SMT	Surface mount technology
SPI	Serial peripheral interface
TDD	Time Division Distortion
TE	Terminal Equipment, also referred to as DTE
TX	Transmit Direction
UART	Universal Asynchronous Receiver & Transmitter
UIM	User identity module
URC	Unsolicited Result Code
USB	Universal serial bus
USSD	Unstructured Supplementary Service Data
WCDMA	Wideband code division multiple access
WCN	Wireless connectivity network
WLAN	Wireless local area network

9.3 Safety Caution

Table 63: Safety Caution

Marks	Requirements
	When in a hospital or other health care facility, observe the restrictions about the use of mobiles. Switch the cellular terminal or mobile off, medical equipment may be sensitive and not operate normally due to RF energy interference.
	Switch off the cellular terminal or mobile before boarding an aircraft. Make sure it is switched off. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. Forgetting to think much of these instructions may impact the flight safety, or offend local legal action, or both.
	Do not operate the cellular terminal or mobile in the presence of flammable gases or fumes. Switch off the cellular terminal when you are near petrol stations, fuel depots, chemical plants or where blasting operations are in progress. Operation of any electrical equipment in potentially explosive atmospheres can constitute a safety hazard.

	Your cellular terminal or mobile receives and transmits radio frequency energy while switched on. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	Road safety comes first! Do not use a hand-held cellular terminal or mobile when driving a vehicle, unless it is securely mounted in a holder for hands free operation. Before making a call with a hand-held terminal or mobile, park the vehicle.
	GSM cellular terminals or mobiles operate over radio frequency signals and cellular networks and cannot be guaranteed to connect in all conditions, especially with a mobile fee or an invalid SIM card. While you are in this condition and need emergent help, please remember to use emergency calls. In order to make or receive calls, the cellular terminal or mobile must be switched on and in a service area with adequate cellular signal strength. Some networks do not allow for emergency call if certain network services or phone features are in use (e.g. lock functions, fixed dialing etc.). You may have to deactivate those features before you can make an emergency call. Also, some networks require that a valid SIM card be properly inserted in the cellular terminal or mobile.