



SIM8950x

Hardware Design

Smart Module

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Contents

Version History	3
Contents	4
Table Index	6
Figure Index	8
1. Introduction	10
1.1 SIM8950x Key Features.....	12
1.2 SIM8950x Functional Diagram.....	15
2. Pin Definitions	16
2.1 Pin Assignment.....	16
2.2 Pin Description.....	17
3. Interface Application	30
3.1 Power Supply.....	30
3.1.1 Recommended power supply resolutions.....	30
3.1.2 Enhance power stability.....	31
3.2 Power On/off.....	32
3.2.1 Power on.....	32
3.2.2 Power-on sequence.....	33
3.2.3 Power off sequence.....	34
3.3 VRTC.....	34
3.4 Output Power Management.....	36
3.5 USB Type-C Interface.....	36
3.6 UART/SPI/I2C.....	38
3.7 Secure Digital Interface.....	39
3.8 LCD Interface.....	40
3.9 Touch Screen Interface.....	42
3.10 Camera Interface.....	43
3.11 Audio.....	46
3.11.1 Microphone.....	47
3.11.2 Headset.....	47
3.11.3 Earpiece.....	48
3.11.4 Speaker.....	49
3.11.5 LINEOUT.....	50
3.12 I2S Interface.....	50
3.13 UIM Interface.....	51
3.14 ADC.....	52
3.15 Antenna Interface.....	52
3.15.1 MAIN Antenna reference circuit.....	52
3.15.2 DRX Antenna reference circuit.....	53
3.15.3 GNSS Antenna reference circuit.....	54
3.15.4 WiFi/BT Antenna reference circuit.....	55
3.16 RF traces layout guidelines.....	55

3.17	Antenna Requirement.....	57
4.	PCB Layout.....	59
4.1	General Placement Guidelines.....	59
4.2	General Placement Guidelines.....	59
4.3	PCB Layout Guideline Details.....	59
4.3.1	RF Trace.....	59
4.3.2	Power/GND.....	60
4.3.3	UIM Card.....	60
4.3.4	MIPI_DSI/CSI.....	60
4.3.5	USB.....	60
4.3.6	SDC.....	61
4.3.7	Audio.....	61
5.	Electrical and Reliability.....	62
5.1	Absolute Maximum Ratings.....	62
5.2	Temperature Range.....	62
5.3	Operating Voltage.....	62
5.4	Digital-logic Characteristics.....	63
5.5	Current Consumption (VBAT=3.9V).....	63
5.6	Electro-Static Discharge.....	65
5.7	Module Operating Frequencies.....	65
5.8	Module Output power.....	67
5.9	Module Receiving Sensitivity.....	68
5.10	WIFI main RF Characteristics.....	69
5.11	BT Main RF Characteristics.....	70
5.12	GNSS Main RF Characteristics.....	70
6.	Manufacturing.....	71
6.1	Top and Bottom View of SIM8950x.....	71
6.2	Physical Dimensions.....	72
6.3	Recommended PCB footprint.....	73
6.4	Recommended SMT Stencil.....	74
6.5	Typical SMT Reflow Profile.....	76
6.6	Moisture Sensitivity Level (MSL).....	76
6.7	Baking Requirements.....	77
7.	Packaging.....	78
8.	Recommend Peripheral Component list.....	81
9.	Appendix.....	85
a)	Related Documents.....	85
b)	Terms and abbreviations.....	86
c)	Safety Caution.....	89

Table Index

TABLE 1: SIM8950X VARIANTS.....	10
TABLE 2: SIM8950X KEY FEATURES.....	12
TABLE 3: I/O PARAMETER DEFINITIONS.....	17
TABLE 4: PIN DESCRIPTION.....	17
TABLE 5: PIN CHARACTERS.....	23
TABLE 6: RECOMMENDED COMPONENTS.....	32
TABLE 7: PWRKEY CHARACTERISTICS.....	33
TABLE 8: VRTC CHARACTERISTIC.....	35
TABLE 9: OUTPUT POWER MANAGEMENT SUMMARY.....	36
TABLE 10: UART/SPI/I2C FUNCTIONAL ASSIGNMENTS.....	38
TABLE 11: SD INTERFACE PIN DEFINITIONS.....	39
TABLE 12: DISPLAY INTERFACE PIN DEFINITIONS.....	41
TABLE 13: TOUCH SCREEN INTERFACE PIN DEFINITIONS.....	42
TABLE 14: CAMERA INTERFACE PIN DEFINITIONS.....	43
TABLE 15: AUDIO INTERFACE PIN DEFINITIONS.....	46
TABLE 16: I2S INTERFACE PIN DEFINITIONS.....	50
TABLE 17: UIM INTERFACE PIN DEFINITIONS.....	51
TABLE 18: ADC PERFORMANCE PARAMETERS.....	52
TABLE 19: EXAMPLE OF IMPEDANCE CONTROL OF MICROSTRIP LINE STRUCTURE.....	56
TABLE 20: EXAMPLE OF IMPEDANCE CONTROL OF COPLANAR WAVEGUIDE STRUCTURE.....	56
TABLE 21: ANTENNA REQUIREMENT.....	57
TABLE 22: ABSOLUTE MAXIMUM RATINGS.....	62
TABLE 23: TEMPERATURE RANGE.....	62
TABLE 24: OPERATING VOLTAGE.....	62
TABLE 25: 1.8 V DIGITAL I/O CHARACTERISTICS.....	63
TABLE 26: CURRENT CONSUMPTION.....	63
TABLE 27: ESD PERFORMANCE PARAMETERS (TEMPERATURE: 25°C, HUMIDITY: 45%).....	65
TABLE 28: MODULE OPERATING FREQUENCIES.....	65
TABLE 29: CONDUCTED TRANSMISSION POWER.....	67
TABLE 30: CONDUCTED RECEIVING SENSITIVITY.....	68
TABLE 31: REFERENCE SENSITIVITY QPSK PREFSENS (LTE).....	68
TABLE 32: 2.4G WIFI MAIN RF CHARACTERISTICS.....	69
TABLE 33: 5G WIFI MAIN RF CHARACTERISTICS.....	70
TABLE 34: BT MAIN RF CHARACTERISTICS.....	70
TABLE 35: GNSS MAIN RF CHARACTERISTICS.....	70
TABLE 36: MSL RATINGS SUMMARY.....	76
TABLE 37: BAKING REQUIREMENTS.....	77
TABLE 38: MODULE TRAY INFORMATION.....	79
TABLE 39: SMALL CARTON INFORMATION.....	79
TABLE 40: BIG CARTON INFORMATION.....	80
TABLE 41: RECOMMENDED CAMERA SENSOR LIST.....	81
TABLE 42: RECOMMENDED LCD DRIVER IC LIST.....	82
TABLE 43: RECOMMENDED ACCELEROMETER & GYROSCOPE LIST.....	82
TABLE 44: RECOMMENDED E-COMPASS LIST.....	83

TABLE 45: RECOMMENDED PROXIMITY & AMBIENT LIGHT LIST.....	84
TABLE 46: RELATED DOCUMENTS.....	85
TABLE 47: TERMS AND ABBREVIATIONS.....	86
TABLE 48: SAFETY CAUTION.....	89

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Figure Index

FIGURE 1: SIM8950X FUNCTIONAL DIAGRAM.....	15
FIGURE 2: SIM8950X PIN ASSIGNMENT (TOP VIEW).....	16
FIGURE 3: LDO POWER SUPPLY REFERENCE CIRCUIT.....	30
FIGURE 4: DC-DC POWER SUPPLY REFERENCE CIRCUIT.....	31
FIGURE 5: VBAT INPUT REFERENCE CIRCUIT.....	31
FIGURE 6: POWERED ON/OFF MODULE USING BUTTON.....	32
FIGURE 7: POWERED ON/OFF MODULE USING TRANSISTOR.....	32
FIGURE 8: POWER-ON SEQUENCE.....	33
FIGURE 9: POWER-OFF SEQUENCE.....	34
FIGURE 10: KEEP-ALIVE CAPACITOR.....	35
FIGURE 11: NON-RECHARGEABLE BATTERY.....	35
FIGURE 12: RECHARGEABLE BATTERY.....	35
FIGURE 13: USB TYPE-C REFERENCE CIRCUIT.....	37
FIGURE 14: MICRO USB REFERENCE CIRCUIT.....	37
FIGURE 15: SD CARD REFERENCE CIRCUIT.....	40
FIGURE 16: DISPLAY REFERENCE CIRCUIT.....	42
FIGURE 17: PRIMARY CAMERA REFERENCE CIRCUIT.....	44
FIGURE 18: SECONDARY CAMERA REFERENCE CIRCUIT.....	44
FIGURE 19: DUAL CAMERA REFERENCE CIRCUIT.....	45
FIGURE 20: ECM-TYPE MICROPHONE REFERENCE CIRCUIT.....	47
FIGURE 21: MEMS-TYPE MICROPHONE REFERENCE CIRCUIT.....	47
FIGURE 22: HEADSET REFERENCE CIRCUIT.....	48
FIGURE 23: EARPIECE REFERENCE CIRCUIT.....	49
FIGURE 24: SPEAKER REFERENCE CIRCUIT.....	49
FIGURE 25: LINEOUT REFERENCE CIRCUIT.....	50
FIGURE 26: UIM CARD REFERENCE CIRCUIT.....	51
FIGURE 27: MAIN ANTENNA RECOMMENDED CIRCUIT.....	53
FIGURE 28: DRX ANTENNA RECOMMENDED CIRCUIT.....	53
FIGURE 29: GNSS ANTENNA RECOMMENDED CIRCUIT.....	54
FIGURE 30: GNSS ACTIVE ANTENNA CIRCUIT.....	54
FIGURE 31: WIFI/BT ANTENNA RECOMMENDED CIRCUIT.....	55
FIGURE 32: TWO LAYER PCB MICROSTRIP STRUCTURE.....	56
FIGURE 33: TWO LAYER PCB COPLANAR WAVEGUIDE STRUCTURE.....	56
FIGURE 34: FOUR LAYER PCB COPLANAR WAVEGUIDE STRUCTURE 1#.....	57
FIGURE 35: FOUR LAYER PCB COPLANAR WAVEGUIDE STRUCTURE 2#.....	57
FIGURE 36: TOP AND BOTTOM VIEW OF SIM8950X.....	71
FIGURE 37: OUTLINE DRAWING (UNIT: MM).....	72
FIGURE 38: RECOMMENDED PCB FOOTPRINT.....	73
FIGURE 39: OUTER PIN RECOMMENDED STENCIL.....	74
FIGURE 40: INNER FUNCTION PIN RECOMMENDED STENCIL.....	74
FIGURE 41: INNER GND PIN RECOMMENDED STENCIL.....	75
FIGURE 42: TYPICAL SMT REFLOW PROFILE.....	76
FIGURE 43: PACKAGING PROCESS.....	78

FIGURE 44: MODULE TRAY DRAWING.....	78
FIGURE 45: SMALL CARTON DRAWING.....	79
FIGURE 46: BIG CARTON DRAWING.....	79

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1. Introduction

This document describes electrical specifications, mechanical information, interfaces application and manufacturing information about SIM8950x module. With the help of this document and other application notes or user guide, users can understand SIM8950x well and develop various products quickly. almost any space requirement in users' applications, such as smart phone, PDA, industrial handheld, machine-to-machine and vehicle application, etc.

SIM8950x is a multi-mode and multi-band wireless smart module, which is based on Qualcomm SDM450 platform :

- 14nm FinFET ,64-bit ARM Cortex-A53 octa-core at 1.8GHz
- Non-PoP 2GB LPDDR3 SDRAM designed for 933Mhz clock.
- 16GB eMMC Flash
- Qualcomm Adreno 506 GPU at 600MHz, with 64-bit addressing
- Rich multimedia features: Support Dual-LCM, two cameras and multi-path analog audio IO
- Support for USB3.0 and SD3.0
- Global location-based service, wireless connectivity, and air interface standards including GSM, WCDMA, TD-SCDMA, CDMA2000, and LTE.

With higher integration to reduce PCB surface area, time-to-market, and BOM costs, SIM8950x will help drive wireless products adoption in more industry around the world.

The operating bands are different between SIM8950x variants, which are summarized in Table 1.

Table 1: SIM8950x Variants

Configuration		SIM8950LH	SIM8950A (AC)	SIM8950E (EC)	SIM8050LH
CPU		1.8GHz	1.8GHz	1.8GHz	1.8GHz
Memory	RAM (standard)	2GB	2GB	2GB	2GB
	ROM (standard)	16GB	16GB	16GB	16GB
Standards & bands					
GSM	GSM850		✓	✓	
	EGSM900	✓	✓	✓	
	DCS1800	✓		✓	

	PCS1900		✓		
WCDMA	B1	✓	✓	✓	
	B2		✓		
	B4		✓		
	B5		✓	✓	
	B8	✓	✓	✓	
CDMA2000 1X/EVDO	BC0	✓			
TDSCDMA	B34	✓			
	B39	✓			
FDD-LTE	B1	✓		✓	
	B2		✓		
	B3	✓		✓	
	B4		✓		
	B5	✓	✓	✓	
	B7		✓	✓	
	B8	✓		✓	
	B12		✓		
	B13		✓		
	B17		✓		
	B20			✓	
	B25			✓	
	B26			✓	
TDD-LTE	B34	✓			
	B38	✓		✓	
	B39	✓			
	B40	✓		✓	
	B41	✓	✓	✓	
WLAN	2.4G/5GHz; 802.11a/b/g/n/ac	✓	✓	✓	✓
BT	BT4.2 LE	✓	✓	✓	✓
GNSS	GPS	✓	✓	✓	
	GLONASS	✓	✓	✓	
	BEIDOU	✓	✓	✓	

1.1 SIM8950x Key Features

Table 2: SIM8950x key features

Feature	Implementation
Application processor	Octa ARM Cortex-A53 cores up to 1.8 GHz 64-bit processor
Memory	2GB LPDDR3 RAM up to 933Mhz 16GB eMMC NAND flash (MLC) Customization: 3GB LPDDR3 + 32GB eMMC 4GB LPDDR3 + 64GB eMMC
External memory via SDC2	SD3.0; Support SD flash devices up to 128GB
GPU	Qualcomm Adreno 506 GPU, 64bit addressing, designed for 600MHz
Operating system	Android OS 7.x/8.x/9.x
Power supply	3.4V ~4.4V
Charge management	External charging IC needed Provide Qualcomm PMI8952 interface for QC 3.0
Display	Dual MIPI DSI four-lane FHD (1920 × 1200) 60 fps; 16/18/24 bpp RGB
Camera	Primary camera: 4-lane MIPI_CSI, 21MP Secondary camera: 2-lane MIPI_CSI, 8MP
Video performance	Encode: 1080p60, H.264, H.265, and VP8 Decode: 1080p60, H.264, H.265, VP8, and VP9
Audio	One digital port I2S, support both master and slave mode Three analog input ports: MIC1 supports differential configuration MIC2 supports single-ended configuration MIC3 supports single-ended configuration Supports dual-mic noise suppression 16, 32, and 48 KHz sample rate Four analog output ports: earpiece, stereo headphones, class-D speaker driver ,and line out 16, 32, 48, 96 and 192 KHz sample rate Audio codec support: G711; QCELP; EVRC, EVRC-B, EVRC-WB; AMR-NB, AMR-WB; GSM-EFR, GSM-FR, GSM-HR
USB	One USB 3.0/2.0 Support Type-C Support OTG (external 5V power supply is needed)

UART	<p>4*UART: UART2、UART4、UART5 & UART6</p> <ul style="list-style-type: none"> ● UART2 for debug, 2-line ● UART4、UART5 & UART6 are 4-line that support RTS and CTS hardware flow control, the speed can up to 4Mbps.
I2C	8* I2C
SPI	5* SPI
ADC	<p>1*ADC (16bit)</p> <p>Detection range: 0.1V~1.7V or 0.3V~4.5V (software controlled)</p>
UIM card	Dual cards dual standby
Transmitting power	<p>Class 4 (33dBm±2dB) for EGSM850</p> <p>Class 4 (33dBm±2dB) for EGSM900</p> <p>Class 1 (30dBm±2dB) for DCS1800</p> <p>Class 1 (30dBm±2dB) for PCS1900</p> <p>Class E2 (27dBm±3dB) for EGSM850 8-PSK</p> <p>Class E2 (27dBm±3dB) for EGSM900 8-PSK</p> <p>Class E2 (26dBm±3dB) for DCS1800 8-PSK</p> <p>Class E2 (26dBm±3dB) for PCS1900 8-PSK</p> <p>Class 3 (24dBm+1/-3dB) for WCDMA bands</p> <p>Class 3 (24dBm+3/-1dB) for CDMA BC0</p> <p>Class 2 (24dBm+1/-3dB) for TD-SCDMA bands</p> <p>Class 3 (23dBm±2dB) for LTE-FDD bands</p> <p>Class 3 (23dBm±2dB) for LTE-TDD bands</p>
LTE features	<p>Support 3GPP R8 Cat.4</p> <p>Support 1.4 ~ 20MHz RF bandwidth</p> <p>Support MIMO in DL direction</p> <p>Cat.4 FDD: Max 150Mbps (DL)/Max 50Mbps (UL)</p> <p>Cat.4 TDD: Max 130Mbps (DL)/Max 35Mbps (UL)</p>
UMTS features	<p>Support 3GPP R8 DC-HSDPA/ HSPA+/HSDPA/HSUPA/WCDMA</p> <p>Support QPSK, 16-QAM and 64-QAM modulation</p> <p>DC-HSDPA: Max 42Mbps (DL)</p> <p>DC-HSUPA: Max 11.2Mbps (UL)</p> <p>WCDMA: Max 384Kbps (DL)/Max 384Kbps (UL)</p>
TD-SCDMA features	<p>Support CCSA Release 3 TD-SCDMA</p> <p>Max 4.2Mbps (DL)/Max 2.2Mbps (UL)</p>
CDMA2000 features	<p>Support 3GPP2 CDMA2000 1X Advanced, CDMA2000 1x EV-DO Rev.A</p> <p>EVDO: Max 3.1Mbps (DL)/Max 1.8 Mbps (UL)</p> <p>1X Advanced: Max 307.2Kbps (DL)/Max 307.2Kbps (UL)</p>
GSM features	<p>R99:</p> <p>CSD: 9.6kbps, 14.4kbps</p> <p>GPRS:</p> <p>Support GPRS multi-slot class 33 (default)</p> <p>Coding scheme: CS-1, CS-2, CS-3 and CS-4</p> <p>Max 85.6Kbps (UL), 107Kbps (DL)</p> <p>EDGE:</p> <p>Support EDGE multi-slot class 33 (default)</p> <p>Support GMSK and 8-PSK for different MCS</p>

	Downlink coding schemes: CS 1-4 and MCS 1-9 Uplink coding schemes: CS 1-4 and MCS 1-9 Max 236.8Kbps (UL), 296Kbps (DL)
WLAN features	2.4G/5GHz, 802.11a/b/g/n/ac, up to 433Mbps Support AP mode
Bluetooth features	BT2.1+EDR /3.0 /4.2 BLE
GNSS	GPS/GLONASS/BEIDOU
Temperature range	Operating temperature: $-35^{\circ}\text{C} \sim +75^{\circ}\text{C}$ [1] Extreme operating temperature: $-40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ [2] Storage temperature: $-40^{\circ}\text{C} \sim +90^{\circ}\text{C}$
Physical features	Dimension: $44.1(\pm 0.2) \times 45.6(\pm 0.2) \times 2.8(\pm 0.2)\text{mm}$ Weight: about 12.5g

NOTE

1. Module can operate in the $-35^{\circ}\text{C} \sim +75^{\circ}\text{C}$ range, and the performance can be meet the 3GPP specifications.
2. Module is working when the temperature change to $-40^{\circ}\text{C} \sim +85^{\circ}\text{C}$, Module is able to make and receive voice calls, data calls, SMS and make GPRS/UMTS/HSPA+/LTE traffic. The performance will be reduced slightly from the 3GPP specifications if the temperature is outside the normal operating temperature range and still within the extreme operating temperature range.

1.2 SIM8950x Functional Diagram

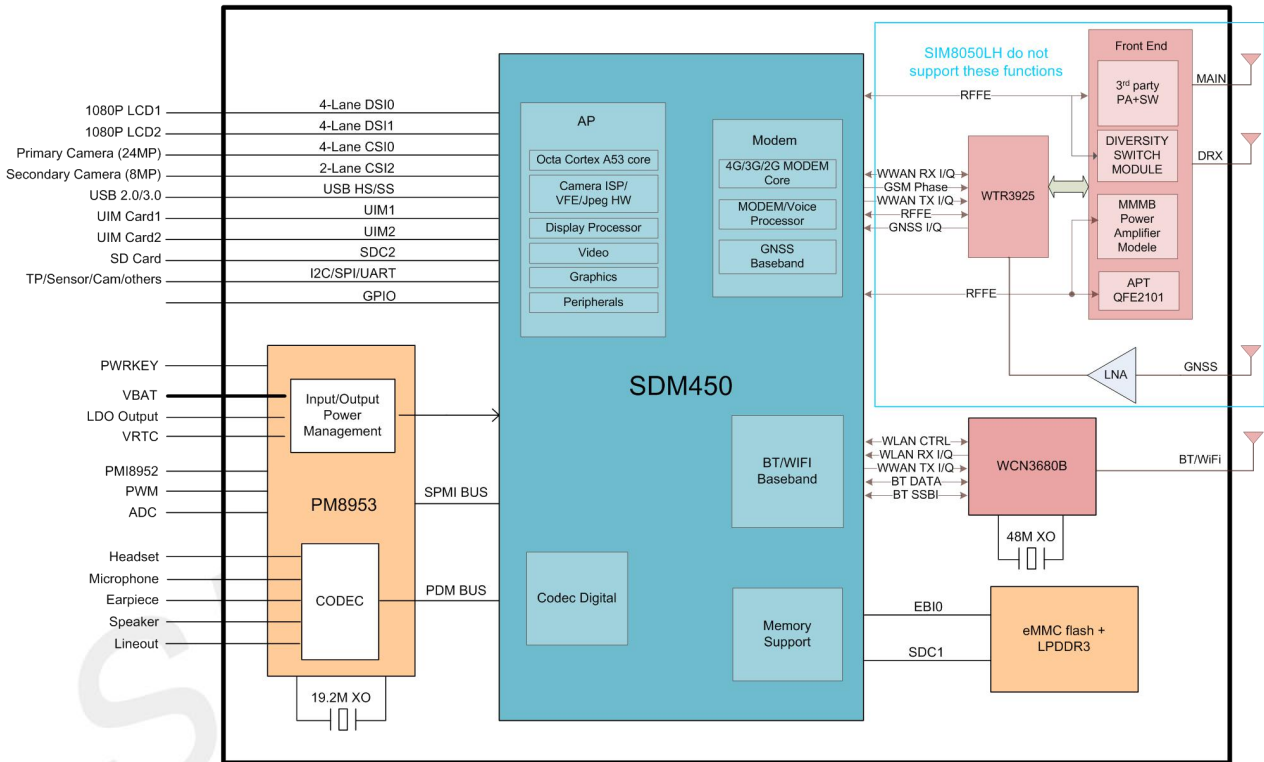


Figure 1: SIM8950x functional diagram

2. Pin Definitions

2.1 Pin Assignment

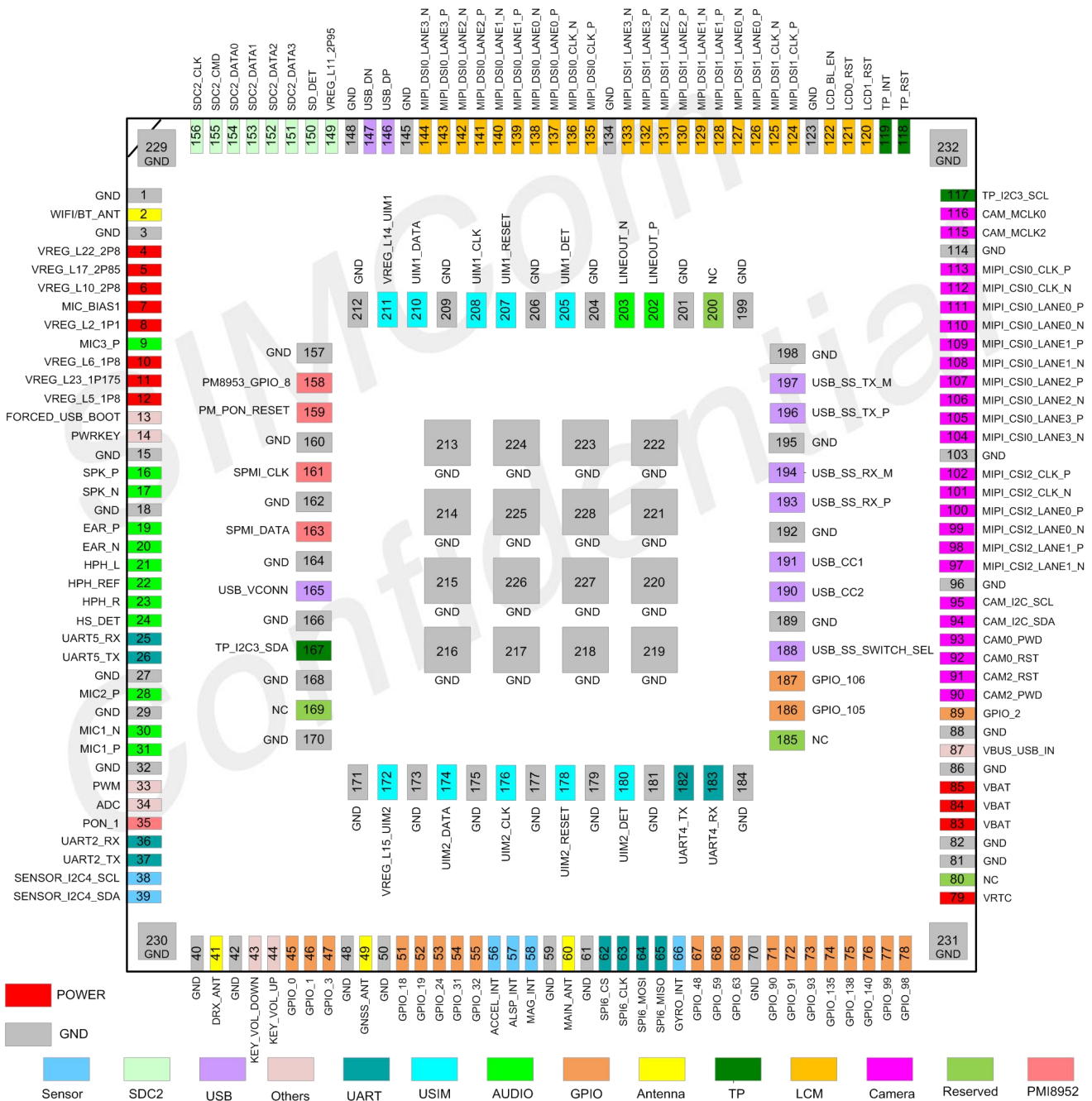


Figure 2: SIM8950x pin assignment (top view)

2.2 Pin Description

Table 3: I/O parameter definitions

Symbol	Description
Pad attribute	
PI	Power input
PO	Power input
AI	Analog input
AO	Analog output
DI	Digital input
DO	Digital output
Pad pull details for digital I/Os	
NP	No internal pull
PU	Internal pull up
PD	Internal pull down

Table 4: Pin description

Pin Name	Pin No.	I/O	Description	Note
Power Supply				
VBAT	83, 84, 85	PI	Main power supply for the module	
VRTC	79	PI/PO	Coin cell or backup-battery charger supply and input	
VREG_L22_2P8	4	PO	LDO 22 output for camera AVDD	
VREG_L17_2P85	5	PO	LDO 17 output for display and camera VCM	
VREG_L10_2P8	6	PO	LDO 10 output for Sensors and touch screen	
VREG_L2_1P1	8	PO	LDO 2 output for camera DVDD	
VREG_L6_1P8	10	PO	LDO 6 output , could be turned off in sleep mode	
VREG_L23_1P175	11	PO	LDO 23 output for camera DVDD	
VREG_L5_1P8	12	PO	LDO 5 output, should not be changed and turned off	
Ground				

GND	1 3 15 18 27 29 32 40	Ground
	42 48 50 59 61 70 81	
	82 86 88 96 103 114	
	123 134 145 148 157	
	160 162 164 166 168	
	170 171 173 175 177	
	179 181 184 189 192	
	195 198 199 201 204	
	206 209 212 213 214	
	215 216 217 218 219	
	220 221 222 223 224	
	225 226 227 228 229	
	230 231 232	

USB TYPE-C

VBUS_USB_IN	87	AI	VBUS monitor signal from Type-C connector
USB_DN	147	AI/AO	USB high-speed data
USB_DP	146	AI/AO	
USB_VCONN	165	AI	Power input pin (5 V, 210 mA from VBUS) to drive active cables during the DFP mode.
USB_SS_SWITCH_SEL	188	DO	USB Type-C switch control, cannot be pull up externally
USB_CC2	190	AI/AO	USB Type-C connector configuration channel 1
USB_CC1	191	AI/AO	USB Type-C connector configuration channel 2
USB_SS_RX_P	193	AI	USB super-speed receive – plus
USB_SS_RX_M	194	AI	USB super-speed receive –minus
USB_SS_TX_P	196	AO	USB super-speed transmit – plus
USB_SS_TX_M	197	AO	USB super-speed transmit – minus

UIM Interface

VREG_L15_UIM2	172	PO	LDO 15 output for UIM2, 1.8V/2.95V	
UIM2_DATA	174	DI/DO	UIM2 data	Cannot be used as GPIO
UIM2_CLK	176	DO	UIM2 clock	
UIM2_RESET	178	DO	UIM2 reset	
UIM2_DET	180	DI	UIM2 presence detection	
UIM1_DET	205	DI	UIM1 presence detection	
UIM1_RESET	207	DO	UIM1 reset	Cannot be used as GPIO
UIM1_CLK	208	DO	UIM1 clock	
UIM1_DATA	210	DI/DO	UIM1 data	
VREG_L14_UIM1	211	PO	LDO 14 output for UIM1, 1.8V/2.95V	

SDC Interface

VREG_L11_2P95	149	PO	LDO 11 output for SD card
SDC2_CLK	156	DO	Secure digital controller 2 clock
SDC2_CMD	155	DI/DO	Secure digital controller 2 command
SDC2_DATA0	154	DID/O	Secure digital controller 2 data bit 0
SDC2_DATA1	153	DI/DO	Secure digital controller 2 data bit 1
SDC2_DATA2	152	DI/DO	Secure digital controller 2 data bit 2
SDC2_DATA3	151	DI/DO	Secure digital controller 2 data bit 3
SD_DET	150	DI	Secure digital card detection
Touch Screen			
TS_I2C3_SDA	167	DI/DO	Touch screen I2C data
TS_I2C3_SCL	117	DO	Touch screen I2C clock
TS_INT	119	DI	Touch screen interrupt
TS_RST	118	DO	Touch screen reset
LCD Interface			
MIPI_DSI0_CLK_P	135	AO	
MIPI_DSI0_CLK_N	136	AO	
MIPI_DSI0_LANE0_P	137	AI/AO	
MIPI_DSI0_LANE0_N	138	AI/AO	
MIPI_DSI0_LANE1_P	139	AI/AO	
MIPI_DSI0_LANE1_N	140	AI/AO	Primary display serial interface 0
MIPI_DSI0_LANE2_P	141	AI/AO	
MIPI_DSI0_LANE2_N	142	AI/AO	
MIPI_DSI0_LANE3_P	143	AI/AO	
MIPI_DSI0_LANE3_N	144	AI/AO	
MIPI_DSI1_CLK_P	124	AO	
MIPI_DSI1_CLK_N	125	AO	
MIPI_DSI1_LANE0_P	126	AI/AO	
MIPI_DSI1_LANE0_N	127	AI/AO	
MIPI_DSI1_LANE1_P	128	AI/AO	
MIPI_DSI1_LANE1_N	129	AI/AO	Secondary display serial interface 1
MIPI_DSI1_LANE2_P	130	AI/AO	
MIPI_DSI1_LANE2_N	131	AI/AO	
MIPI_DSI1_LANE3_P	132	AI/AO	
MIPI_DSI1_LANE3_N	133	AI/AO	

LCD1_RST	120	DO	LCD1 reset
LCD0_RST	121	DO	LCD0 reset
LCD_BL_EN	122	DO	LCD back light enable
PWM	33	DO	PWM control for external WLED driver
Camera Interface			
MIPI_CSI0_LANE3_N	104	AI/AO	
MIPI_CSI0_LANE3_P	105	AI/AO	
MIPI_CSI0_LANE2_N	106	AI/AO	
MIPI_CSI0_LANE2_P	107	AI/AO	
MIPI_CSI0_LANE1_N	108	AI/AO	Primary camera serial interface 0
MIPI_CSI0_LANE1_P	109	AI/AO	
MIPI_CSI0_LANE0_N	110	AI/AO	
MIPI_CSI0_LANE0_P	111	AI/AO	
MIPI_CSI0_CLK_N	112	AI	
MIPI_CSI0_CLK_P	113	AI	
MIPI_CSI2_LANE1_N	97	AI/AO	
MIPI_CSI2_LANE1_P	98	AI/AO	
MIPI_CSI2_LANE0_N	99	AI/AO	Secondary camera serial interface 2
MIPI_CSI2_LANE0_P	100	AI/AO	
MIPI_CSI2_CLK_N	101	AI	
MIPI_CSI2_CLK_P	102	AI	
CAM2_PWD	90	DO	Secondary Camera power down, cannot be pull up externally
CAM2_RST	91	DO	Secondary Camera reset
CAM0_RST	92	DO	Primary Camera reset
CAM0_PWD	93	DO	Primary Camera power down
CAM_I2C_SDA	94	DI/DO	Dedicated Camera I2C data
CAM_I2C_SCL	95	DO	Dedicated Camera I2C clock
CAM_MCLK2	115	DO	Secondary Camera master clock
CAM_MCLK0	116	DO	Primary Camera master clock
Keypad			
KEY_VOL_UP	44	DI	Volume up keypad
KEY_VOL_DOWN	43	DI	Volume down keypad
PWRKEY	14	DI	Power on keypad
Sensors			
SENSOR_I2C4_SCL	38	DO	Sensors I2C clock

SENSOR_I2C4_SDA	39	DI/DO	Sensors I2C data
ACCEL_INT	56	DI	Accelerate sensor interrupt
ALSP_INT	57	DI	Ambient light and proximity sensor interrupt
MAG_INT	58	DI	Magnetic sensor interrupt
GYRO_INT	66	DI	Gyroscope sensor interrupt
Audio			
SPK_P	16	AO	Speaker driver output, positive
SPK_N	17	AO	Speaker driver output, negative
EAR_P	19	AO	Earpiece output, positive
EAR_N	20	AO	Earpiece output, negative
HPH_L	21	AO	Headphone output, left channel
HPH_REF	22	AI	Headphone ground reference
HPH_R	23	AO	Headphone output, right channel
HS_DET	24	AI	Headset detection
MIC2_P	28	AI	Microphone input 2, positive
MIC1_N	30	AI	Microphone input 1, negative
MIC1_P	31	AI	Microphone input 1, positive
MIC3_P	9	AI	Microphone input 3, positive
MIC_BIAS1	7	PO	Microphone bias1
LINEOUT_P	202	AO	LINEOUT output, positive
LINEOUT_N	203	AO	LINEOUT output, negative
Antenna			
MAIN_ANT	60	AI/AO	2G/3G/4G main antenna port
DRX_ANT	41	AI	4G diversity antenna port
GNSS_ANT	49	AI	GNSS antenna port
WIFI/BT_ANT	2	AI/AO	WIFI/BT antenna port
UART			
UART2_RX	36	DI	UART2 data receive for debug
UART2_TX	37	DO	UART2 data transmit for debug
UART4_TX	182	DO	UART4 data transmit
UART4_RX	183	DI	UART4 data receive
UART5_RX	25	DI	UART5 data receive
UART5_TX	26	DO	UART5 data transmit
SPI			
SPI6_CS	62	DO	SPI6 chip select
SPI6_CLK	63	DO	SPI6 clock
SPI6_MOSI	64	DO	SPI6 master out slave in
SPI6_MISO	65	DI	SPI6 master in slave out
GPIO			
GPIO_0	45	DI/DO	GPIO

GPIO_1	46	DI/DO	GPIO
GPIO_2	89	DI/DO	GPIO
GPIO_3	47	DI/DO	GPIO
GPIO_18	51	DI/DO	GPIO
GPIO_19	52	DI/DO	GPIO
GPIO_24	53	DI/DO	GPIO
GPIO_31	54	DI/DO	GPIO
GPIO_32	55	DI/DO	GPIO
GPIO_48	67	DI/DO	GPIO
GPIO_59	68	DI/DO	GPIO
GPIO_63	69	DI/DO	GPIO
GPIO_90	71	DI/DO	GPIO
GPIO_91	72	DI/DO	GPIO
GPIO_93	73	DI/DO	GPIO
GPIO_99	77	DI/DO	GPIO
GPIO_98	78	DI/DO	GPIO
GPIO_105	186	DI/DO	GPIO, cannot be pull up externally
GPIO_106	187	DI/DO	GPIO, cannot be pull up externally
GPIO_135	74	DI/DO	GPIO
GPIO_138	75	DI/DO	GPIO
GPIO_140	76	DI/DO	GPIO
Others			
FORCED_USB_BOOT	13	DI	Force boot from USB interface
ADC	34	AI	ADC
PMI8952 Interface			
PON_1	35	DI	LOW to HIGH from PMI8952 initiates power on
PM8953_GPIO8	158	DO	Disables and enables external regulator source for VCONN and also serves as the USB_ID pin control for PMI8952
PM_PON_RESET	159	DO	Power-on reset control for PMI8952
SPMI_CLK	161	DO	SPMI clock for PMI8952
SPMI_DATA	163	DI/DO	SPMI data for PMI8952
NC			
NC	80,169, 185, 200		Do not connect

NOTE

1. Leave unused pins floating unless otherwise specified.
2. For SIM8050LH, MAIN_ANT /DRX_ANT /GNSS_ANT are NC pins.

For more information about SIM8950x pin characters, refer to the following table.

Table 5: Pin Characters

Pin#	Pin Name	Voltage	SDM450 Platform Pin Name	Reset Status	Wakeup Interrupt	Note
1	GND					
2	WIFI/BT_ANT					
3	GND					
4	VREG_L22_2P8	2.8V				
5	VREG_L17_2P85	2.85V				
6	VREG_L10_2P8	2.8V				
7	MIC_BIAS1	1.6~2.85V				
8	VREG_L2_1P1	1.1V				
9	MIC3_P					
10	VREG_L6_1P8	1.8V				
11	VREG_L23_1P175	1.15V				
12	VREG_L5_1P8	1.8V				
13	FORCED_USB_BOOT	1.8V	GPIO_37	I-PD	√	
14	PWRKEY	1.8V				
15	GND					
16	SPK_P					
17	SPK_N					
18	GND					
19	EAR_P					
20	EAR_N					
21	HPH_L					
22	HPH_REF					
23	HPH_R					
24	HS_DET					
25	UART5_RX	1.8V	GPIO_17	I-PD	√	
26	UART5_TX	1.8V	GPIO_16	I-PD		
27	GND					

28	MIC2_P				
29	GND				
30	MIC1_N				
31	MIC1_P				
32	GND				
33	PWM				
34	ADC				
35	PON_1	1.8V			
36	UART2_RX	1.8V	GPIO_5	I-PD	√
37	UART2_TX	1.8V	GPIO_4	I-PD	
38	SENSOR_I2C4_SCL	1.8V	GPIO_15	I-PD	
39	SENSOR_I2C4_SDA	1.8V	GPIO_14	I-PD	
40	GND				
41	DRX_ANT				
42	GND				
43	KEY_VOL_DOWN	1.8V			
44	KEY_VOL_UP	1.8V	GPIO_85	I-PD	√
45	GPIO_0	1.8V	GPIO_0	I-PD	
46	GPIO_1	1.8V	GPIO_1	I-PD	√
47	GPIO_3	1.8V	GPIO_3	I-PD	
48	GND				
49	GNSS_ANT				
50	GND				
51	GPIO_18	1.8V	GPIO_18	I-PD	
52	GPIO_19	1.8V	GPIO_19	I-PD	
53	GPIO_24	1.8V	GPIO_24	I-PD	
54	GPIO_31	1.8V	GPIO_31	I-PD	√
55	GPIO_32	1.8V	GPIO_32	I-PD	
56	ACCEL_INT	1.8V	GPIO_42	I-PD	√
57	ALSP_INT	1.8V	GPIO_43	I-PD	√
58	MAG_INT	1.8V	GPIO_44	I-PD	√
59	GND				
60	MAIN_ANT				
61	GND				
62	SPI6_CS	1.8V	GPIO_22	I-PD	
63	SPI6_CLK	1.8V	GPIO_23	I-PD	
64	SPI6_MOSI	1.8V	GPIO_20	I-PD	
65	SPI6_MISO	1.8V	GPIO_21	I-PD	√
66	GYRO_INT	1.8V	GPIO_45	I-PD	√
67	GPIO_48	1.8V	GPIO_48	I-PD	√
68	GPIO_59	1.8V	GPIO_59	I-PD	√

69	GPIO_63	1.8V	GPIO_63	I-PD	√	
70	GND					
71	GPIO_90	1.8V	GPIO_90	I-PD	√	
72	GPIO_91	1.8V	GPIO_91	I-PD	√	
73	GPIO_93	1.8V	GPIO_93	I-PD	√	
74	GPIO_135	1.8V	GPIO_135	I-PD		
75	GPIO_138	1.8V	GPIO_138	I-PD	√	
76	GPIO_140	1.8V	GPIO_140	I-PD	√	
77	GPIO_99	1.8V	GPIO_99	I-PD		
78	GPIO_98	1.8V	GPIO_98	I-PD		
79	VRTC	3V				
80	NC					
81	GND					
82	GND					
83	VBAT	3.4~4.4V				
84	VBAT	3.4~4.4V				
85	VBAT	3.4~4.4V				
86	GND					
87	VBUS_USB_IN	5V				
88	GND					
89	GPIO_2	1.8V	GPIO_2	I-PD		
90	CAM2_PWD	1.8V	GPIO_130	I-PD	√	Cannot be pull up externally
91	CAM2_RST	1.8V	GPIO_129	I-PD	√	
92	CAM0_RST	1.8V	GPIO_40	I-PD		
93	CAM0_PWD	1.8V	GPIO_39	I-PD		
94	CAM_I2C_SDA	1.8V	GPIO_29	I-PD		
95	CAM_I2C_SCL	1.8V	GPIO_30	I-PD		
96	GND					
97	MIPI_CSI2_LANE1_N					
98	MIPI_CSI2_LANE1_P					
99	MIPI_CSI2_LANE0_N					
100	MIPI_CSI2_LANE0_P					
101	MIPI_CSI2_CLK_N					
102	MIPI_CSI2_CLK_P					
103	GND					
104	MIPI_CSI0_LANE3_N					
105	MIPI_CSI0_LANE3_P					

106	MIPI_CSI0_LANE2_N				
107	MIPI_CSI0_LANE2_P				
108	MIPI_CSI0_LANE1_N				
109	MIPI_CSI0_LANE1_P				
110	MIPI_CSI0_LANE0_N				
111	MIPI_CSI0_LANE0_P				
112	MIPI_CSI0_CLK_N				
113	MIPI_CSI0_CLK_P				
114	GND				
115	CAM_MCLK2	1.8V	GPIO_27	I-PD	
116	CAM_MCLK0	1.8V	GPIO_26	I-PD	
117	TP_I2C3_SCL	1.8V	GPIO_11	I-PD	
118	TP_RST	1.8V	GPIO_64	I-PD	
119	TP_INT	1.8V	GPIO_65	I-PD	√
120	LCD1_RST	1.8V	GPIO_136	I-PD	
121	LCD0_RST	1.8V	GPIO_61	I-PD	√
122	LCD_BL_EN	1.8V	GPIO_137	I-PD	√
123	GND				
124	MIPI_DSI1_CLK_P				
125	MIPI_DSI1_CLK_N				
126	MIPI_DSI1_LANE0_P				
127	MIPI_DSI1_LANE0_N				
128	MIPI_DSI1_LANE1_P				
129	MIPI_DSI1_LANE1_N				
130	MIPI_DSI1_LANE2_P				
131	MIPI_DSI1_LANE2_N				
132	MIPI_DSI1_LANE3_P				
133	MIPI_DSI1_LANE3_N				
134	GND				
135	MIPI_DSI0_CLK_P				
136	MIPI_DSI0_CLK_N				
137	MIPI_DSI0_LANE0_P				
138	MIPI_DSI0_LANE0_N				

139	MIPI_DSI0_LANE1_P				
140	MIPI_DSI0_LANE1_N				
141	MIPI_DSI0_LANE2_P				
142	MIPI_DSI0_LANE2_N				
143	MIPI_DSI0_LANE3_P				
144	MIPI_DSI0_LANE3_N				
145	GND				
146	USB_DP				
147	USB_DN				
148	GND				
149	VREG_L11_2P95	2.95V			
150	SD_DET_N	1.8V	GPIO_133	I-PD	√
151	SDC2_DATA3	1.8/2.95		BH-P	√
152	SDC2_DATA2	1.8/2.95 V		BH-P D	
153	SDC2_DATA1	1.8/2.95 V		BH-P D	√
154	SDC2_DATA0	1.8/2.95 V		BH-P D	
155	SDC2_CMD	1.8/2.95 V		BH-P D	
156	SDC2_CLK	1.8/2.95 V		BHNP	
157	GND				
158	PM8953_GPIO8	1.8V			
159	PM_PON_RESET	1.8V			
160	GND				
161	SPMI_CLK				
162	GND				
163	SPMI_DATA				
164	GND				
165	USB_VCONN				
166	GND				
167	TP_I2C3_SDA	1.8V	GPIO_10	I-PD	
168	GND				
169	NC				
170	GND				
171	GND				
172	VREG_L15_UIM2	1.8/2.95 V			
173	GND				

174	UIM2_DATA	1.8/2.95 V	GPIO_55	I-PD		
175	GND					Cannot be used as GPIO
176	UIM2_CLK	1.8/2.95 V	GPIO_56	I-PD		
177	GND					
178	UIM2_RESET	1.8/2.95 V	GPIO_57	I-PD		
179	GND					
180	UIM2_DET	1.8V	GPIO_58	I-PD		
181	GND					
182	UART4_TX	1.8V	GPIO_12	I-PD	√	
183	UART4_RX	1.8V	GPIO_13	I-PD	√	
184	GND					
185	NC					
186	GPIO_105	1.8V	GPIO_105	I-PD		cannot be pull up externally
187	GPIO_106	1.8V	GPIO_106	I-PD		cannot be pull up externally
188	USB_SS_SWITCH_SELECT	1.8V	GPIO_139	I-PD	√	cannot be pull up externally
189	GND					
190	USB_CC2					
191	USB_CC1					
192	GND					
193	USB1_SS_RX_P					
194	USB1_SS_RX_M					
195	GND					
196	USB1_SS_TX_P					
197	USB1_SS_TX_M					
198	GND					
199	GND					
200	NC					
201	GND					
202	LINEOUT_P					
203	LINEOUT_N					
204	GND					
205	UIM1_DET	1.8V	GPIO_54	I-PD	√	
206	GND					
207	UIM1_RESET	1.8 / 2.95 V	GPIO_53	I-PD		Cannot be used as GPIO
208	UIM1_CLK	1.8 / 2.95 V	GPIO_52	I-PD		
209	GND					

210	UIM1_DATA	1.8 / 2.95 V	GPIO_51	I-PD
211	VREG_L14_UIM1	1.8 / 2.95 V		
212	GND			
213	GND			
214	GND			
215	GND			
216	GND			
217	GND			
218	GND			
219	GND			
220	GND			
221	GND			
222	GND			
223	GND			
224	GND			
225	GND			
226	GND			
227	GND			
228	GND			
229	GND			
230	GND			
231	GND			
232	GND			

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3. Interface Application

3.1 Power Supply

The power supply of SIM8950x ranges from 3.4V to 4.4V, and 3.9V is recommended. It must be able to provide sufficient current up to 3A for the high-power transmitting.

3.1.1 Recommended power supply resolutions

For battery-powered applications, the external charging IC is needed.

For non-battery applications, if the DC input voltage is +5V and users do not care about the power efficiency, a high-current low-dropout regulator is recommended.

The reference design is shown in Figure 3.

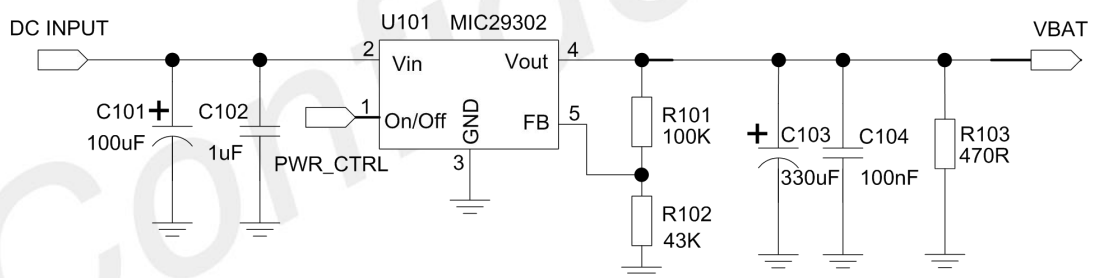


Figure 3: LDO power supply reference circuit

NOTE

To ensure a proper behavior of the regulator under light load, an extra minimum load (R103 in Figure 3) is required, because the current SIM8950x consumed is very small in sleep mode and power off mode. For more details about minimum load, please refer to specification of MIC29302.

To increase power efficiency, the switching mode DC-DC converter is preferable, especially when DC input voltage is quite high. The reference design is shown in Figure 4, and it is recommended to reserve a proper ferrite bead (FB101 in Figure 4) in series for EMI suppression.

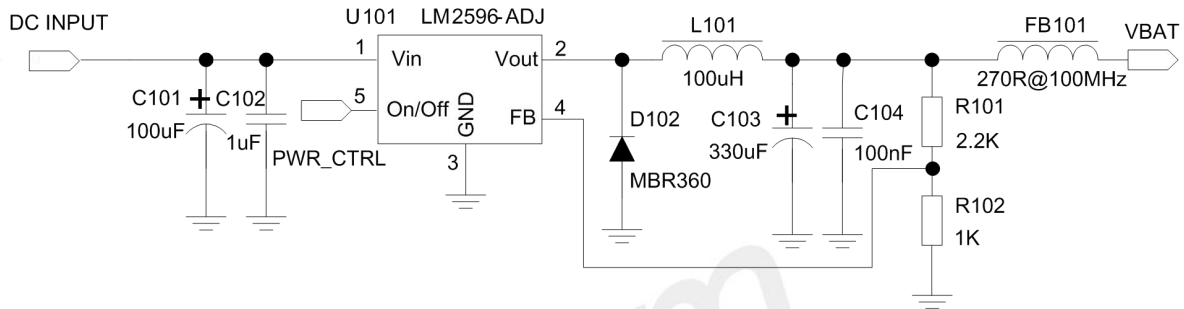


Figure 4: DC-DC power supply reference circuit

3.1.2 Enhance power stability

To enhance power stability, it is recommended to add some bypass capacitors and zener diode closed to VBAT pins. The reference design is shown in Figure 5, where C101 and C102 are two 110uF tantalum capacitors with low ESR, C103 could be a 1~10uF ceramic capacitor, 33pF and 10pF capacitors are used for eliminating the high frequency interference, D101 can protect the module against voltage surge.

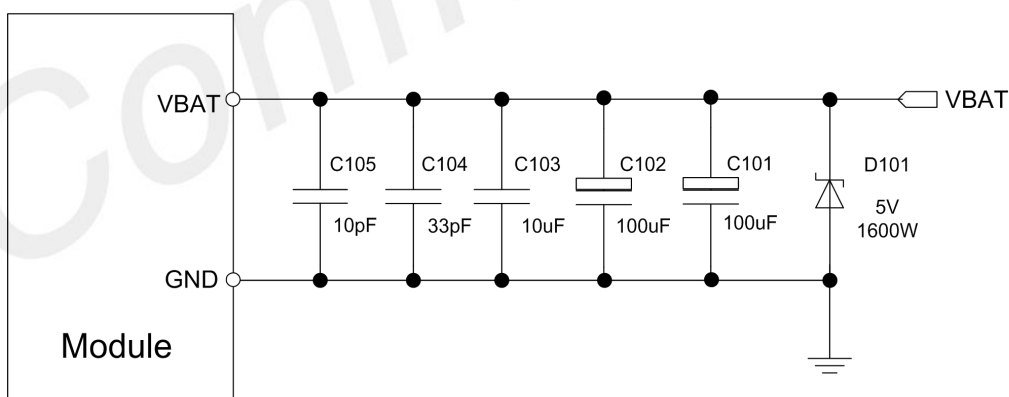


Figure 5: VBAT input reference circuit

Table 6: Recommended components

Posite	Supplier	Part number	parameter	package
C101 C102	AVX	TAJY107M010RNJ	ESR 0.9ohm@100KHz	7343-20
D101	Prisemi	PTVSHC3N4V8U	POWER 3200W	DFN2×2-3L
	Prisemi	PTVSHC2EN5VU	POWER 1600W	DFN1610-2L

3.2 Power On/off

3.2.1 Power on

Users can power on SIM8950x by pulling down the PWRKEY pin for more than 2 second then release. This pin is already pulled up to 1.8V internally, so external pull up is not necessary. The electrical characteristics are listed in Table 7, and reference circuits are shown in the following figures:

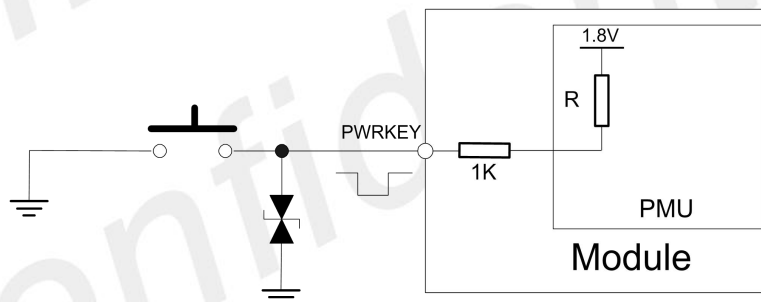


Figure 6: Powered on/off module using button

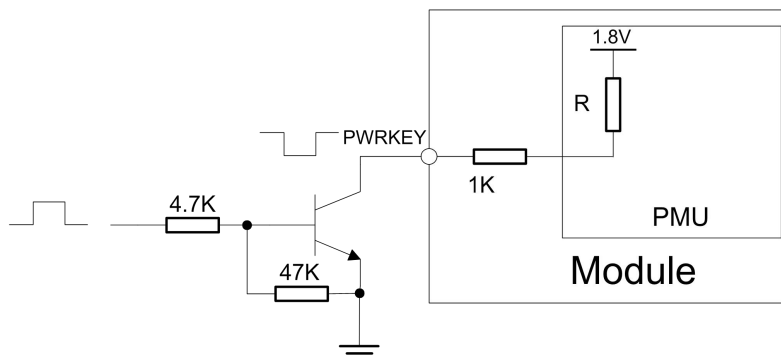


Figure 7: Powered on/off module using transistor

Table 7: PWRKEY characteristics

Parameters	Description	Min	Typ	Max	Unit
V _{IH}	High-level input voltage	1.4	-	-	V
V _{IL}	Low-level input voltage	-	-	0.6	V

3.2.2 Power-on sequence

The power-on sequence is shown in Figure 8.

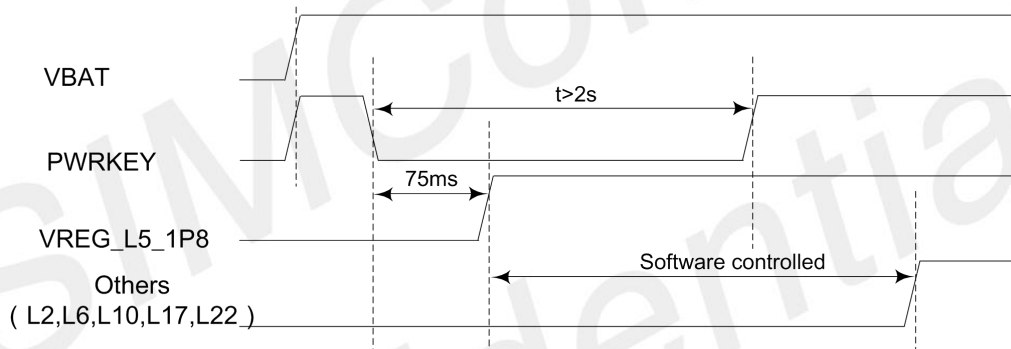


Figure 8: Power-on sequence

NOTE

- 1, Make sure that VBAT is stable before pulling down PWRKEY pin. The time between them is no less than 50ms.
- 2, PWRKEY pin cannot be pulled down all the time.

3.2.3 Power off sequence

Users can turn off SIM8950x by pulling down the PWRKEY pin for more than 1 second. After the module detects that the PWRKEY is low level, a prompt window will pop up on the screen to confirm whether to execute the shutdown action.

Module can also be forced to shut down by pulling down PWRKEY for more than 8 seconds.

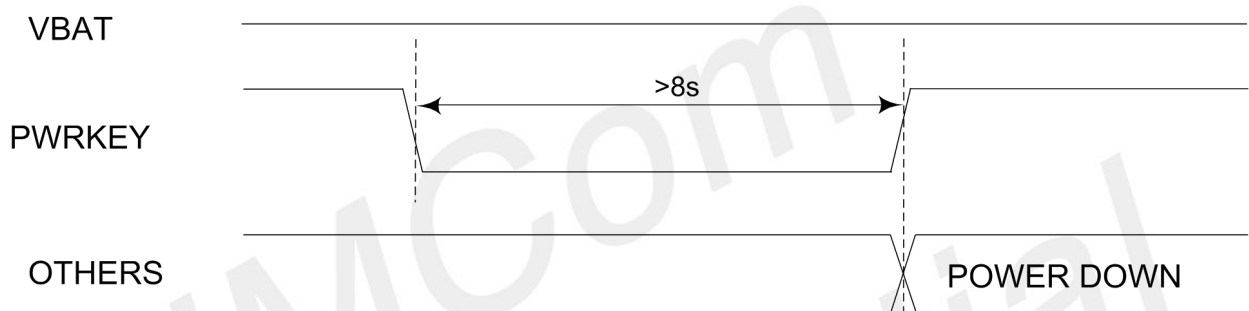


Figure 9: Power-off sequence

NOTE

1. The VBAT power supply circuit of the module can be cut off in the customer's hardware design.
2. It is recommended to add a low-cost MCU, which can control the PWRKEY to power on and power off the module, as well as the hardware watchdog to protect the normal operation.
3. Do not directly cut off the power supply VBAT of the module when the module is working normally, otherwise the internal flash of the module will be damaged. It is strongly recommended to shut down the module through PWRKEY or AT command before disconnecting the power supply VBAT of the module.

3.3 VRTC

VRTC is the power supply for RTC circuit and charger output for coin cell or backup battery. If RTC support is needed when the battery is removed, a qualified coin cell or keep-alive capacitor is required on the VRTC pin. When VBAT is present and valid, coin cell charging is enabled through software control and powered from VBAT. Reference circuits are shown in the following figures:

Keep-alive capacitor:

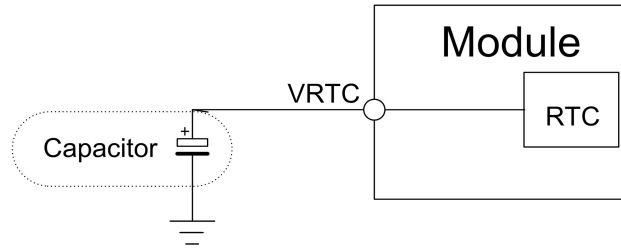


Figure 10: Keep-alive capacitor

Non-rechargeable battery:

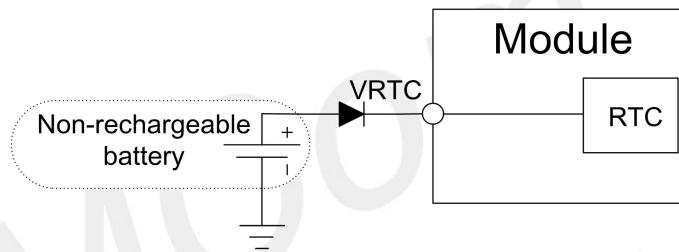


Figure 11: Non-rechargeable battery

Rechargeable battery:

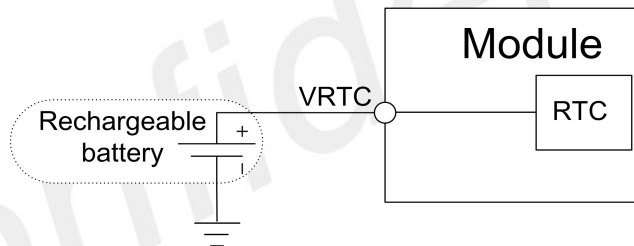


Figure 12: Rechargeable battery

VRTC typical voltage is 3.0V, and the current consumption is about 5uA when VBAT is absence. VRTC electrical characteristics are listed in the following table.

Table 8: VRTC characteristic

Parameter	Description	Min	Typ	Max	Unit
VRTC-IN	VRTC input voltage	2.0	3.0	3.25	V
I _{RTC-IN}	VRTC current consumption	-	7.5	-	uA
VRTC-OUT	VRTC output voltage	2.5	3.1	3.2	V
I _{RTC-OUT}	VRTC output current	-		2	mA

3.4 Output Power Management

Table 9: Output power management summary

Pin Name	Pin#	Specified range (V)	Programmable Range (V)	Rated current (mA)	Expected use
VREG_L22_2P8	4	2.8	1.750–3.3375	150	camera AVDD
VREG_L17_2P85	5	2.85	1.750–3.3375	300	display and camera VCM
VREG_L10_2P8	6	2.8	1.750–3.3375	150	Sensors and touch screen
VREG_L2_1P1	8	1.1	0.375–1.5375	1200	camera DVDD
VREG_L6_1P8	10	1.8	N/A	300	Display, camera, sensors
VREG_L23_1P175	11	1.175	0.375–1.5375	600	camera DVDD
VREG_L5_1P8	12	1.8	N/A	100	Force USB boot, level shifter
VREG_L11_2P95	149	2.95	N/A	800	SD/MMC card
VREG_L15_UIM2	172	1.8V/2.95V	N/A	50	UIM2
VREG_L14_UIM1	211	1.8V/2.95V	N/A	50	UIM1

3.5 USB Type-C Interface

SIM8950x module provides one USB 3.0/2.0 interface used for software upgrading, debugging, charging, etc. Moreover, SIM8950x has integrated Type-C interface to provide multiple Type-C features, including mode configuration, channel configuration, current advertisement, and active cable support.

In addition, SIM8950x supports OTG function, but external 5V power supply is required. USB_ID function could be configured via a GPIO (GPIO_140 is recommended), then connect it to PMI8953_GPIO_8 when using USB Type-C connector, or connect to USB_ID pin of connector when using micro USB connector.

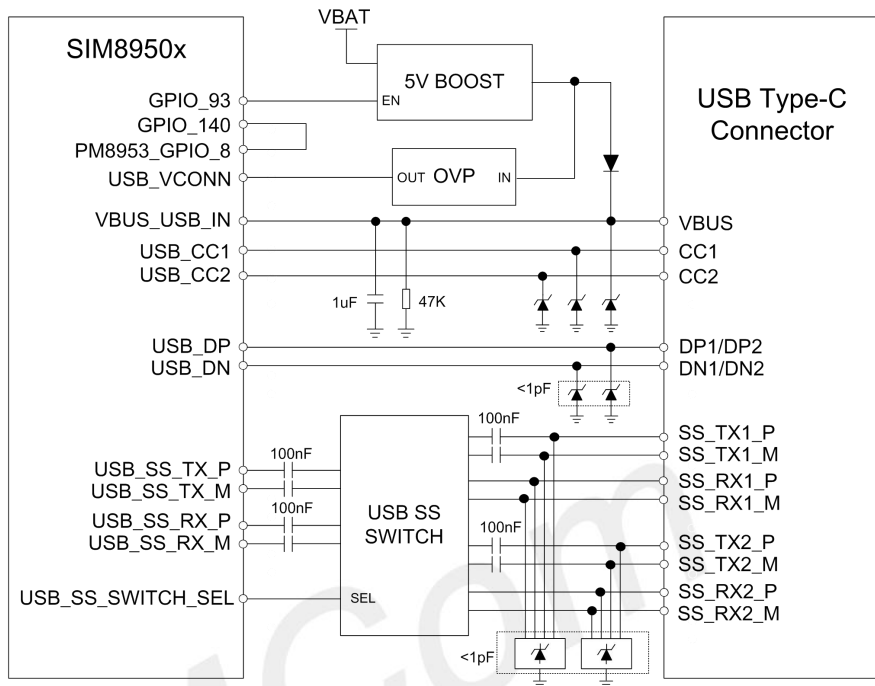


Figure 13: USB Type-C reference circuit

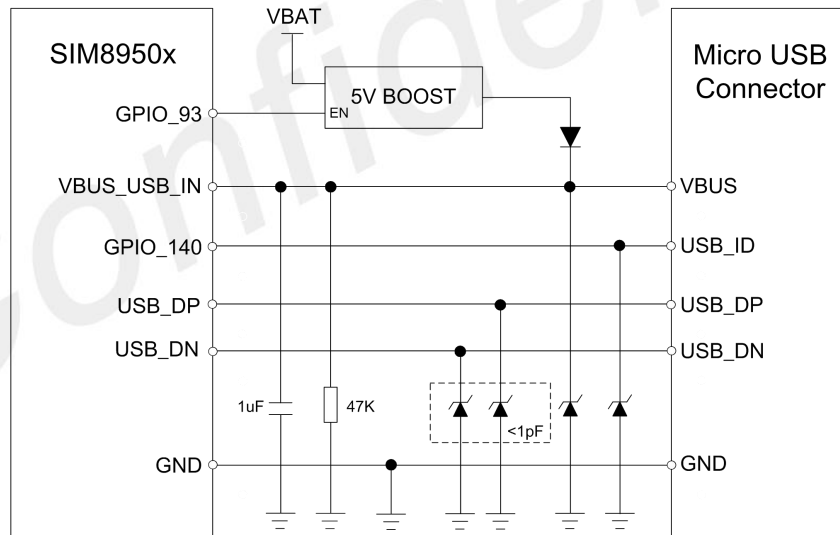


Figure 14: Micro USB reference circuit

3.6 UART/SPI/I2C

SIM8950x provides several sets of GPIOs which are available as BLSP (BAM-enabled low-speed peripheral) interfaces that can be configured to support various interface combinations, as shown in Table 10.

UART:

- Support 4*UART
- UART2 for debug, 2-line port.
- UART4、UART5 & UART6 are 4-line port that support RTS and CTS hardware flow control, the speed can up to 4Mbps.

SPI:

- Supports 5*SPI; master-only mode; up to 52 MHz

I2C:

- Support 8*I2C; master-only mode; up to 3.4 MHz, 2.2Kohm pull-up resistors are needed externally;

NOTE

CAM_I2C is a dedicated camera control interface, which cannot be used as general-purpose I2C ports.

Table 10: UART/SPI/I2C functional assignments

Pin Name	Pin#	Alternative Function 1	Alternative Function 2	Alternative Function 3
GPIO_0	45		SPI1_MOSI	
GPIO_1	46		SPI1_MISO	
GPIO_2	89		SPI1_CS	I2C1_SDA
GPIO_3	47		SPI1_CLK	I2C1_SCL
UART2_TX	37	UART2_TX		
UART2_RX	36	UART2_RX		
TS_I2C3_SDA	167			I2C3_SDA
TS_I2C3_SCL	117			I2C3_SCL
UART4_TX	182	UART4_TX	SPI4_MOSI	
UART4_RX	183	UART4_RX	SPI4_MISO	
SENSOR_I2C4_SDA	39	UART4_CTS	SPI4_CS	I2C4_SDA
SENSOR_I2C4_SCL	38	UART4_RTS	SPI4_CLK	I2C4_SCL
UART5_TX	26	UART5_TX	SPI5_MOSI	

UART5_RX	25	UART5_RX	SPI5_MISO	
GPIO_18	51	UART5_CTS	SPI5_CS	I2C5_SDA
GPIO_19	52	UART5_RTS	SPI5_CLK	I2C5_SCL
SPI6_MOSI	64	UART6_TX	SPI6_MOSI	
SPI6_MISO	65	UART6_RX	SPI6_MISO	
SPI6_CS	62	UART6_CTS	SPI6_CS	I2C6_SDA
SPI6_CLK	63	UART6_RTS	SPI6_CLK	I2C6_SCL
LCD_BL_EN	122		SPI7_MOSI	
GPIO_138	75		SPI7_MISO	
LCD1_RST_N	120		SPI7_CS	I2C7_SDA
GPIO_135	74		SPI7_CLK	I2C7_SCL
GPIO_98	78			I2C8_SDA
GPIO_99	77			I2C8_SCL
CAM_I2C_SDA	94			CAM_I2C_SDA0
CAM_I2C_SCL	95			CAM_I2C_SCL0

3.7 Secure Digital Interface

SIM8950x provides one 4-bit secure digital interface, which supports SD 3.0 specifications.

Table 11: SD interface pin definitions

Pin Name	Pin#	I/O	Description
VREG_L11_2P95	149	PO	LDO 11 output for SD card
SDC2_CLK	156	DO	Secure digital controller 2 clock
SDC2_CMD	155	DI/DO	Secure digital controller 2 command
SDC2_DATA0	154	DI/DO	Secure digital controller 2 data bit 0
SDC2_DATA1	153	DI/DO	Secure digital controller 2 data bit 1
SDC2_DATA2	152	DI/DO	Secure digital controller 2 data bit 2
SDC2_DATA3	151	DI/DO	Secure digital controller 2 data bit 3
SD_DET_N	150	DI	Secure digital card detection

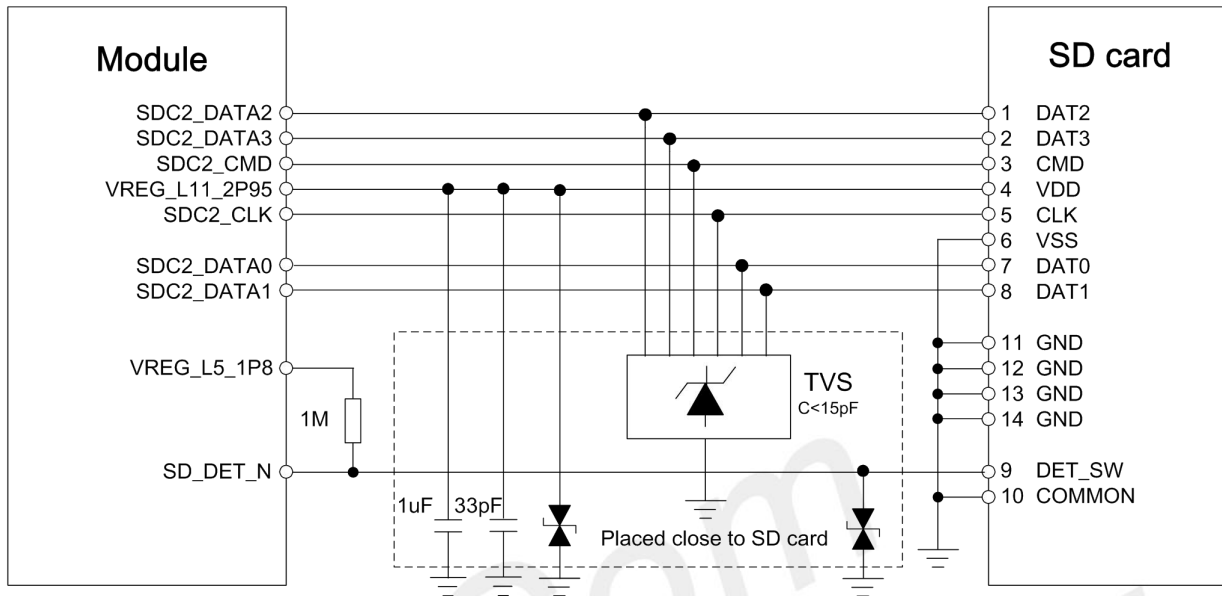


Figure 15: SD card reference circuit

NOTE

SDC signal cannot be pulled up to VREG_L11_2P95.

3.8 LCD Interface

SIM8950x provides two 4-lane MIPI_DSI, with 2.1 Gbps per lane high-speed mode bandwidth, to support dual LCDs with FHD (1920 × 1200 @ 60 fps) resolution.

NOTE

MIPI_DSI0 must be used for primary display.

Table 12: Display interface pin definitions

Pin Name	Pin#	I/O	Description
MIPI_DSI0_CLK_P	135	AO	Primary display serial interface 0
MIPI_DSI0_CLK_N	136	AO	
MIPI_DSI0_LANE0_P	137	AI/AO	
MIPI_DSI0_LANE0_N	138	AI/AO	
MIPI_DSI0_LANE1_P	139	AI/AO	
MIPI_DSI0_LANE1_N	140	AI/AO	
MIPI_DSI0_LANE2_P	141	AI/AO	
MIPI_DSI0_LANE2_N	142	AI/AO	
MIPI_DSI0_LANE3_P	143	AI/AO	
MIPI_DSI0_LANE3_N	144	AI/AO	
MIPI_DSI1_CLK_P	124	AO	Secondary display serial interface 1
MIPI_DSI1_CLK_N	125	AO	
MIPI_DSI1_LANE0_P	126	AI/AO	
MIPI_DSI1_LANE0_N	127	AI/AO	
MIPI_DSI1_LANE1_P	128	AI/AO	
MIPI_DSI1_LANE1_N	129	AI/AO	
MIPI_DSI1_LANE2_P	130	AI/AO	
MIPI_DSI1_LANE2_N	131	AI/AO	
MIPI_DSI1_LANE3_P	132	AI/AO	
MIPI_DSI1_LANE3_N	133	AI/AO	
LCD1_RST_N	120	DO	LCD1 reset
LCD0_RST_N	121	DO	LCD0 reset
LCD_BL_EN	122	DO	LCD back light enable
PWM	33	DO	PWM control for external WLED driver

If only 2-lane MIPI_DSI is needed, just leave LANE2 and LANE3 floating. The reference circuit is shown in Figure 15.

Common mode filters is recommended for EMI issue, and it may be omitted if best EMI practices are followed.

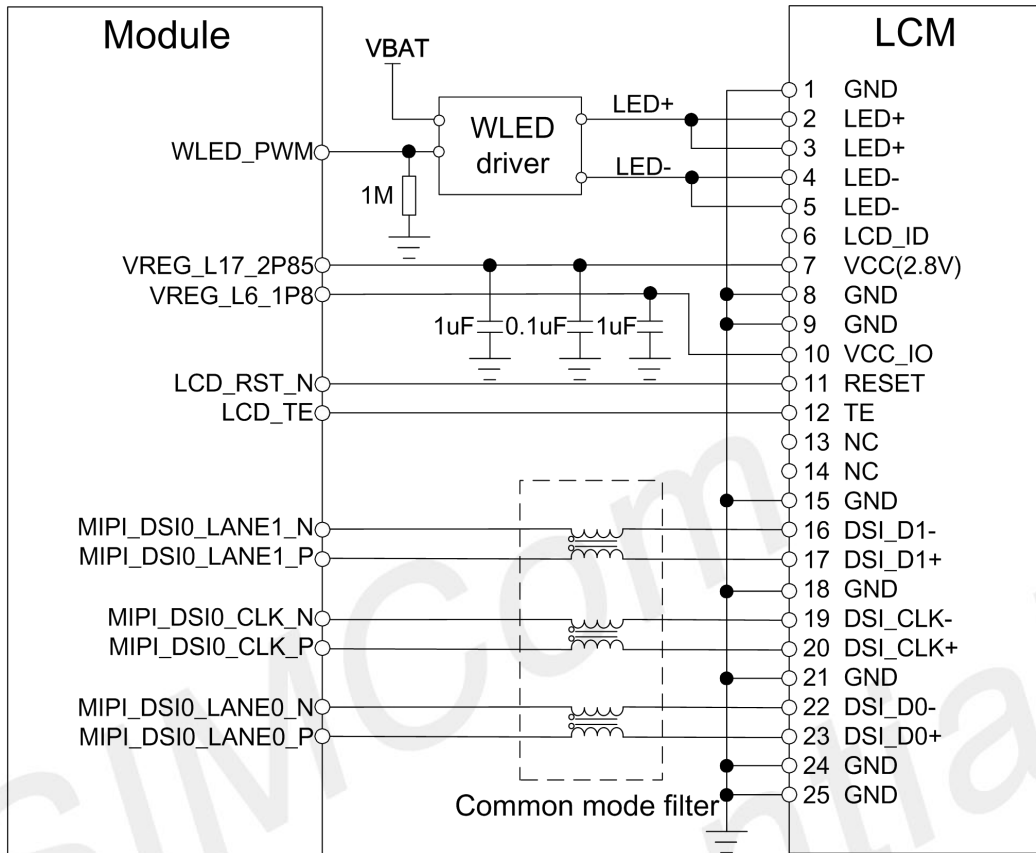


Figure 16: Display reference circuit

3.9 Touch Screen Interface

Table 13: Touch screen interface pin definitions

Pin Name	Pin#	I/O	Description
TS_I2C3_SDA	167	DI/DO	Touch screen I2C data
TS_I2C3_SCL	117	DO	Touch screen I2C clock
TS_INT_N	119	DI	Touch screen interrupt
TS_RST_N	118	DO	Touch screen reset

3.10 Camera Interface

SIM8950x supports two cameras:

4-lane MIPI_CSI primary camera up to 21MP resolution

2-lane MIPI_CSI secondary camera up to 8MP resolution.

Table 14: Camera interface pin definitions

Pin Name	Pin#	I/O	Description
MIPI_CSI0_LANE3_N	104	AI/AO	Primary camera serial interface 0
MIPI_CSI0_LANE3_P	105	AI/AO	
MIPI_CSI0_LANE2_N	106	AI/AO	
MIPI_CSI0_LANE2_P	107	AI/AO	
MIPI_CSI0_LANE1_N	108	AI/AO	
MIPI_CSI0_LANE1_P	109	AI/AO	
MIPI_CSI0_LANE0_N	110	AI/AO	
MIPI_CSI0_LANE0_P	111	AI/AO	
MIPI_CSI0_CLK_N	112	AI	
MIPI_CSI0_CLK_P	113	AI	
MIPI_CSI2_LANE1_N	97	AI/AO	Secondary camera serial interface 2
MIPI_CSI2_LANE1_P	98	AI/AO	
MIPI_CSI2_LANE0_N	99	AI/AO	
MIPI_CSI2_LANE0_P	100	AI/AO	
MIPI_CSI2_CLK_N	101	AI	
MIPI_CSI2_CLK_P	102	AI	
CAM2_PWD_N	90	DO	Secondary Camera power down, cannot be pull up externally
CAM2_RST_N	91	DO	Secondary Camera reset
CAM0_RST_N	92	DO	Primary Camera reset
CAM0_PWD_N	93	DO	Primary Camera power down
CAM_I2C_SDA	94	DI/DO	Dedicated Camera I2C data
CAM_I2C_SCL	95	DO	Dedicated Camera I2C clock
CAM_MCLK2	115	DO	Secondary Camera master clock
CAM_MCLK0	116	DO	Primary Camera master clock

The reference circuit is shown in the following figures.

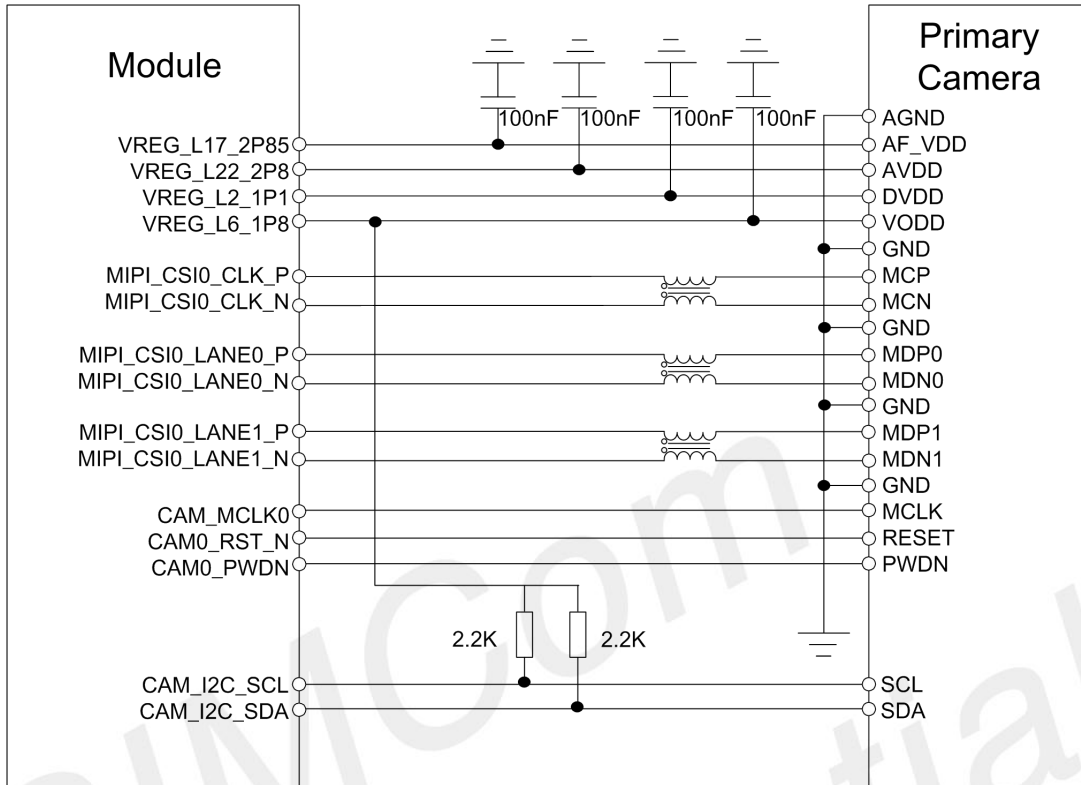


Figure 17: Primary camera reference circuit

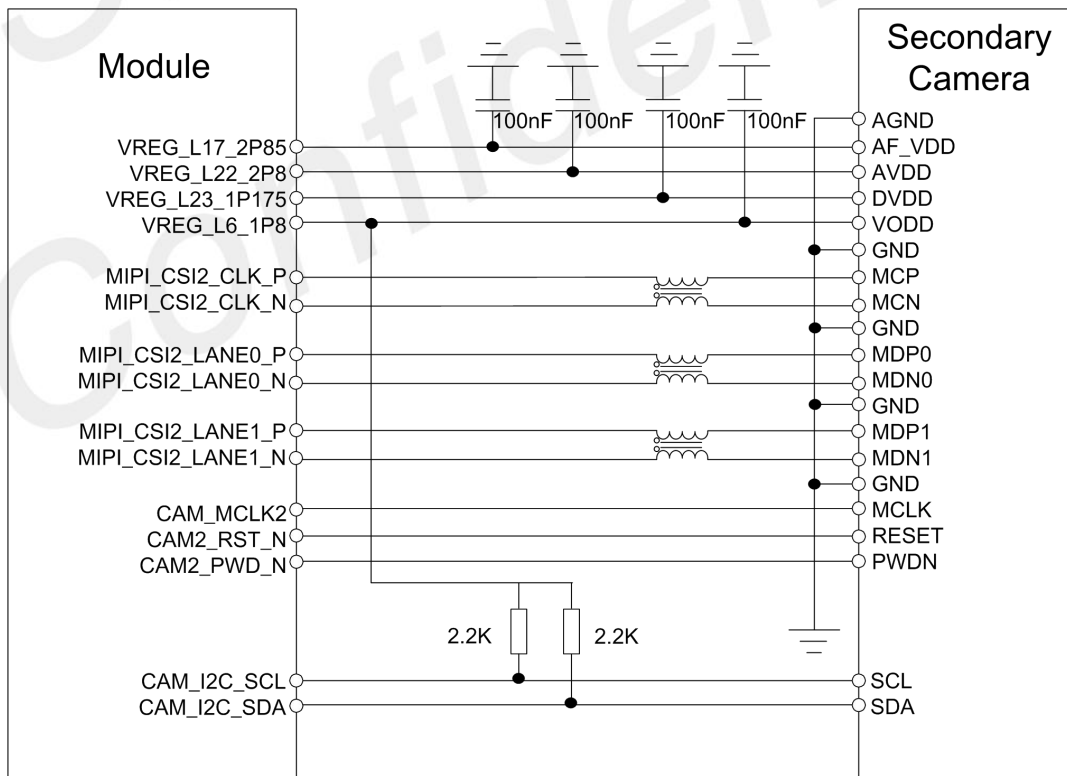


Figure 18: Secondary camera reference circuit

The sim8950x module has built-in dual ISPs, which can support two cameras working at the same time. The primary camera and secondary camera need independent I2C control. The reference circuit is shown as follows:

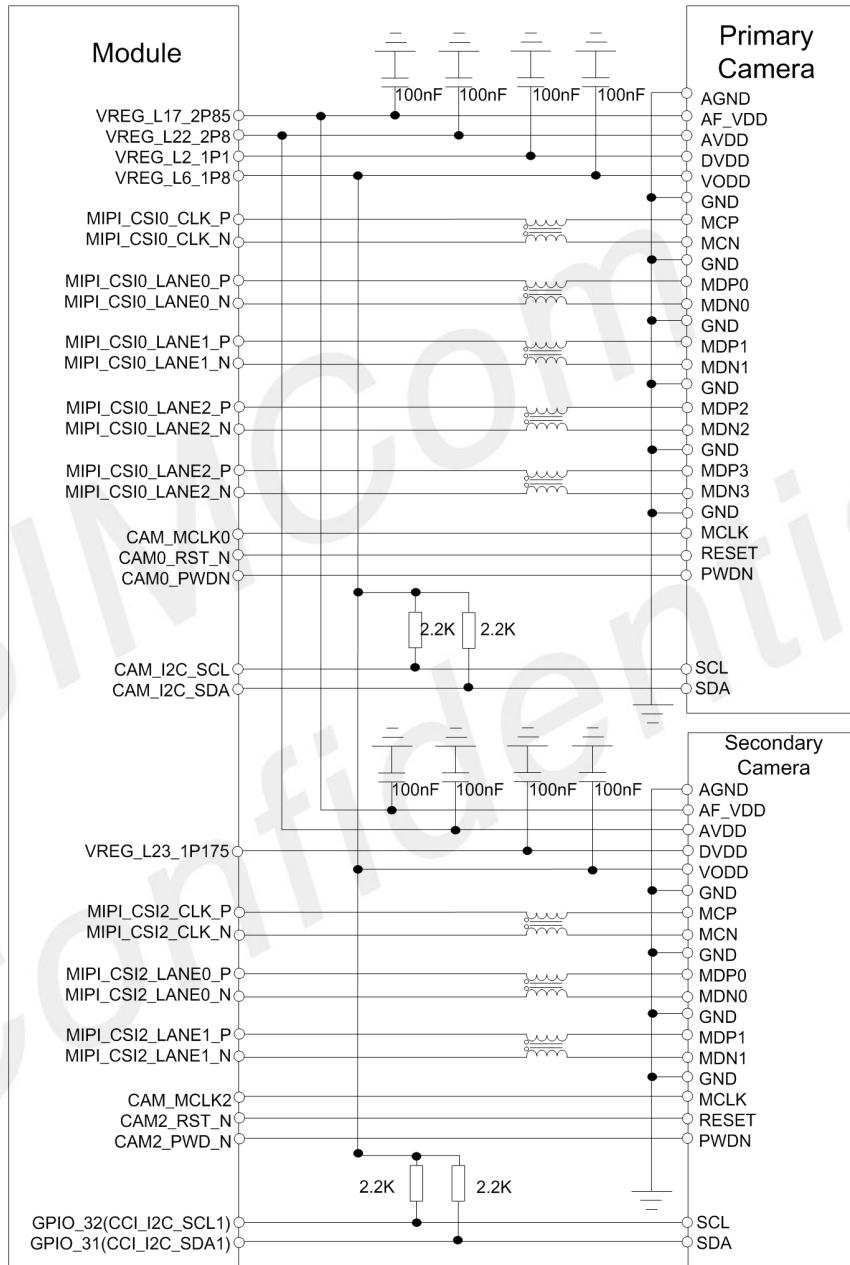


Figure 19: Dual camera reference circuit

3.11 Audio

SIM8950x provides three microphone inputs and four outputs including earpiece, stereo headphones, and mono class-D speaker driver.

Table 15: Audio interface pin definitions

Pin Name	Pin#	I/O	Description
SPK_P	16	AO	Speaker driver output, positive
SPK_N	17	AO	Speaker driver output, negative
EAR_P	19	AO	Earpiece output, positive
EAR_N	20	AO	Earpiece output, negative
HPH_L	21	AO	Headphone output, left channel
HPH_REF	22	AI	Headphone ground reference
HPH_R	23	AO	Headphone output, right channel
HS_DET	24	AI	Headset detection
MIC2_P	28	AI	Microphone input 2, positive
MIC1_N	30	AI	Microphone input 1, negative
MIC1_P	31	AI	Microphone input 1, positive
MIC3_P	9	AI	Microphone input 3, positive
MIC_BIAS1	7	PO	Microphone bias1
LINEOUT_P	202	AO	LINEOUT output, positive
LINEOUT_N	203	AO	LINEOUT output, negative

3.11.1 Microphone

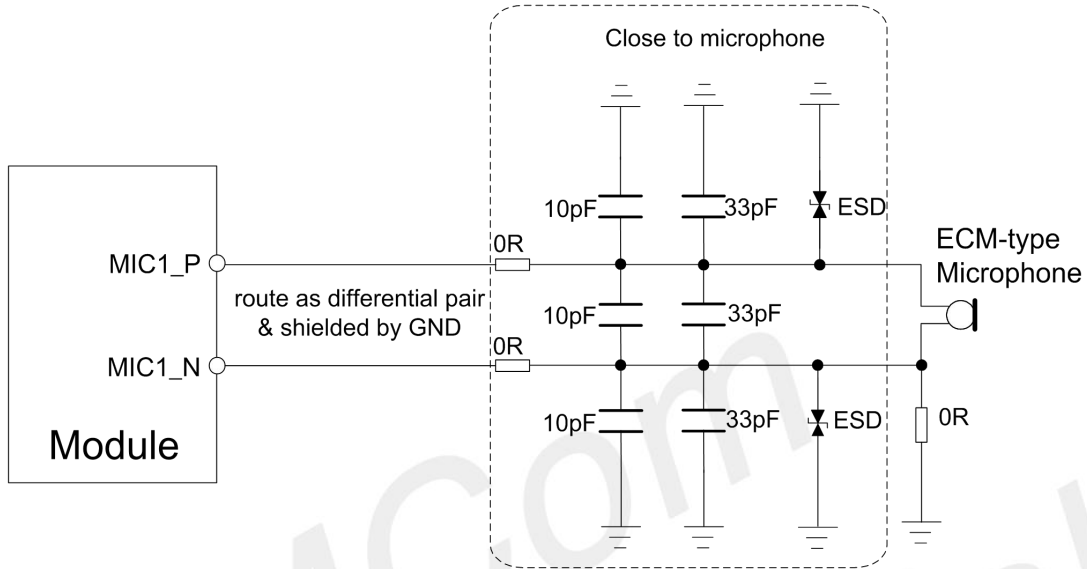


Figure 20: ECM-type microphone reference circuit

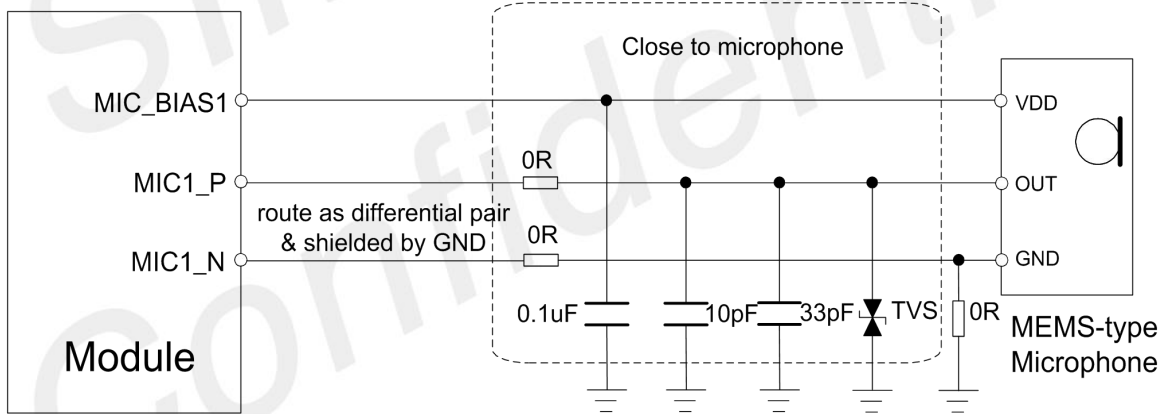


Figure 21: MEMS-type microphone reference circuit

3.11.2 Headset

Stereo class-AB headphone supports 16 Ω , 32 Ω , and up to 50 K Ω loads. Its typical output power at 1.02 KHz and THD + N \leq 1% is:

62 mW with 16 Ω loads, 0 dBFS and 0 dB gain
 30 mW with 32 Ω loads, 0 dBFS and 0 dB gain

A 100K Ω pull-down resistor is integrated at HPH_L pin, which could be used for mechanical insertion or removal detection through HS_DET pin. Figure 20 shows the reference circuit for normally-closed (NC) type headset jack.

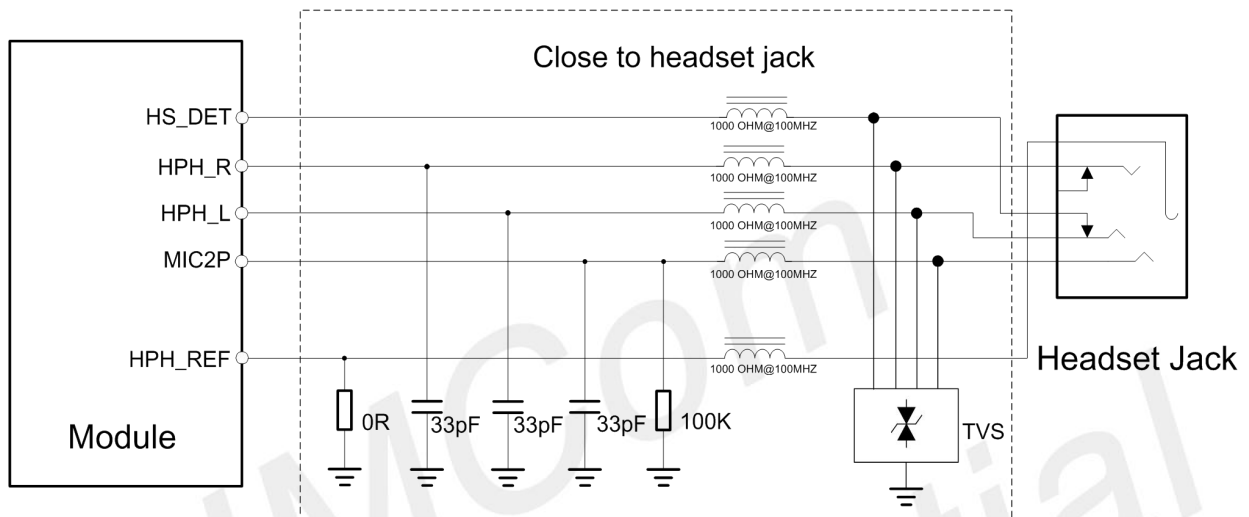


Figure 22: Headset reference circuit

NOTE

1. SIM8950x also supports NO/NC type headset jack with detect pin on HPH_L or GND.
2. HPH has a negative swing and requires a bi-directional TVS diode.

3.11.3 Earpiece

Class AB earpiece driver supports 10.67 Ω , 16 Ω , 32 Ω , and up to 50 K Ω loads. The typical output power at 1.02 KHz, 6 dB gain, and THD + N \leq 1% is:

126 mW with 32 Ω loads and 0 dBFS input

243 mW with 16 Ω loads and -1.5 dBFS input

320 mW with 10.67 Ω loads and -3.5 dBFS input

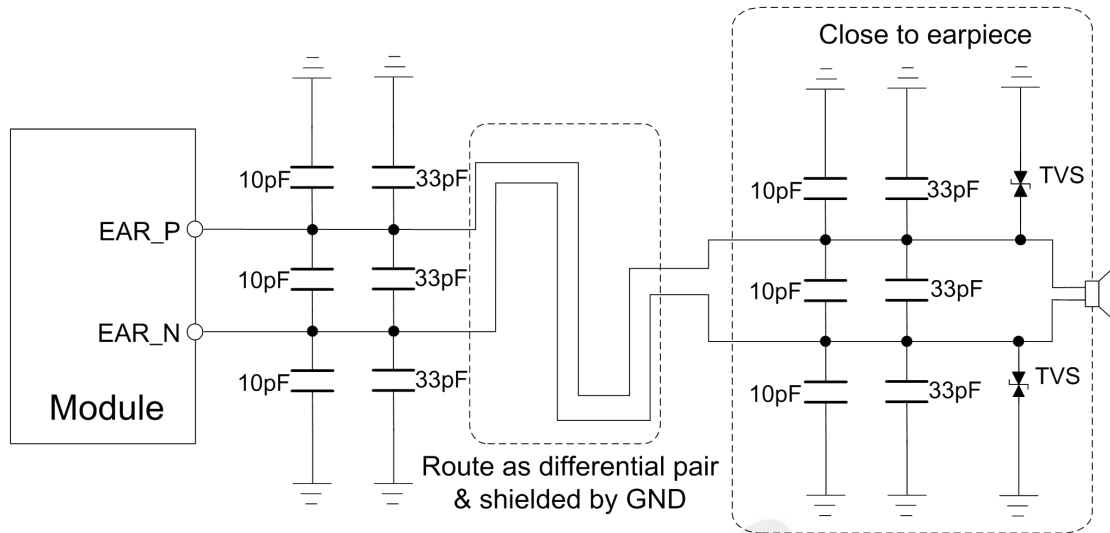


Figure 23: Earpiece reference circuit

3.11.4 Speaker

Class-D mono differential loud speaker driver supports 4 Ω and 8 Ω loads. The driver is powered from internal 5 V Boost (VDD_SPKR). Its typical output power at 1.02 KHz, 12 dB gain, and THD + N \leq 1% is:

1500 mW with 4 Ω loads and VDD_SPKR = 5V

2000 mW with 8 Ω loads and VDD_SPKR = 5.5V

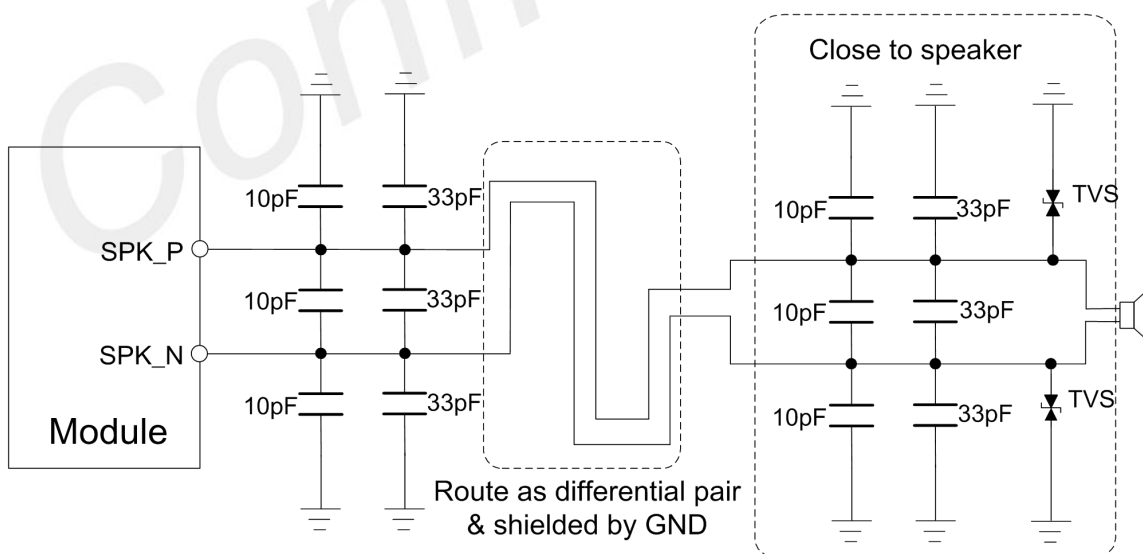


Figure 24: Speaker reference circuit

NOTE

the maximum breakdown voltage of TVS for SPKR should not be less than 6 V.

3.11.5 LINEOUT

LINEOUT is a differential class-AB output to drive external speaker amplifier for loudspeaker.

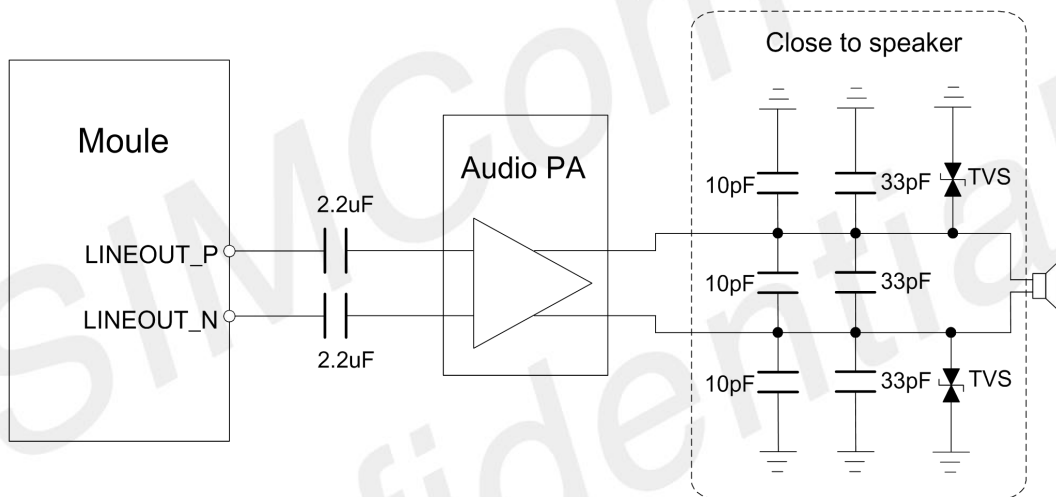


Figure 25: LINEOUT reference circuit

3.12 I2S Interface

SIM8950x supports one I2S port, the pin definitions are shown in Table 16.

Table 16: I2S interface pin definitions

Pin Name	Pin#	Alternative Function (I2S)	Type	Description
GPIO_135	74	I2S_SCK	DI/DO	I2S bit clock
LCD1_RST_N	120	I2S_WS	DI/DO	I2S word select
LCD0_BL_EN	122	I2S_D0	DI/DO	I2S data0
GPIO_138	75	I2S_D1	DI/DO	I2S data1

3.13 UIM Interface

SIM8950x supports dual cards dual standby, and card presence detection.

NOTE

The standard software provided by SIMCom only supports single UIM card configuration.

Table 17: UIM interface pin definitions

Pin Name	Pin#	Type	Description
VREG_L15_UIM2	172	PO	LDO 15 output for UIM2, 1.8V/2.95V
UIM2_DATA	174	DI/DO	UIM2 data , Need 10K external Pull-up resistor
UIM2_CLK	176	DO	UIM2 clock
UIM2_RESET	178	DO	UIM2 reset
UIM2_DET	180	DI	UIM2 presence detection
UIM1_DET	205	DI	UIM1 presence detection
UIM1_RESET	207	DO	UIM1 reset
UIM1_CLK	208	DO	UIM1 clock
UIM1_DATA	210	DI/DO	UIM1 data , Need 10K external Pull-up resistor
VREG_L14_UIM1	211	PO	LDO 14 output for UIM1, 1.8V/2.95V

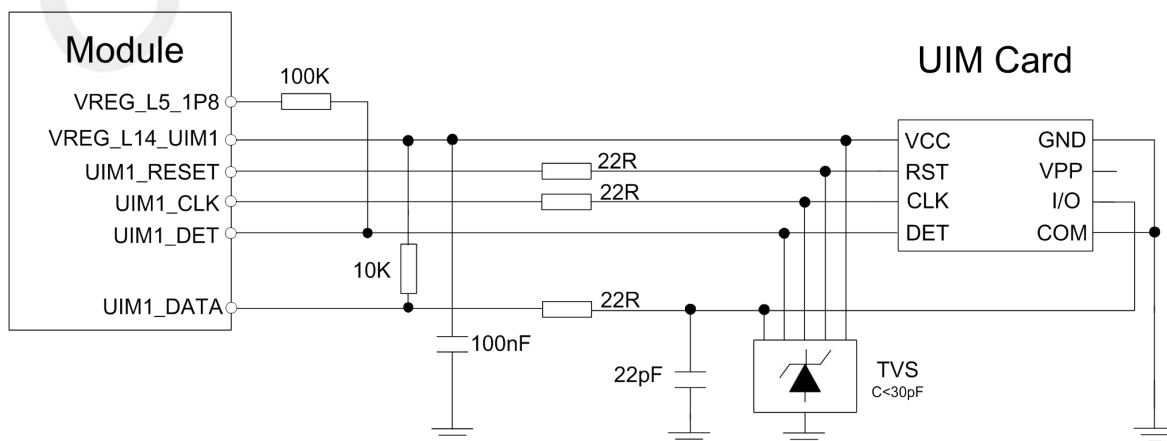


Figure 26: UIM card reference circuit

3.14 ADC

SIM8950x provides one 16bits ADC. Its performance parameters are shown as Table 18.

Table 18: ADC performance parameters

Parameter	Comments	Min	Typ	Max	Unit
Input voltage range	Programmable	0.1 0.3	- -	1.7 4.5	V
Resolution		-	16	-	bits
Analog input bandwidth		-	100	-	kHz
Sample rate	XO/8	-	2.4	-	MHz
INL	15-bit output	-	-	±8	LSB
DNL	15-bit output	-	-	±4	LSB
Offset error	Relative to full-scale	-	-	±1	%
Gain error	Relative to full-scale	-	-	±1	%

3.15 Antenna Interface

SIM8950x provides four antenna interfaces including MAIN antenna, DRX antenna, GNSS antenna, and WiFi/BT antenna. To ensure good RF performance, users should meet the following requirements:

- Keep the RF traces at 50Ω.
- Maintain a complete and continuous reference ground plane from antenna pin to the RF connector.
- The RF traces should be away from any other noisy traces.
- Keep the RF traces as short as possible.

3.15.1 MAIN Antenna reference circuit

The recommended circuit is shown in the following figures:

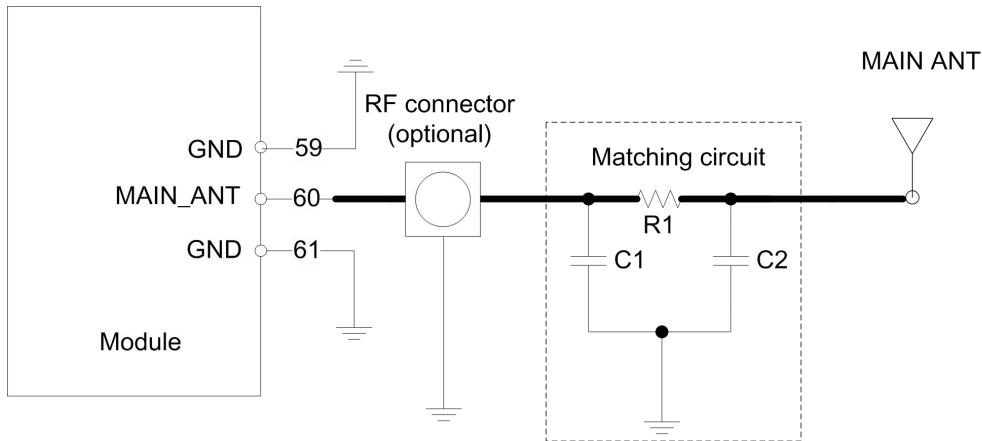


Figure 27: MAIN antenna recommended circuit

R1, C1 and C2 are antenna matching components in Figure 27, the value of these components are determined according to the antenna tuning results. By default, R1 is 0Ω, C1 and C2 are reserved. The RF connector in Figure 27 is used to ensure the accuracy and convenience of the conduction testing, so SIMCOM suggest keeping it. If considering Low-Cost BOM, user can cancel the connector.

3.15.2 DRX Antenna reference circuit

The recommended circuit is shown in the following figures:

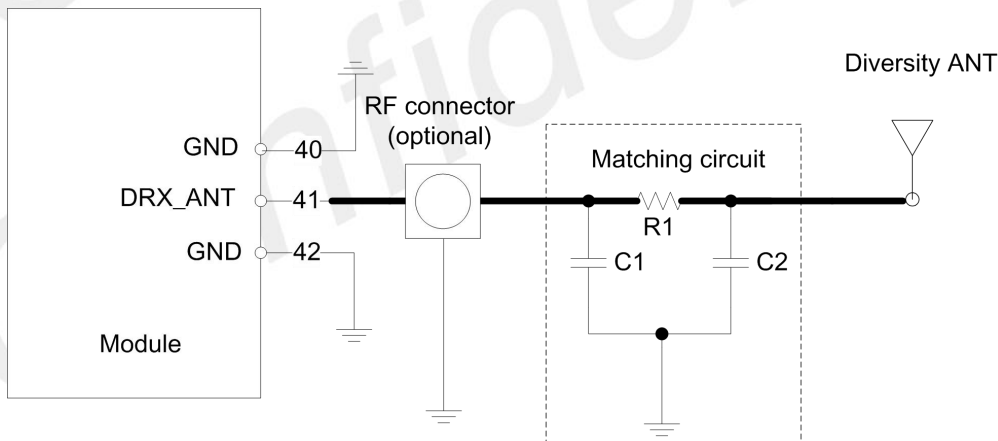


Figure 28: DRX antenna recommended circuit

R1, C1 and C2 are antenna matching components in Figure 28, the value of these components are determined according to the antenna tuning results. By default, R1 is 0Ω, C1 and C2 are reserved. The RF connector in Figure 28 is used to ensure the accuracy and convenience of the conduction testing, so SIMCOM suggest keeping it. If considering Low-Cost BOM, user can cancel the connector.

3.15.3 GNSS Antenna reference circuit

The recommended circuit is shown in the following figures:

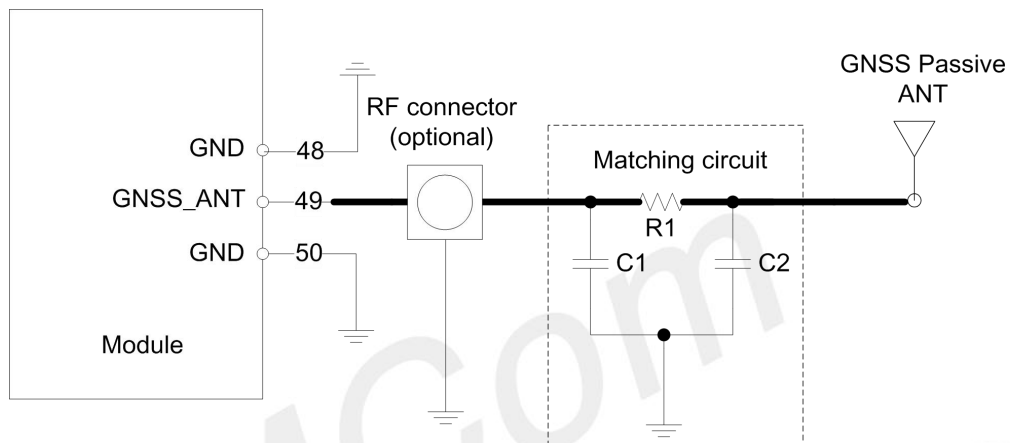


Figure 29: GNSS antenna recommended circuit

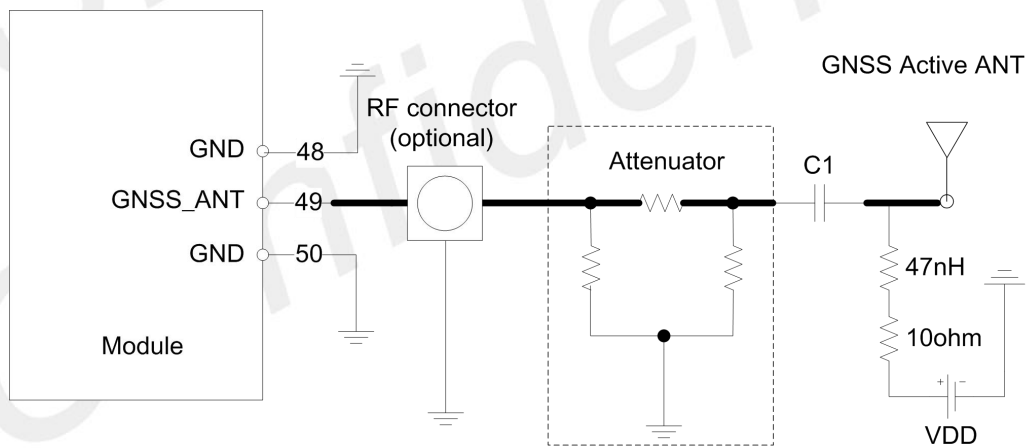


Figure 30: GNSS active antenna circuit

The attenuator in Figure 30 must be added as required and attenuation value is determined according to the active antenna gain. Normally, the relationship between the attenuation value and the gain satisfies the following formula:

$$\text{Antenna gain} = \text{Attenuation value} + \text{Cable Losses}$$

In Figure 30, the VDD is used to provide voltage to the external active antenna and its value should be

taken according to antenna characteristic; C1 is used for DC blocking and its value is 33pF by default.; the RF connector is used to ensure the accuracy and convenience of the conduction testing, if considering LOW-Cost BOM, users can cancel it.

3.15.4 WiFi/BT Antenna reference circuit

The recommended circuit is shown in the following figures:

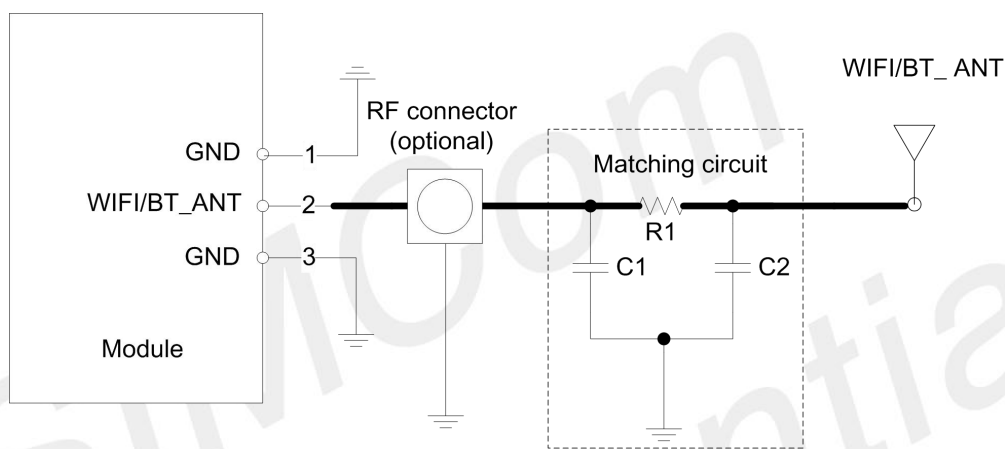


Figure 31: WIFI/BT antenna recommended circuit

R1, C1 and C2 are antenna matching components in Figure 31, the value of these components are determined according to the antenna tuning results. By default, R1 is 0Ω, C1 and C2 are reserved. The RF connector in Figure 31 is used to ensure the accuracy and convenience of the conduction testing, so SIMCOM suggest keeping it. If considering Low-Cost BOM, user can cancel the connector.

3.16 RF traces layout guidelines

The characteristic impedance of RF signals should be controlled at 50 ohm. In general, the impedance of RF signal is determined by the Permittivity (ER) of PCB material, line width (W), ground clearance (S), height of reference ground plane (H) and other factors.

Microstrip line and coplanar waveguide are usually used to control the characteristic impedance of RF wiring. The following illustrations show the structure design of microstrip line and coplanar waveguide.

- **Microstrip line structure**

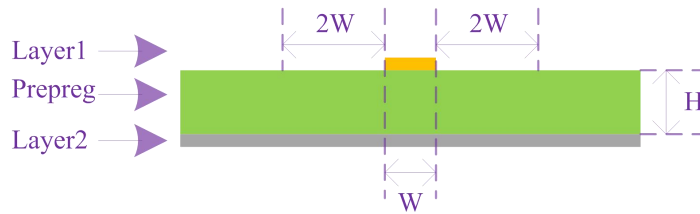


Figure 32: Two layer PCB microstrip structure

Table 19: Example of impedance control of microstrip line structure

PCB thickness	Permittivity (ER)	Line thickness	Layer	Reference plane	Target impedance	Expected linewidth W
1mm	4.2	0.035mm	Layer1	Layer2	50 ohm	1.7mm (67 mil)
1.6mm	4.2	0.035mm	Layer1	Layer2	50 ohm	3mm (118 mil)

- Coplanar waveguide (CPW) structure (recommended)

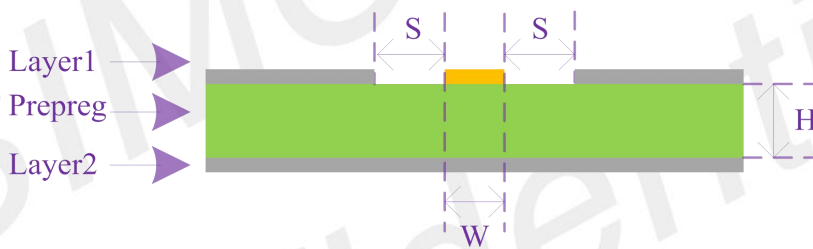


Figure 33: Two layer PCB coplanar waveguide structure

Table 20: Example of impedance control of coplanar waveguide structure

PCB thickness	Permittivity (ER)	Line thickness	Layer	Reference plane	Target impedance	Expected gap to ground S	Expected linewidth W
1mm	4.2	0.035mm	Layer1	Layer2	50 ohm	0.65mm (25.6 mil)	0.2mm (7.8 mil)
1.6mm	4.2	0.035mm	Layer1	Layer2	50 ohm	0.65mm (25.6 mil)	0.15mm (5.9 mil)

Four layer PCB coplanar waveguide structure 1# is shown in following figure. The third layer is reference layer.

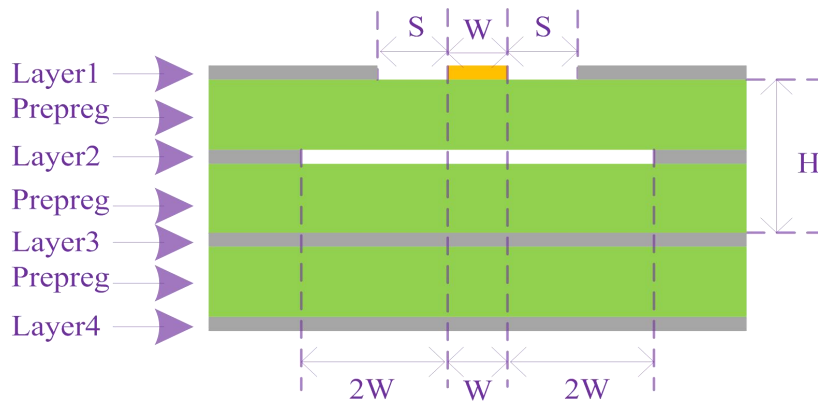


Figure 34: Four layer PCB coplanar waveguide structure 1#

Four layer PCB coplanar waveguide structure 2# is shown in following figure. The fourth layer is reference layer.

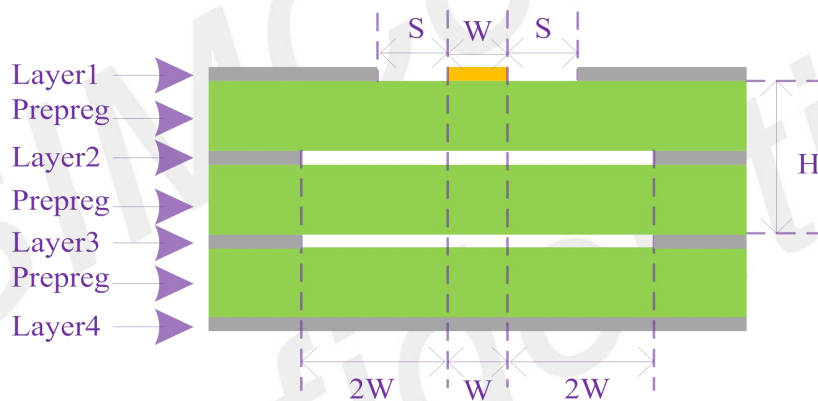


Figure 35: Four layer PCB coplanar waveguide structure 2#

3.17 Antenna Requirement

The following table shows the requirements on main antenna, Rx-diversity antenna and GNSS antenna.

Table 21: Antenna Requirement

Antenna	Requirements
GSM/WCDMA/TD-SCDMA/LTE	VSWR: ≤ 2 Gain (dBi): >1 Max Input Power (W): 50 Input Impedance (ohm): 50 Polarization Type: Vertical

Wi-Fi/BT	VSWR: ≤ 2 Gain (dBi): >1 Max Input Power (W): 50 Input Impedance (ohm): 50 Polarization Type: Vertical
GNSS	Frequency range: 1565-1607MHz Polarization: RHCP or linear VSWR: < 2 (Typ.) Passive antenna gain: >0 dBi Active antenna noise figure: < 1.5 dB Active antenna gain: > 0 dBi Active antenna embedded LNA gain: <17 dB

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4. PCB Layout

This section provides PCB layout guidelines for SIM8950x users to ensure their production against lots of issues, and achieve the optimum performance.

4.1 General Placement Guidelines

At least, 4-layer through-hole PCB should be chosen for good impedance control and signal shielding.

4.2 General Placement Guidelines

- Digital devices and traces should not be placed near sensitive signals like RF and clock.
- Keep SPKR and MIC away from sensitive RF lines.

4.3 PCB Layout Guideline Details

4.3.1 RF Trace

- RF connector should be placed close to the module's antenna pin.
- Antenna matching circuit should be placed close to the antenna.
- Keep the RF traces at 50Ω.
- Maintain a complete and continuous reference ground plane from antenna pin to the RF connector.
- The RF traces should be far away from any other noisy traces.
- Keep the RF traces as short as possible.
- If using a coaxial RF cable to connect the antenna, please avoid spanning on UIM cards, power circuits and high-speed digital circuits to minimize the impact of each other.

4.3.2 Power/GND

- Both VBAT and return path should be as short and wide as possible to minimize the IR drop
- The VBAT current should go through Zener diode, capacitors, then VBAT pins
- Must have a solid ground plane throughout the board as the primary reference plane for most signals

4.3.3 UIM Card

- Ensure UIM card holder is far way from antenna or RF signal
- ESD component and bypass caps should be placed closed to UIM Card
- UIM card signals should be far away from other high-speed signal

4.3.4 MIPI_DSI/CSI

- Protect MIPI_DSI/CSI signals from noisy signals (clocks, SMPS, etc.)
- Differential pairs, 100 Ω nominal, $\pm 10\%$
- Total routing length < 305 mm
- Intra-pair length matching < 5 ps (0.67 mm)
- Inter-pair length matching < 10 ps (1.3 mm)
- Lane-to-lane trace spacing = 3x line width
- Spacing to all other signals = 4x line width
- Maintain a solid ground reference for clocks to provide a low-impedance path for return currents
- Each trace needs to be next to a ground plane
- Minimize the number of via on the trace

4.3.5 USB

- 90 Ω differential, $\pm 10\%$ trace impedance
- Differential data pair matching < 6.6 mm (50 ps)
- External components should be located near the USB connector.
- Should be routed away from sensitive circuits and signals.
- If there are test points, place them on the trace to keep branches as short as possible
- If USB connector is used as the charger input, USB_VBUS node must be routed to the module using extremely wide traces or sub planes.

4.3.6 SDC

- Protect other sensitive signals/circuits from SDC corruption.
- Protect SDC signals from noisy signals (clocks, SMPS, etc.).
- Up to 200 MHz clock rate
- 50 Ω nominal, $\pm 10\%$ trace impedance
- CLK to DATA/CMD length matching < 1 mm
- 30–35 Ω termination resistor on clock lines near the module
- Total routing length < 50 mm recommended
- Spacing to all other signals = 2x line width
- Bus capacitance < 15 pF

4.3.7 Audio

Analog input

- 4 to 5 mil trace widths; 4 to 5 mil spacing between traces
- Differential route for MIC1P with MIC1N and MIC2P with GND_MIC;
- Isolate from noise sources, such as antenna, RF signals, SMPS, clocks, and other digital signals with fast transients

Analog output

- Coplanar ground fill on both sides (of traces or pair as appropriate); in between ground planes – grounds above and below
- Isolate from noise sources such as antenna, RF signals, SMPS, clocks, and other digital signals with fast transients.
- EAR output signal – route as differential pair with 10 mil trace widths.
- SPKR output signals – route as differential pair with 20 mil trace widths with 8 Ω load and 25 mil trace widths with 4 Ω load
- HPH output signals – not a differential pair; 10 mil trace widths for HPH_L and HPH_R; 15 mil trace widths for HPH_REF
- Connect HPH_REF to the ground pin of the jack connector and route HPH_REF in between HPH_L and HPH_R for best crosstalk minimization

5. Electrical and Reliability

5.1 Absolute Maximum Ratings

Absolute maximum ratings reflect the stress levels that, if exceeded, may cause permanent damage to the device. Functionality and reliability are only guaranteed within the operating conditions.

Table 22: Absolute maximum ratings

Parameter	Min	Max	Unit
VBAT	-0.3	5	V
VBUS	-0.3	28	V
VRTC	-	3.5	V

5.2 Temperature Range

Table 23: Temperature range

Parameter	Min	Typ	Max	Unit
Operating temperature	-25	25	+75	°C
Storage temperature	-45		+90	°C

5.3 Operating Voltage

Table 24: Operating voltage

Parameter	Min	Typ	Max	Unit
VBAT	3.4	3.9	4.4	V
VBUS	4.35	5	10	V
VRTC	2.0	3.0	3.25	V

5.4 Digital-logic Characteristics

Table 25: 1.8 V digital I/O characteristics

Parameter	Description	Min	Typ	Max	Unit
V _{IH}	High-level input voltage	1.17	-	-	V
V _{IL}	Low-level input voltage	-	-	0.63	V
V _{OH}	High-level output voltage	1.35	-	-	V
V _{OL}	Low-level output voltage	-	-	0.45	V

5.5 Current Consumption (V_{BAT}=3.9V)

Table 26: Current consumption

Parameter	Conditions	Typ.	Max	Unit
Leakage current	Off mode	31		uA
	Flight mode	2.6		mA
Standby current	GSM@BS-PA-MFRMS=2	3.5		mA
	WCDMA @DRX=8	3.47		mA
	CDMA 1X @max slot=1~7	3.53		mA
	EVDO @max slot=1~7	3.17		mA
	TD-SCDMA @DRX=7	3.14		mA
	LTE-FDD @standby 1.28s	3.95		mA
	LTE-TDD @standby 1.28s	4.0		mA
	GSM Voice call	GSM850 @PCL5	259	
EGSM900 @PCL5		269		mA
DCS1800 @PCL0		224		mA
PCS1900 @PCL0		195		mA
WCDMA Voice call	Band 1 @max power	588		mA
	Band 2 @max power	562		mA
	Band 4 @max power	540		mA
	Band 5 @max power	504		mA
	Band 8 @max power	504		mA
FDD-LTE voice call	Band 1 @max power	583		mA
	Band 2 @max power	650		mA
	Band 3 @max power	680		mA
	Band 4 @max power	690		mA

		Band 5 @max power	520	mA
		Band 8 @max power	510	mA
		Band 12 @max power	550	mA
		Band 13 @max power	570	mA
		Band 17 @max power	600	mA
		Band 20 @max power	558	mA
		Band 25 @max power	620	mA
		Band 26 @max power	580	mA
TDD-LTE call	voice	Band 34 @max power	350	mA
		Band 38 @max power	326	mA
		Band 39 @max power	330	mA
		Band 40 @max power	428	mA
		Band 41 @max power	413	mA
GPRS data		GSM850 (1UL/4DL) @PCL5	251	mA
		GSM850 (2UL/3DL) @PCL5	446	mA
		GSM850 (4UL/1DL) @PCL5	577	mA
		GSM900 (1UL/4DL) @PCL5	253	mA
		GSM900 (2UL/3DL) @PCL5	461	mA
		GSM900 (4UL/1DL) @PCL5	616	mA
		DCS1800 (1UL/4DL) @PCL5	196	mA
		DCS1800 (2UL/3DL) @PCL5	344	mA
		DCS1800 (4UL/1DL) @PCL5	533	mA
		DCS1900 (1UL/4DL) @PCL5	178	mA
		DCS1900 (2UL/3DL) @PCL5	315	mA
		DCS1900 (4UL/1DL) @PCL5	500	mA
EDGE data		GSM850 (1UL/4DL) @PCL8	145	mA
		GSM850 (2UL/3DL) @PCL8	245	mA
		GSM850 (4UL/1DL) @PCL8	365	mA
		GSM900 (1UL/4DL) @PCL8	165	mA
		GSM900 (2UL/3DL) @PCL8	268	mA
		GSM900 (4UL/1DL) @PCL8	381	mA
		DCS1800 (1UL/4DL) @PCL2	157	mA
		DCS1800 (2UL/3DL) @PCL2	248	mA
		DCS1800 (4UL/1DL) @PCL2	420	mA
		DCS1900 (1UL/4DL) @PCL2	137	mA
		DCS1900 (2UL/3DL) @PCL2	235	mA
		DCS1900 (4UL/1DL) @PCL2	399	mA
LTE data		FDD Band1 @0dBm	294	mA
		FDD Band2 @0dBm	/	mA
		FDD Band3 @0dBm	296	mA
		FDD Band4 @0dBm	/	mA

	FDD Band5 @0dBm	231	mA
	FDD Band7 @0dBm	/	mA
	FDD Band8 @0dBm	234	mA
	FDD Band12 @0dBm	/	mA
	FDD Band13 @0dBm	/	mA
	FDD Band17 @0dBm	/	mA
	FDD Band25 @0dBm	/	mA
	FDD Band26 @0dBm	/	mA
	TDD Band34 @0dBm	314	mA
	TDD Band38 @0dBm	209	mA
	TDD Band39 @0dBm	231	mA
	TDD Band40 @0dBm	297	mA
	TDD Band41 @0dBm	210	mA
Peak current	Max power		3 A

5.6 Electro-Static Discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, it may result in destructive damage.

SIM8950x must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, Protection of Electrical and Electronic Parts, Assemblies, and Equipment.

Table 27: ESD performance parameters (Temperature: 25°C, Humidity: 45%)

Pin	Contact discharge	Air discharge
VBAT	±5KV	±10KV
GND	±6KV	±12KV
Antenna	±5KV	±10KV

5.7 Module Operating Frequencies

Table 28: Module operating frequencies

Frequency	Receive	Transmit	Physical channel
GSM850	869-894MHz	824-849MHz	128-251
EGSM900	925-960MHz	880-915MHz	0-124, 975-1023
DCS1800	1805-1880MHz	1710-1785MHz	512-885

PCS1900	1930-1990MHz	1850-1910MHz	512-810
WCDMA B1	2110-2170 MHz	1920-1980 MHz	TX: 9612-9888 RX: 10562-10838
WCDMA B2	1930-1990MHz	1850-1910MHz	TX: 9262-9538 RX: 9662-9938
WCDMA B4	2110-2155MHz	1710-1755MHz	TX: 1312-1862 RX: 1537-2087
WCDMA B5	869-894MHz	824-849MHz	TX: 4132-4233 RX: 4357-4458
WCDMA B8	925-960MHz	880-915 MHz	TX: 2712-2863 RX: 2937-3088
CDMA BC0	869-894MHz	824-849MHz	1-799 ;991-1023
TDSCDMA 1.9G	1880-1920 MHz	1880-1920MHz	9400-9600
TDSCDMA 2G	2010-2025 MHz	2010-2025MHz	10054-10121
LTE B1	2110-2170 MHz	1920-1980 MHz	TX: 18000-18599 RX: 0-599
LTE B2	1930-1990MHz	1850-1910MHz	TX: 18600-19199 RX: 600-1199
LTE B3	1805-1880 MHz	1710-1785 MHz	TX: 19200-19949 RX: 1200-1949
LTE B4	2110-2155MHz	1710-1755MHz	TX: 19950-20399 RX: 1950-2399
LTE B5	869-894 MHz	824-849MHz	TX: 20400-20649 RX: 2400-2649
LTE B7	2620-2690MHz	2500-2570MHz	TX: 20750-21449 RX: 2750-3449
LTE B8	925-960 MHz	880-915 MHz	TX: 21450-21799 RX: 3450-3799
LTE B12	729-746MHz	699-716MHz	TX: 23010-23179 RX: 5010-5179
LTE B13	746-756MHz	777-787MHz	TX: 23180-23279 RX: 5180-5279
LTE B17	734-746MHz	704-716MHz	TX: 23730-23849 RX: 5730-5849
LTE B20	791-821MHz	832-862MHz	TX: 24150-24449 RX: 6150-6449
LTE B25	1850-1915MHz	1930-1995MHz	TX: 26040-26689 RX:8040-8689
LTE B26	859-894MHz	814-849MHz	TX: 26690-27039 RX: 8690-9039
LTE B34	2010-2025 MHz	2010-2025 MHz	36200-36349
LTE B38	2570-2620 MHz	2570-2620 MHz	37750-38249
LTE B39	1880-1920 MHz	1880-1920 MHz	38250-38649
LTE B40	2300-2400 MHz	2300-2400 MHz	38650-39649
LTE B41	2555-2655 MHz	2555-2655MHz	40240-41240

5.8 Module Output power

Table 29: Conducted transmission power

Frequency	Power	Min.
GSM850	33dBm ±2dB	5dBm ± 5dB
E-GSM900	33dBm ±2dB	5dBm ± 5dB
DCS1800	30dBm ±2dB	0dBm ± 5dB
PCS1900	30dBm ±2dB	0dBm ± 5dB
GSM850(8-PSK)	27dBm ±3dB	5dBm ± 5dB
E-GSM900 (8-PSK)	27dBm ±3dB	5dBm ± 5dB
DCS1800 (8-PSK)	26dBm +3/-4dB	0dBm ±5dB
PCS1900(8-PSK)	26dBm +3/-4dB	0dBm ±5dB
WCDMA B1	24dBm +1/-3dB	<-50dBm
WCDMA B2	24dBm +1/-3dB	<-50dBm
WCDMA B4	24dBm +1/-3dB	<-50dBm
WCDMA B5	24dBm +1/-3dB	<-50dBm
WCDMA B8	24dBm +1/-3dB	<-50dBm
CDMABC0	24dBm +1/-1dB	<-50dBm
TDSCDMA B34	24dBm +1/-3dB	<-50dBm
TDSCDMA B39	24dBm +1/-3dB	<-50dBm
LTE-FDD B1	23dBm +/-2.7dB	<-40dBm
LTE-FDD B2	23dBm +/-2.7dB	<-40dBm
LTE-FDD B3	23dBm +/-2.7dB	<-40dBm
LTE-FDD B4	23dBm +/-2.7dB	<-40dBm
LTE-FDD B5	23dBm +/-2.7dB	<-40dBm
LTE-FDD B7	23dBm +/-2.7dB	<-40dBm
LTE-FDD B8	23dBm +/-2.7dB	<-40dBm
LTE-FDD B12	23dBm +/-2.7dB	<-40dBm
LTE-FDD B13	23dBm +/-2.7dB	<-40dBm
LTE-FDD B17	23dBm +/-2.7dB	<-40dBm
LTE-FDD B20	23dBm +/-2.7dB	<-40dBm
LTE-FDD B25	23dBm +/-2.7dB	<-40dBm
LTE-FDD B26	23dBm +/-2.7dB	<-40dBm
LTE-TDD B34	23dBm +/-2.7dB	<-40dBm
LTE-TDD B38	23dBm +/-2.7dB	<-40dBm
LTE-TDD B39	23dBm +/-2.7dB	<-40dBm
LTE-TDD B40	23dBm +/-2.7dB	<-40dBm
LTE-TDD B41	23dBm +/-2.7dB	<-40dBm

5.9 Module Receiving Sensitivity

Table 30: Conducted receiving sensitivity

Band	Receiving sensitivity (Typ)	Receiving sensitivity (Max)
GSM850	< -108dBm	3GPP standard
EGSM900	< -108dBm	3GPP standard
DCS1800	< -108dBm	3GPP standard
PCS1900	< -108dBm	3GPP standard
WCDMA B1	<-109dBm	3GPP standard
WCDMA B2	<-109dBm	3GPP standard
WCDMA B4	<-109dBm	3GPP standard
WCDMA B5	<-109dBm	3GPP standard
WCDMA B8	<-109dBm	3GPP standard
CDMA BC0	<-109dBm	3GPP standard
TDSCDMA B34	<-110dBm	3GPP standard
TDSCDMA B39	<-110dBm	3GPP standard
LTE FDD/TDD	See Table 31	3GPP standard

Table 31: Reference sensitivity QPSK PREFSENS (LTE)

E-UTRA Band number	1.4 MHz	3 MHz	5 MHz	10 MHz	15 MHz	20 MHz	Duplex mode
1	-	-	-100	-97	-95.2	-94	FDD
2	-102.7	-99.7	-98	-95	-93.2	-92	FDD
3	-101.7	-98.7	-97	-94	-92.2	-91	FDD
4	-104.7	-101.7	-100	-97	-95.2	-94	FDD
5	-103.2	-100.2	-98	-95			FDD
6	-	-	-100	-97			FDD
7	-	-	-98	-95	-93.2	-92	FDD
8	-102.2	-99.2	-97	-94			FDD
9	-	-	-99	-96	-94.2	-93	FDD
10	-	-	-100	-97	-95.2	-94	FDD
11	-	-	-100	-97			FDD
12	-101.7	-98.7	-97	-94			FDD
13			-97	-94			FDD
14		-	-97	-94			FDD
17	-	-	-97	-94			FDD

18	-	-	-100	-97	-95.2	-	FDD
19	-	-	-100	-97	-95.2	-	FDD
20			-97	-94	-91.2	-90	FDD
21			-100	-97	-95.2		FDD
22			-97	-94	-92.2	-91	FDD
23	-104.7	-101.7	-100	-97			FDD
24			-100	-97			FDD
25	-101.2	-98.2	-96.5	-93.5	-91.7	-90.5	FDD
26	-102.7	-99.7	-97.5	-94.5	-92.7		FDD
33	-	-	-100	-97	-95.2	-94	TDD
34	-	-	-100	-97	-95.2	-	TDD
35	-106.2	-102.2	-100	-97	-95.2	-94	TDD
36	-106.2	-102.2	-100	-97	-95.2	-94	TDD
37	-	-	-100	-97	-95.2	-94	TDD
38	-	-	-100	-97	-95.2	-94	TDD
39	-	-	-100	-97	-95.2	-94	TDD
40	-	-	-100	-97	-95.2	-94	TDD
41	-	-	-99	-96	-94.2	-93	TDD
42	-	-	-99	-96	-94.2	-93	TDD
43	-	-	-99	-96	-94.2	-93	TDD

5.10 WIFI main RF Characteristics

Table 32: 2.4G WIFI main RF Characteristics

Transmission performance				
	802.11B(11M)	802.11G(54M)	802.11N(MCS7)	
Output power	17dBm±1dB	13dBm±1dB	12dBm±1dB	
EVM	<35%	<-25dB	<-27dB	
Receiving performance				
	802.11B(11M)	802.11G(54M)	802.11N(MCS7)	
Receiving sensitivity	<-88	<-73	<-71	dBm

Table 33: 5G WIFI main RF Characteristics

Transmission performance			
	802.11A (54M)	802.11N (MCS7)	802.11AC (MCS9)
Output power	17dBm±1dB	16dBm±1dB	14dBm±1dB
EVM	<-25	<-27	<-30
			dB
Receiving performance			
	802.11A (54M)	802.11N (MCS7)	802.11AC (MCS9)
Receiving sensitivity	<-71	<-70	<-64
			dBm

5.11 BT Main RF Characteristics

Table 34: BT Main RF Characteristics

Transmission performance			
	DH5	2DH5	3DH5
Output power	9dBm±1dB	7dBm±1dB	7dBm±1dB
Receiving performance			
	DH5	2DH5	3DH5
Receiving sensitivity	<-90	<-80	<-80
			dBm

5.12 GNSS Main RF Characteristics

Table 35: GNSS Main RF Characteristics

Receiver type	GPS, GLONASS, BEIDOU	
CNO	40dB/Hz@-130dBm	
Accuracy (Open Sky)	2.5m (CEP50)	
Sensitivity	Tracking & Navigation	-159dBm
	Reacquisition	-156dBm
	Cold start	-148dBm
TTFF(Open Sky)	Cold start	<35s
	Warm start	<15s
	Hot start	<5s

6. Manufacturing

6.1 Top and Bottom View of SIM8950x

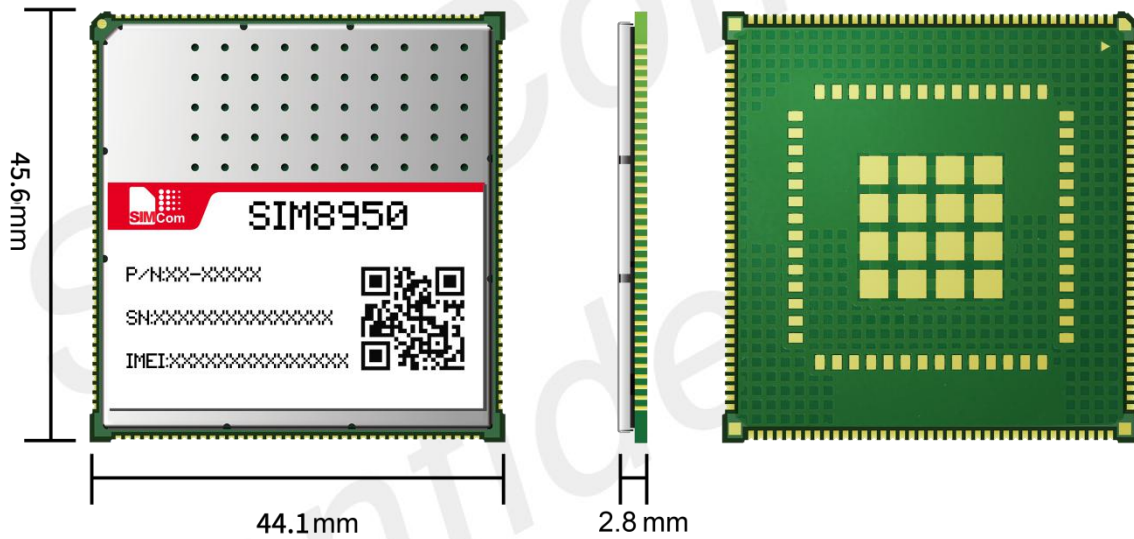


Figure 36: Top and bottom view of SIM8950x

6.2 Physical Dimensions

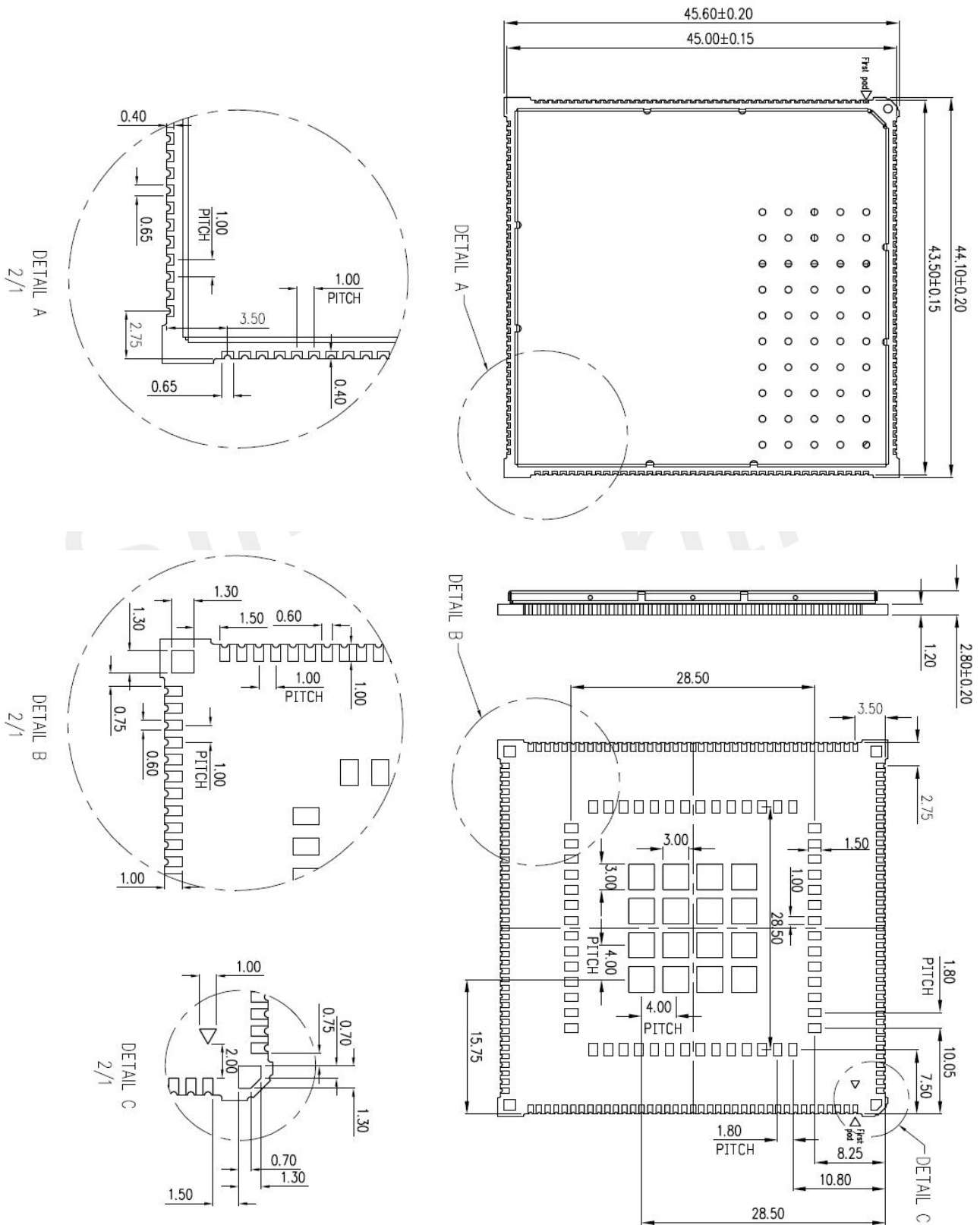


Figure 37: Outline drawing (unit: mm)

6.3 Recommended PCB footprint

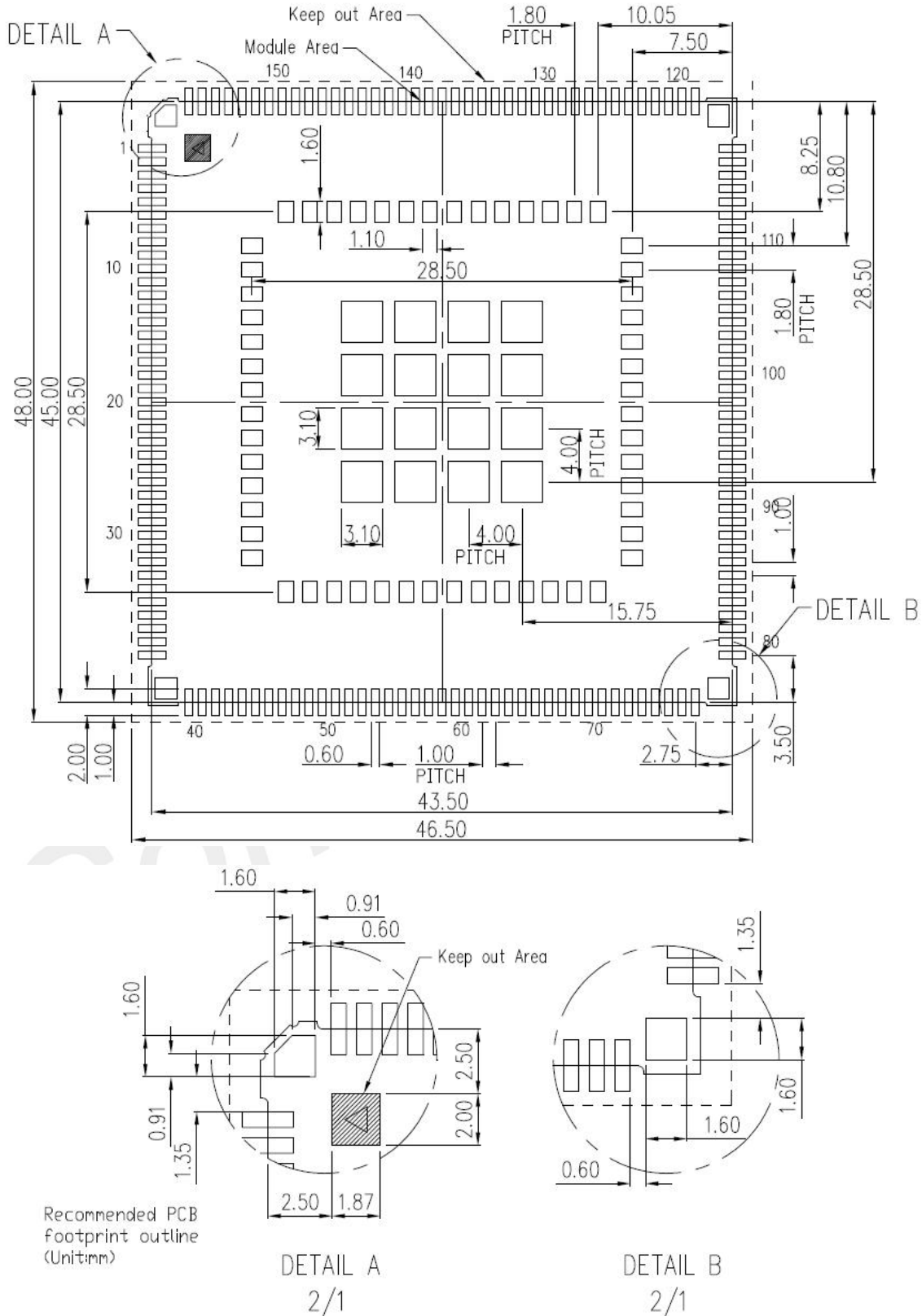


Figure 38: Recommended PCB footprint

6.4 Recommended SMT Stencil

Stencil thickness requirement:

- The stencil thickness of outer circle's pin need 0.18mm
- The stencil thickness of inner pin need reduce, recommend 0.15mm.

Recommended SMT stencil:

1, Outer pin (units: mm):

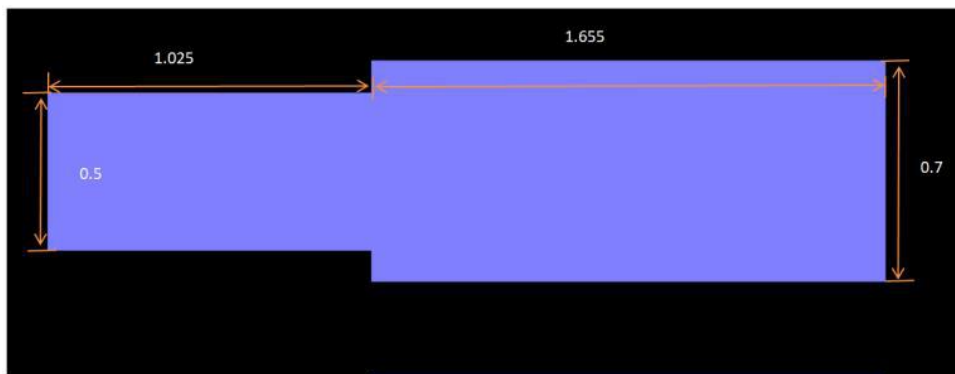


Figure 39: Outer PIN recommended stencil

2, Inner function pin (units: mm):

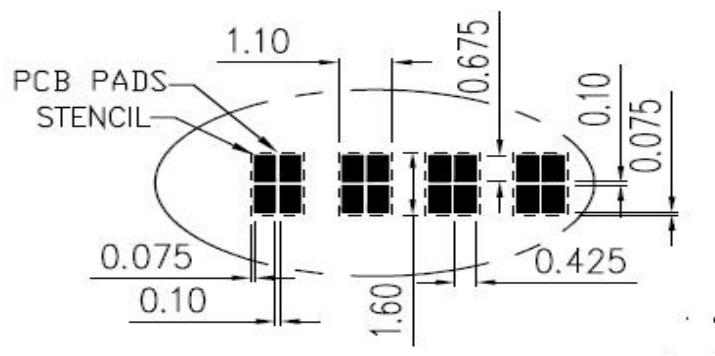


Figure 40: Inner function PIN recommended stencil

3, Inner GND pin(units: mm):

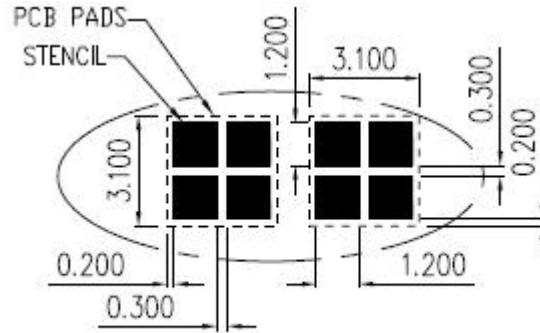


Figure 41: Inner GND PIN recommended stencil

NOTE

The SMT stencil of Inner PIN need cross design.

6.5 Typical SMT Reflow Profile

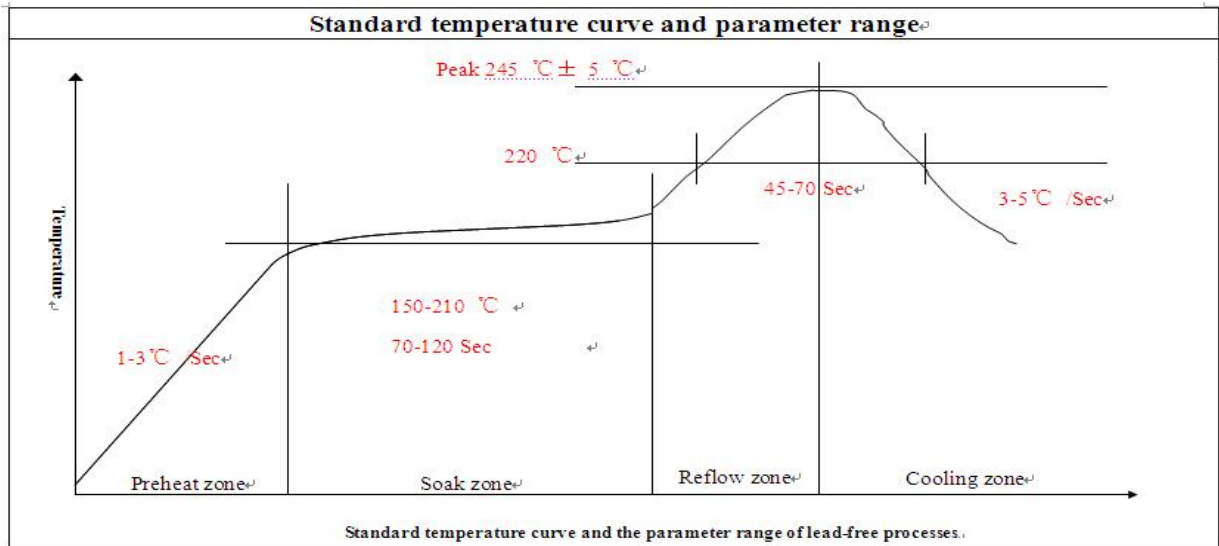


Figure 42: Typical SMT reflow profile

NOTE

Refer to “Module secondary-SMT-UGD” for more information about the module shipping and manufacturing.

6.6 Moisture Sensitivity Level (MSL)

SIM8950x is susceptible to damage induced by absorbed moisture and high temperature. A package’s moisture-sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in Table 36.

Table 36: MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤+30°C/85% RH

2	1 year	≤+30°C/60% RH
2a	4 weeks	≤+30°C/60% RH
3	168 hours	≤+30°C/60% RH
4	72 hours	≤+30°C/60% RH; SIM8950x rating
5	48 hours	≤+30°C/60% RH
5a	24 hours	≤+30°C/60% RH
6	Mandatory bake before use. After bake, it must be reflowed within the time limit specified on the label.	≤+30°C/60% RH

The MSM8909 device samples are currently classified as **MSL4** at 255 (+5, -0)°C, following the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. This qualification temperature (255°C) should not be confused with the peak temperature within the recommended solder reflow profile.

6.7 Baking Requirements

It is necessary to bake modules if the prescribed time limit has been exceeded. The baking conditions are specified in Table 37. Note that if baking is required, the devices must be transferred into trays that can be baked to at least 125°C.

Table 37: Baking requirements

Baking conditions options	Duration
40°C±5°C, <5% RH	192 hours
120°C±5°C, <5% RH	4 hours

7. Packaging

SIM8950x module supports tray packaging. The packaging process is shown in the following figures.

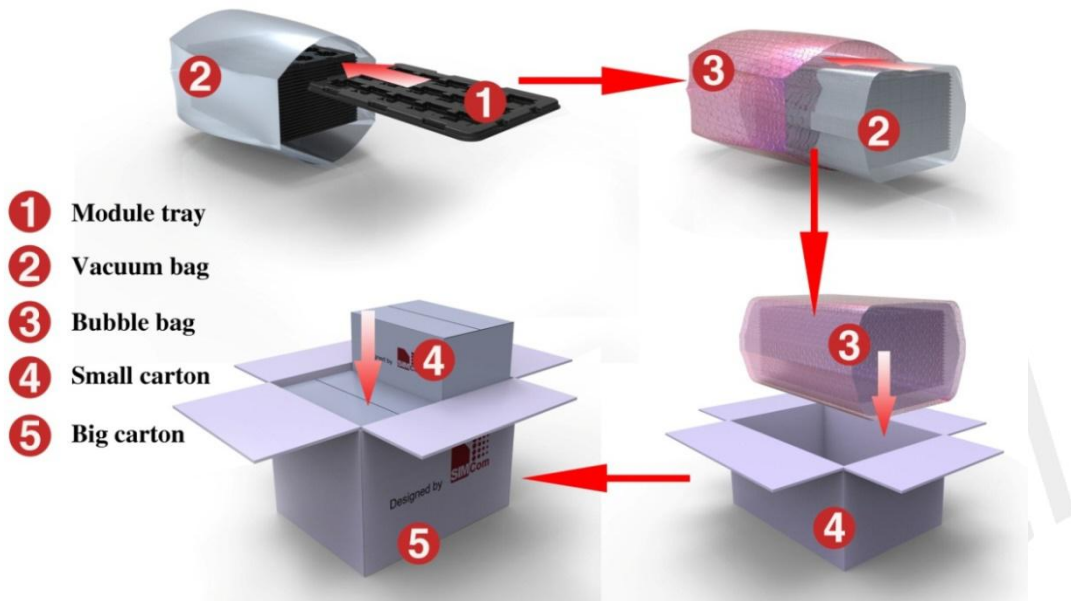


Figure 43: Packaging process

Module tray drawing:

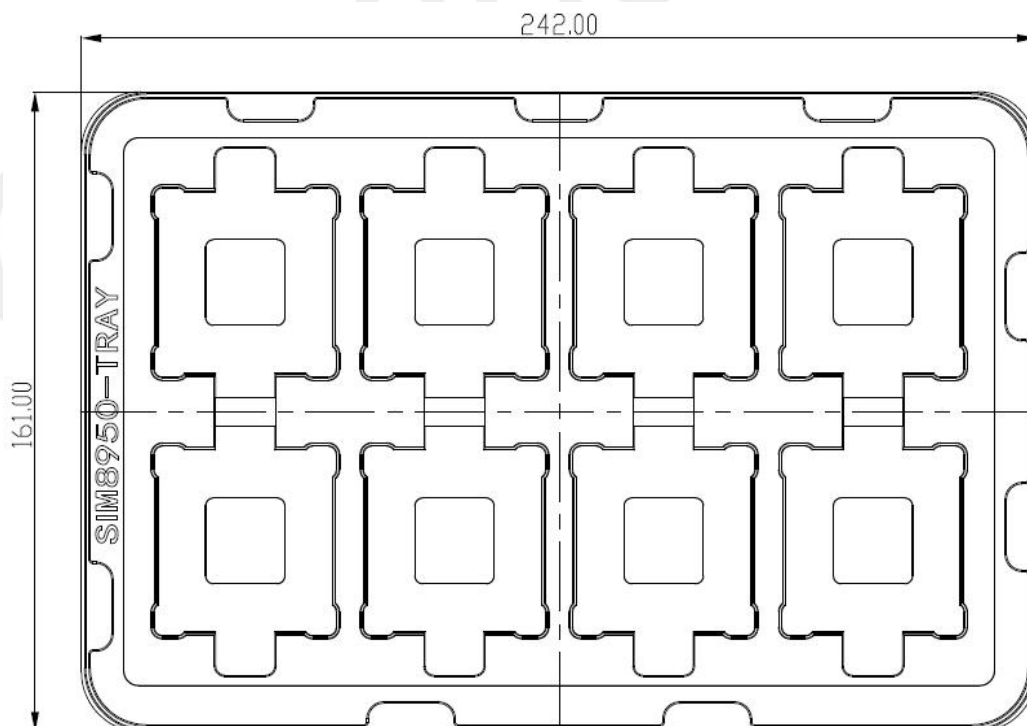


Figure 44: Module tray drawing

Table 38: Module tray information

Length ($\pm 3\text{mm}$)	Width ($\pm 3\text{mm}$)	Units per tray
242.0	161.0	8

Small carton drawing:

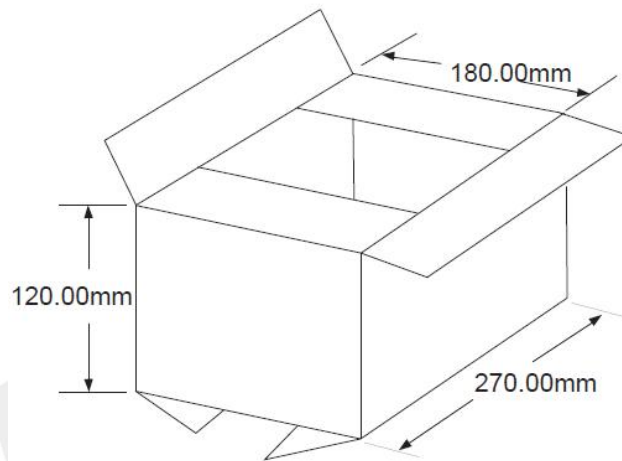


Figure 45: Small carton drawing

Table 39: Small carton information

Length ($\pm 10\text{mm}$)	Width ($\pm 10\text{mm}$)	Height ($\pm 10\text{mm}$)	Units per carton
270	180	120	$8 \times 19 - 2 = 150$

Big carton drawing:

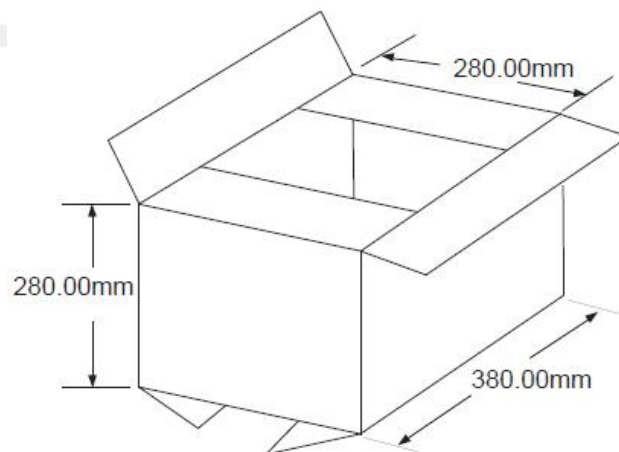


Figure 46: Big carton drawing

Table 40: Big carton information

Length ($\pm 10\text{mm}$)	Width ($\pm 10\text{mm}$)	Height ($\pm 10\text{mm}$)	Units per carton
380	280	280	150*4=600

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8. Recommend Peripheral Component list

Table 41: Recommended Camera Sensor List

	Resolution	Sensor Part Nmuber	Sensor Vendor
Primary camera/ Secondary camera	2M	OV2680	OmniVision
	5M	OV5675	OmniVision
		OV5695	OmniVision
		S5K5E8	SAMSUNG
	8M	OV8856	OmniVision
		OV8858	OmniVision
		OV8865	OmniVision
S5K4H8		SAMSUNG	
Primary camera	12M	OV12890	OmniVision
		S5K2L7	SAMSUNG
		IMX362	SONY
	13M	AR1337	ON Semiconductor
		OV13853(PDAF)	OmniVision
		OV13855	OmniVision
		OV13870	OmniVision
		MN34153	Panasonic
		S5K2M8	SAMSUNG
		S5K3M2XM(PDAF)	SAMSUNG
	16M	IMX258(PDAF)	SONY
		OV16860	OmniVision
		OV16880	OmniVision
S5K2P7		SAMSUNG	
S5K3P3		SAMSUNG	
S5K3P8		SAMSUNG	
20M	IMX298 (PDAF)	SONY	
	20M	IMX230	SONY

Table 42: Recommended LCD Driver IC List

LCD Driver IC	Vendor	Resolution
OTM1902A	FocalTech	FHD
OTM1906C	FocalTech	FHD
HX8399-C	Himax	FHD
ILI7807E	Ilitek	FHD
ILI9885	Ilitek	FHD
NT35532	Novatek	FHD
NT35596	Novatek	FHD
NT35695	Novatek	FHD
R63417	SYNAPTICS	FHD

Table 43: Recommended Accelerometer & Gyroscope List

No.	Part Number	Vendor	Accelerometer	Gyroscope
1	BMA222E	Bosch	√	√
2	BMA250E	Bosch	√	√
3	BMA253	Bosch	√	√
4	BMA255	Bosch	√	√
5	BMA421	Bosch	√	
6	BMA422	Bosch	√	
7	BMA424	Bosch	√	
8	BMG160	Bosch		√
9	BMI120	Bosch	√	√
10	BMI160	Bosch	√	√
11	BMI260	Bosch	√	√
12	ICM-20600	InvenSense	√	√
13	ICM-20602	InvenSense	√	√
14	ICM-20607	InvenSense	√	√
15	ICM-20608-D	InvenSense	√	√
16	ICM-20608-G	InvenSense	√	√
17	ICM-20609	InvenSense	√	√
18	ICM-20621	InvenSense	√	√
19	ICM-20622	InvenSense	√	√
20	ICM-20690	InvenSense	√	√
21	ICM-40602	InvenSense	√	√
22	ICM-40604	InvenSense	√	√

23	ICM-40605	InvenSense	√	√
24	ICM-42602	InvenSense	√	√
25	ICM-42605	InvenSense	√	√
26	ICM-42605-M	InvenSense	√	√
27	ICM-42608	InvenSense	√	√
28	MPU-6500	InvenSense	√	√
29	MPU-6881	InvenSense	√	√
30	KX022-1020	Kionix	√	
31	KX023-1025	Kionix	√	
32	KX122-1037	Kionix	√	
33	KXTJ2-1009	Kionix	√	
34	KXTJ2-1029	Kionix	√	
35	KXTJ3	Kionix	√	
36	MC3413-P	mCube	√	
37	MC3416-P	mCube	√	
38	MXC4005XC	MEMSIC	√	
39	STK8BA53	Sensortek	√	
40	LIS2DH12TR	ST	√	
41	LIS2DS12TR	ST	√	
42	LIS2HH12	ST	√	
43	LIS3DH	ST	√	
44	LIS3DHTR	ST	√	
45	LSM6DS3TR	ST	√	√
46	LSM6DS3TR-C	ST	√	√
47	LSM6DSLTR	ST	√	√
48	LSM6DSMTR	ST	√	√

Table 44: Recommended E-Compass List

No.	Part Number	Vendor
1	AK09911C	AKM
2	AK09915C	AKM
3	AK09915D	AKM
4	AK09916C	AKM
5	AK09918C	AKM
6	HSCDTD008A	Alps
7	BMM150	Bosch
8	GMC306	Globalmems
9	IST8305	iSentek
10	IST8306	iSentek

11	IST8307	iSentek
12	IST8310	iSentek
13	MXG4300	MagnaChip
14	MMC3530	MEMSIC
15	MMC3630	MEMSIC
16	MMC3630KJ	MEMSIC
17	MMC5603NJ	MEMSIC
18	STM350MC	Senodia
19	STM480MW	Senodia
20	LIS2MDL	ST
21	AF6133	Voltafield
22	AF6133E	Voltafield
23	AF8133J	Voltafield
24	AF9133	Voltafield
25	YAS539	Yamaha

Table 45: Recommended Proximity & Ambient Light List

No.	Part Number	Vendor	Proximity	Ambient Light
1	TMD26203	ams	√	
2	CM36686	Capella	√	√
3	AP3426	Dyna Image	√	√
4	EPL2590KTWJP	Elan	√	√
5	MN66213	Elan	√	√
6	LTR-578ALS	Lite-On	√	√
7	BH1745NUC	ROHM		√
8	RPR-0521RS	ROHM	√	√
9	RPR-0531	ROHM	√	√
10	RPR-0531RS	ROHM	√	√
11	STK3321	Sensortek	√	√
12	PA12200001	TXC	√	√
13	PA22401001	TXC	√	
14	PA22A00001	TXC	√	√
15	TMD26203	ams	√	

9. Appendix

a) Related Documents

Table 46: Related Documents

No.	Document name	Remark
[1]	GSM 07.07:	Digital cellular telecommunications (Phase 2+); AT command set for GSM Mobile Equipment (ME)
[2]	GSM 07.10:	Support GSM 07.10 multiplexing protocol
[3]	GSM 07.05:	Digital cellular telecommunications (Phase 2+); Use of Data Terminal Equipment – Data Circuit terminating Equipment (DTE – DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)
[4]	GSM 11.14:	Digital cellular telecommunications system (Phase 2+); Specification of the SIM Application Toolkit for the Subscriber Identity Module – Mobile Equipment (SIM – ME) interface
[5]	GSM 11.11:	Digital cellular telecommunications system (Phase 2+); Specification of the Subscriber Identity Module – Mobile Equipment (SIM – ME) interface
[6]	GSM 03.38:	Digital cellular telecommunications system (Phase 2+); Alphabets and language-specific information
[7]	GSM 11.10	Digital cellular telecommunications system (Phase 2); Mobile Station (MS) conformance specification; Part 1: Conformance specification
[8]	3GPP TS 51.010-1	Digital cellular telecommunications system (Release 5); Mobile Station (MS) conformance specification
[9]	3GPP TS 34.124	Electromagnetic Compatibility (EMC) for mobile terminals and ancillary equipment.
[10]	3GPP TS 34.121	Electromagnetic Compatibility (EMC) for mobile terminals and ancillary equipment.
[11]	3GPP TS 34.123-1	Technical Specification Group Radio Access Network; Terminal conformance specification; Radio transmission and reception (FDD)
[12]	3GPP TS 34.123-3	User Equipment (UE) conformance specification; Part 3: Abstract Test Suites.
[13]	EN 301 908-02 V2.2.1	Electromagnetic compatibility and Radio spectrum Matters (ERM); Base Stations (BS) and User Equipment (UE) for IMT-2000. Third Generation cellular networks; Part 2: Harmonized EN for IMT-2000, CDMA Direct Spread (UTRA FDD) (UE) covering essential requirements of article 3.2 of the R&TTE Directive

[14]	EN 301 489-24 V1.2.1	Electromagnetic compatibility and Radio Spectrum Matters (ERM); Electromagnetic Compatibility (EMC) standard for radio equipment and services; Part 24: Specific conditions for IMT-2000 CDMA Direct Spread (UTRA) for Mobile and portable (UE) radio and ancillary equipment
[15]	IEC/EN60950-1(2001)	Safety of information technology equipment (2000)
[16]	GCF-CC V3.23.1	Global Certification Forum - Certification Criteria
[17]	2002/95/EC	Directive of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS)

b) Terms and abbreviations

Table 47: Terms and abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-Rate
BOM	Bill of materials
bps	Bits per second
BT	Bluetooth
CDMA	Code division multiple access
CS	Coding Scheme
CSD	Circuit Switched Data
CSI	Camera serial interface
CTS	Clear to Send
DAC	Digital-to-analog converter
DDR	Double data rate
DSDA	Dual SIM dual active
DSDS	Dual SIM dual standby
DSP	Digital signal processor
DTE	Data Terminal Equipment (typically computer, terminal, printer)
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
ESD	Electrostatic Discharge
ESR	Effective series resistance
ETS	European Telecommunication Standard
EVDO	Evolution data optimized

FDD	Frequency division duplex
FR	Full Rate
GNSS	Global navigation satellite system
GPIO	General-purpose input/output
GPRS	General Packet Radio Service
GPU	Graphics processing unit
GSM	Global Standard for Mobile Communications
HR	Half Rate
HSPA	High-speed packet access
I2C	Inter-integrated circuit
IMEI	International Mobile Equipment Identity
ISP	Image signal processing
Kbps	kilobits per second
LCD	Liquid crystal display
LDO	Low dropout (linear regulator)
LPDDR	Low-power DDR
MIC	Microphone
MIPI	Mobile industry processor interface
PA	Power amplifier
PBCCH	Packet Broadcast Control Channel
PCB	Printed Circuit Board
PCL	Power Control Level
PCS	Personal Communication System, also referred to as GSM 1900
PDU	Protocol Data Unit
RF	Radio Frequency
PM	Power management
RoHS	Restriction of hazardous substances
PPP	Point-to-point protocol
PWM	Pulse-width modulator
RMS	Root Mean Square (value)
RTC	Real-time clock
RX	Receive Direction
SD	Secure digital
SDC	Secure digital controller
SIM	Subscriber Identification Module
SMS	Short Message Service
SMT	Surface mount technology
SPI	Serial peripheral interface
TDD	Time Division Distortion
TE	Terminal Equipment, also referred to as DTE
TX	Transmit Direction

UART	Universal Asynchronous Receiver & Transmitter
UIM	User Identity module
URC	Unsolicited Result Code
USB	Universal serial bus
USSD	Unstructured Supplementary Service Data
WCDMA	Wideband code division multiple access
WCN	Wireless connectivity network
WLAN	Wireless local area network

Pay attention to the following safety precautions when using or maintaining any terminal or mobile phone that contains the module. Inform the users of the following security information on the terminal device. Otherwise SIMCom will not bear any consequences resulting from the users' not operating according to these warnings.

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c) Safety Caution

Pay attention to the following safety precautions when using or maintaining any terminal or mobile phone that contains the module. Inform the users of the following security information on the terminal device. Otherwise SIMCom will not bear any consequences resulting from the users' not operating according to these warnings.

Table 48: Safety Caution

Marks	Requirements
	<p>When in a hospital or other health care facility, observe the restrictions about the use of mobiles. Switch the cellular terminal or mobile off, medical equipment may not operate normally because of RF energy interference.</p>
	<p>Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. Ignoring of these instructions may lead to flight accident or offend against local legal, or both.</p>
	<p>Do not operate the cellular terminal or mobile in the presence of flammable gases or fumes. Switch off the cellular terminal when you are near petrol stations, fuel depots, chemical plants or where blasting operations are in progress. Operation of any electrical equipment in potentially explosive atmospheres can constitute a safety hazard.</p>
	<p>The cellular terminal or mobile receives and transmits radio frequency energy while switched on. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.</p>
	<p>Road safety comes first! Do not use a hand-held cellular terminal or mobile when driving a vehicle, unless it is securely mounted in a holder for hands free operation. Before making a call with a hand-held terminal or mobile, park the vehicle.</p>
	<p>GSM cellular terminals or mobiles operate over radio frequency signals and cellular networks and cannot be guaranteed to connect in all conditions, for example, no mobile fee or an invalid SIM card. While you are in this condition and need emergent help, please remember using emergency calls. In order to make or receive calls, the cellular terminal or mobile must be switched on and in a service area with adequate cellular signal strength. Some networks do not allow emergency calls if certain network services or phone features are in use (e.g. lock functions, fixed dialing, etc.). You may have to deactivate those features before you can make an emergency call. Also, some networks require that a valid SIM card be properly inserted in the cellular terminal or mobile.</p>