



SIM8905 Series Smart Module SPI Configure Guide

Version: 2.02

Release Date: April 9, 2019

About Document

Document Information

Document	
Title	SIM8905 Series Smart Module SPI Configure Guide
Version	2.02
Document Type	Application Note
Document Status	Released/Confidential

Revision History

Revision	Date	Owner	Status / Comments
1.00	April 8, 2018	Cheng.Zhou	First Release.
2.00	May 14,2018	Liuyuan.Zhang	Second Release.
2.02	April 9, 2019	Liuyuan	Third Release.

Related Documents

This document applies to the following products:

Name	Type	Size (mm)	Comments
SIM8905A/E/AU	Smart Module	40.5*40.5*2.8	N/A

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1 Purpose of this document

SPI allows full duplex / half duplex synchronous serial communication between main and slave ports. There is no explicit communication group frame, error checking, or defined data word length.

Main functions:

1. support up to up to 48MHz
2. support the transmission of 4-32 bit word length
3. at most support, there are four chip selection on each bus (CS).
4. support BAM.

This document directs how to configure SPI for SIM8905 series smart module.

2 SPI Configure Process

2.1 Configure Dts File

Adding a new SPI bus is mainly to modify DTS file, and to add driver file. In SIM8905 series smart module, QUP (Qualcomm universal peripheral (serial)) can be configures as SPI. Each QUP is identified by BLSP core and the QUP core.

Base address

BLSP Hardware ID	QUP core	Physical address
BLSP1	BLSP 1 QUP1	0x78B5000
BLSP1	BLSP 1 QUP2	0x78B6000
BLSP1	BLSP 1 QUP3	0x78B7000
BLSP1	BLSP 1 QUP4	0x78B8000
BLSP1	BLSP 1 QUP5	0x78B9000
BLSP1	BLSP 1 QUP6	0x78BA000

For example, adding a new SPI 0, The first step is to check hardware schematic and if the SPI0_MOSI, SPI0_MISO, SPI0_CLK, SPI0_CS are corresponding to GPIO8, GPIO9, GPIO11, GPIO10, the following file can be modified as: :

/kernel/arch/arm/boot/dts/qcom/msm8909.dtsi

```
spi_0: spi@78b7000 { /* BLSP1 QUP3 */
    compatible = "qcom,spi-qup-v2";
    #address-cells = <1>;
    #size-cells = <0>;
```

```

reg-names = "spi_physical", "spi_bam_physical";
reg = <0x78b7000 0x600>,
      <0x7884000 0x23000>;
interrupt-names = "spi_irq", "spi_bam_irq";
interrupts = <0 97 0>, <0 238 0>;
spi-max-frequency = <19200000>;
pinctrl-names = "default", "sleep", "cs_default";
pinctrl-0 = <&spi0_default>;
pinctrl-1 = <&spi0_sleep>;
pinctrl-2 = <&spi0_cs_sleep>;
clocks = <&clock_gcc clk_gcc_blspl1_ahb_clk>,
         <&clock_gcc clk_gcc_blspl1_qup1_spi_apps_clk>;
clock-names = "iface_clk", "core_clk";
qcom,infinite-mode = <0>;
qcom,use-bam;
qcom,use-pinctrl;
qcom,ver-reg-exists;
qcom,bam-consumer-pipe-index = <8>;
qcom,bam-producer-pipe-index = <9>;
qcom,master-id = <86>;
status = "ok";
};

```

2.2 Configure SPI GPIO File

In order to configure SPI GPIOs, the following file can be modified as:

kernel/arch/arm/boot/dts/qcom/msm8909-pinctrl.dtsi

```

spi0_active {
    /* MOSI, MISO, CLK */
    qcom,pins = <&gp 8>, <&gp 9>, <&gp 11>;
    qcom,num-grp-pins = <3>;
    qcom,pin-func = <1>;
    label = "spi0-active";
    /* active state */
    spi0_default:default {
        drive-strength = <12>; /* 12 MA */
        bias-disable = <0>; /* No PULL */
    };
};

spi0_suspend {
    /* MOSI, MISO, CLK */
    qcom,pins = <&gp 8>, <&gp 9>, <&gp 11>;
    qcom,num-grp-pins = <3>;
    qcom,pin-func = <0>;
};

```

```
label = "spi0-suspend";  
/* suspended state */  
spi0_sleep:sleep {  
drive-strength = <2>; /* 2 MA */  
bias-disable = <0>; /* No PULL */  
};  
};
```

```
spi0_cs0_active {  
/* CS */  
qcom,pins = <&gp 10>;  
qcom,num-grp-pins = <1>;  
qcom,pin-func = <1>;  
label = "spi0-cs0-active";  
spi0_cs0_active:cs0_active {  
drive-strength = <2>;  
bias-disable = <0>;  
};  
};
```

```
spi0_cs0_suspend {  
/* CS */  
qcom,pins = <&gp 10>;  
qcom,num-grp-pins = <1>;  
qcom,pin-func = <0>;  
label = "spi0-cs0-suspend";  
spi0_cs0_sleep:cs0_sleep {  
drive-strength = <2>;  
bias-disable = <0>;  
};  
};
```

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