UZ2400

Low Power 2.4 GHz Transceiver for IEEE 802.15.4 Standard

Datasheet

DS-2400-02

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UZ2400

Low Power 2.4 GHz Transceiver for IEEE 802.15.4 Standard

Applications

- Automated meter reading (AMR)
- Home/Building/Factory automations
- 2-way low data rate applications
- Wireless sensor network
- PC peripherals
- Low power wireless communications
- Consumer electronics

Introduction

The UZ2400 is a solution that complies with the IEEE 802.15.4/ZigBee specifications. It integrates a wireless RF transceiver operating at 2.4 GHz with 802.15.4 compliant baseband and MAC layer function blocks. UZ2400 can be combined with a microprocessor (e.g. 8051) for low data rate applications such as home automation, consumer electronics, PC peripherals, toys, industrial automation, etc. The RF block of UZ2400 integrates receiver, transmitter, VCO and PLL within a single IC. It uses advanced radio architecture to minimize the external component count and the power consumption. UZ2400 MAC/Baseband provides the hardware architecture for both the 802.15.4 MAC and the PHY layers. It mainly consists of TX/RX FIFOs, CSMA-CA controller, Superframe constructor, receiving frame filter, security engine and digital signal processing module. The UZ2400 is fabricated with advanced 0.18μm CMOS process and is sealed in a 40-pin QFN 6x6 mm^2 package.

Features

RF/Analog

- ISM band 2.405~2.480 GHz operation
- Complete IEEE 802.15.4-2003 specification compliance
- -95 dBm sensitivity and 5 dBm maximum input level
- 0 dBm typical output power and 36 dB TX power control range
- Differential RF input/output and integrated TX/RX switch
- Integrated low phase noise VCO, frequency synthesizer and PLL loop filter
- Integrated 20 MHz and 32.768KHz oscillator drive.
- Integrated 100kHz internal oscillator circuit
- Digital VCO and filter calibration
- Integrated RSSI ADC and I/Q DACs
- Integrated LDO
- High receiver and RSSI dynamic range
- Support power saving modes
- Low current consumption, 18 mA in RX and 22

mA in TX mode
- ❑ 2 uA deep sleep mode
- ❑ Small 40-pin leadless QFN 6x6 mm^2 package
- ❑ 0.18 µm CMOS technology
- ❑ Low external component count
- ❑ 625kbps turbo mode supported

MAC/Baseband

- ❑ Complete IEEE 802.15.4-2003 specification compliance
- ❑ Hardware CSMA-CA mechanism, automatic ACK response and FCS check
- ❑ Programmable Superframe construction
- ❑ Independent beacon, transmit and GTS FIFO
- ❑ Hardware security engine(AES-128) with CTR, CCM and CBC-MAC modes
- ❑ Four low power operation modes
- ❑ Support all CCA modes and RSSI/LQI
- ❑ Simple four-wire SPI interface
- ❑ I^{2}C slave supported

Block Diagram

Figure 1 shows the block diagram of UZ2400. UZ2400 is composed of six blocks:

- ❑ PHY block
- ❑ Lower MAC block
- ❑ Memory block
- ❑ Security engine block
- ❑ Power management block
- ❑ Interfacing block

Detailed descriptions for each block will be described in UZ2400 datasheet.

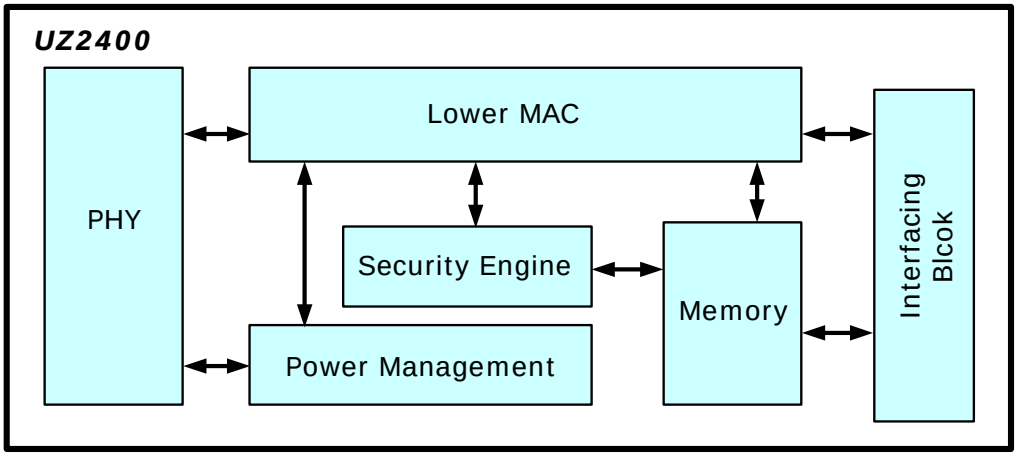

Figure 1 UZ2400 block diagram

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Abbreviations

ADC	Analog to Digital Converter
AES	Advanced Encryption Standard
AGC	Automation Gain Control
BER	Bit Error Rate
CBC-MAC	Cipher Block Chaining Message Authentication Code
CCA	Clear Channel Assessment
CCM	Counter Channel Mode
CSMA-CA	Carrier Sense Multiple Access with Collision Avoidance
CTR	Counter mode + CBC
CW	Continuous Wave
DSSS	Direct Sequence Spread Spectrum
ESD	Electronic Static Discharge
EVM	Error Vector Magnitude
FCC	Federal Communication Commission
FIFO	First In First Out
IEEE	Institute of Electrical and Electronics Engineers
ISM	Industrial Scientific and Medical
ITU-T	International Telecommunication Union - Telecommunication
I/O	Input / Output
I/Q	In – phase / Quadrature – phase
Kbps	Kilo bit per second
LNA	Low Noise Amplifier
LO	Local Oscillator
LQI	Link Quality Indication
LSB	Least Significant Bit / Byte
MSB	Most Significant Bit / Byte
MAC	Medium Access Control
MPDU	MAC Protocol Data Unit
MSDU	MAC Service Data Unit
NA	Not Available
NC	Not Connected
O-QPSK	Offset Quadrature Phase Shift Keying
PA	Power Amplifier
PCB	Printed Circuit Board
PHY	Physical Layer
PLL	Phase Locked Loop
PSDU	PHY Service Data Unit
QFN	Quad Flat No-lead Package
RF	Radio Frequency
RSSI	Receive Signal Strength Indicator
RX	Receive
SPI	Serial Peripheral Interface
TBD	To Be Defined

T/R	Transmit / Receive
TX	Transmit
VCO	Voltage Control Oscillator

1. Pin Configuration

1.1. Device Pin Assignments

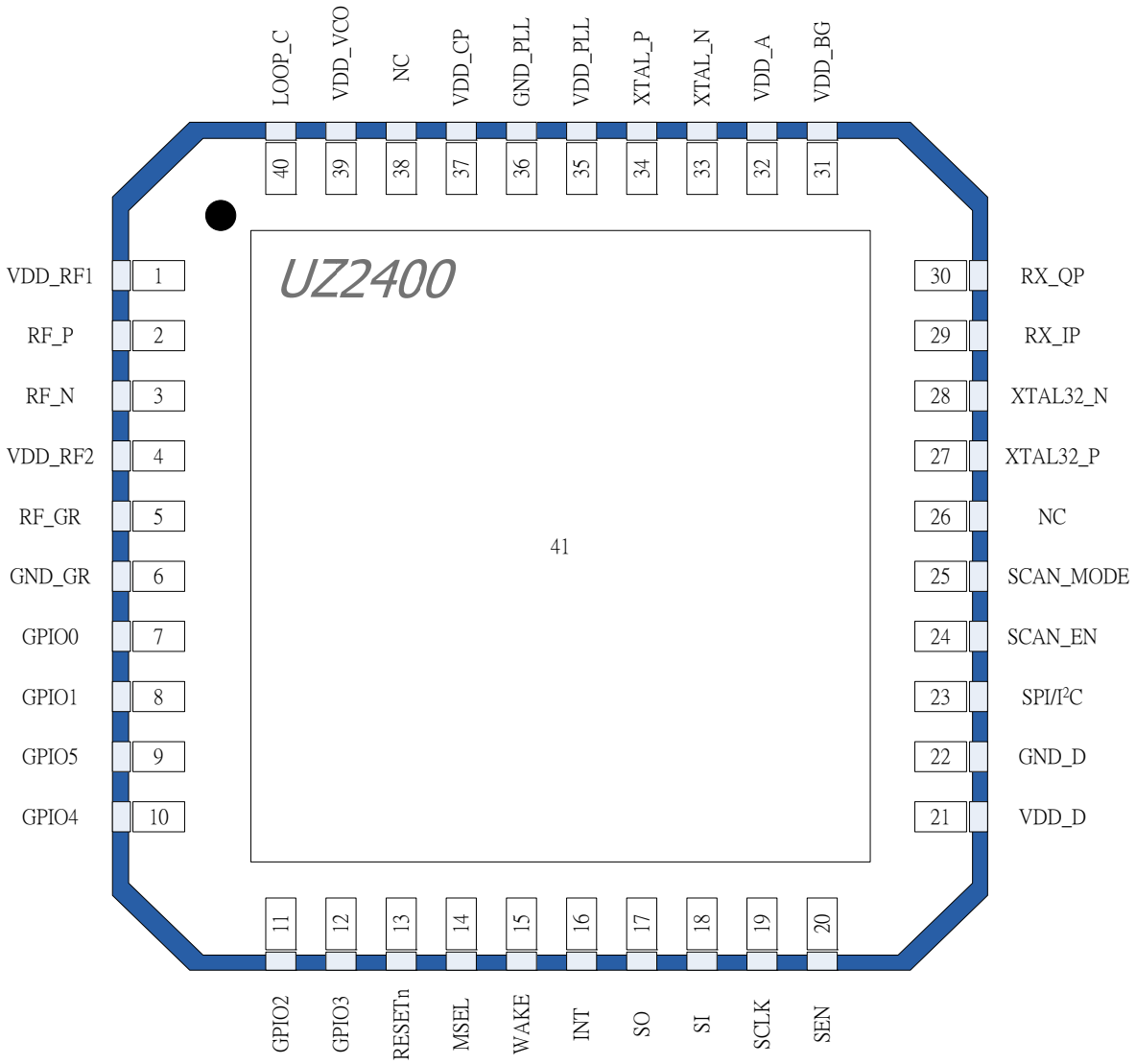


Figure 2. Pin assignments (top view)

1.2. Device Pin Descriptions

Pin type abbreviation: A = Analog, D = Digital, I = Input, O = Output

Pin	Symbol	Type	Description
1	VDD_RF1	Power	RF power supply. Bypass with a capacitor as close to the pin as possible.
2	RF_P*	AIO	Differential RF input/output (+)
3	RF_N*	AIO	Differential RF input/output (-)
4	VDD_RF2	Power	RF power supply. Bypass with a capacitor as close to the pin as possible.
5	VDD_GR*	Power	Guard ring power supply. Bypass with a capacitor as close to the pin as possible.
6	GND_GR	Ground	Guard ring ground
7	GPIO0	DIO	General purpose digital I/O, also used as an external PA enable
8	GPIO1	DIO	General purpose digital I/O, also used as an external TX/RX switch control
9	GPIO5	DIO	General purpose digital I/O
10	GPIO4	DIO	General purpose digital I/O
11	GPIO2	DIO	General purpose digital I/O, also used as an external TX/RX switch control
12	GPIO3	DIO	General purpose digital I/O
13	RESETn	DI	Global hardware reset pin, active low
14	MSEL	DI	SPI/memory interface selection
15	WAKE	DI	External wake up trigger
16	INT	DO	Interrupt pin to micro-processor
17	SO	DIO	Serial interface data output from UZ2400 or I^2C clock
18	SI	DIO	Serial interface data input to UZ2400 or I^2C data in/out
19	SCLK	DI	Serial interface clock
20	SEN	DI	Serial interface enable
21	VDD_D	Power	Digital circuit power supply
22	GND_D	Ground	Ground for digital circuit
23	SPI/I2C	DI	SPI or I^2C interface selection
24	SCAN_EN	DI	Scan insertion testing enable signal
25	SCAN_MODE	DI	Digital scan/test mode enable signal for chip testing purpose
26	NC		No connection (Do not connect power ground and signal)
27	XTAL32_P*	AI	32 kHz Crystal input (+)
28	XTAL32_N*	AI	32 kHz Crystal input (-)
29	RX_IP	AO	Analog RX I channel output (+)
30	RX_QP	AO	Analog RX Q channel output (+)
31	VDD_BG	Power	Power supply for bandgap reference circuit. Bypass with a capacitor as close to the pin as possible.

32	VDD_A	Power	Power supply for analog circuit. Bypass with a capacitor as close to the pin as possible.
33	XTAL_N	AI	20 MHz Crystal input (-)
34	XTAL_P	AI	20 MHz Crystal input (+)
35	VDD_PLL	Power	PLL power supply. Bypass with a capacitor as close to the pin as possible.
36	GND_PLL	Ground	Ground for PLL
37	VDD_CP	Power	Charge pump power supply. Bypass with a capacitor as close to the pin as possible.
38	NC		No connection
39	VDD_VCO	Power	VCO supply. Bypass with a capacitor as close to the pin as possible.
40	LOOP_C		PLL loop filter external capacitor. Connected to external 100pF capacitor.
41	IC ground pad	Ground	

Table 1 Pin descriptions

* ***Caution***: ESD sensitive. Please refer to Section 2.5 for more information.

2. Electrical Characteristics

2.1. Absolute Maximum Ratings

Parameters	Min	Max	Unit
Storage temperature	-40	+120	°C
Supply voltage VDD pin to ground	-0.5	+3.6	V
Voltage applied to inputs	-0.5	VDD+0.5	V
Short circuit duration, to GND or VDD		5	sec

Table 2 Absolute maximum ratings

2.2. Recommended Operating Conditions

Test conditions: VDD = 3 V

Parameters	Min	Typ	Max	Units
*Ambient Operating Temperature	-40		+85	°C
Supply Voltage for RF, analog and digital circuits	2.4	3	3.6	V
Logical high input voltage (for DI type pins)	0.5Xvdd_D			V
Logical low input voltage (for DI type pins)			0.2Xvdd_D	V

Table 3 Recommended operating conditions

2.3. DC Electrical Characteristics

Test conditions: T_A = 25°C, VDD = 3 V

Chip Mode	Condition	Min	Typ	Max	Unit
IDLE	RF in reset mode. Regulator, oscillator and digital circuits are on.		7.6		mA
STANDBY	All circuit power off, only 100kHz oscillator is still on.		3.5		uA
DEEP SLEEP	All circuit power off.		2		uA
ACTIVE: TX	At 0 dBm output power		23		mA
ACTIVE: RX			19		mA

2.4. Radio Frequency AC Characteristics

2.4.1. Receiver Radio Frequency AC Characteristics

Test conditions: T_A = 25°C, VDD = 3 V, LO frequency=2.445 GHz

Parameters	Condition	Min	Typ	Max	Unit
RF input frequency	Compatible to IEEE802.15.4-2003	2.405		2.480	GHz
RF sensitivity	At antenna input with O-QPSK signal		-95		dBm
Maximum RF input		+5			dBm
LO leakage	Measured at the balun matching network with the input frequency at 2.4 ~ 2.5 GHz		-60		dBm
Noise figure (Including matching)			8		dB
Adjacent channel rejection	@+/-5 MHz	30			dB
Alternative channel rejection	@+/-10 MHz	40			dB
RSSI range			50		dB
RSSI error		-5		5	dB
Total RX current			19		mA

2.4.2. Transmitter Radio Frequency Characteristics

Test conditions: T_A = 25°C, VDD = 3 V, LO frequency=2.445 GHz

Parameters	Condition	Min	Typ	Max	Unit
RF carrier frequency		2.405		2.480	GHz
Maximum RF output power			0	3	dBm
RF output power control range			36		dB
TX gain control resolution		0.5	1.25	1.4	dB
Carrier suppression			-30		dBc
TX spectrum mask for O-QPSK signal	Offset frequency > 3.5 MHz, at 0 dBm output power	-33			dBm
TX EVM			10%		
Total TX current	At 0 dBm output power		23		mA

2.5. ESD Notice

For ESD HBM (Human Body Mode), all pins pass 1.5KV voltage requirement.

For ESD MM (Machine Mode), there are 5 pins that are sensitive to ESD; which are pin 2(RF_P), pin 3(RF_N),

pin 5(VDD_GR), pin 27(XTAL32_P) and pin 28(XTAL32_N). PC board designer should take into account of the ESD sensitivity at these 5 pins.

2.6. Peripheral Characteristics

UZ2400 has both slave mode SPI and I^2C interfaces. They can be used by the host MCU to access UZ2400 registers and FIFOs. The 4-wire SPI (SEN, SCLK, SI, SO) provides a high speed interface up to 8MHz on SCLK. Also, the 2-wire I^2C (SDA, SCL) interface provides another lower pin-count solution. The I^2C SDA and SCL share the same pins with SPI SI and SO respectively.

UZ2400 has six GPIO pins. Each can be configured either as an input or output pin. Users can use them for control or monitoring purposes. By simply configure GPIODIR register for input/output selection and GPIO for input/output data, users can gain full control over all six GPIOs.

When using SPI enhanced mode, GPIO4 and GPIO5 become part of SPI bus lines. GPIO0~GPIO3 remain unchanged. Please refer to Section 3.7.1 for detailed description.

2.7. Power-on and Reset Characteristics

UZ2400 has built-in power-on reset (POR) circuit which automatically resets all digital registers when power is turned on. The 20MHz oscillator circuit starts to lock to the right clock frequency after power-on. The whole process takes 2ms for clock circuit to become stable and complete the power-on reset. It is highly recommended that the user waits at least 2ms before starting to access UZ2400.

For external hardware reset (warm start), external reset pin RESETn is internally pulled-high. UZ2400 will hold in reset state around 250usec after RESETn is released from low state.

2.8. Crystal Parameter Specifications

The clock system of UZ2400 can be separated to two parts, one is called main clock and the other is called sleep clock. Main clock is generated by 20MHz oscillator while sleep clock can be selected between 32.768KHz oscillator and 100KHz oscillator. Among all, the 20MHz and 32.768KHz clocks utilize an external crystal for generating the oscillation. The associated pins are XTAL_P, XTAL_N for 20MHz, and XTAL32_P, XTAL32_N for 32.768KHz crystal respectively. The frequency variation allowed for 20MHz crystal is from -60PPM to 60PPM. The 32.768KHz clock is the sleep clock for UZ2400. It provides real-time-clock based timing accuracy to count sleep duration.

3. Functional Description

UZ2400 is composed of six blocks which are listed as followings,

- PHY block
- Lower MAC block
- Memory block
- Power management block
- Security block
- Interfacing block

The block diagram of UZ2400 is shown in Figure 3. Each of the blocks will be described later in this Chapter.

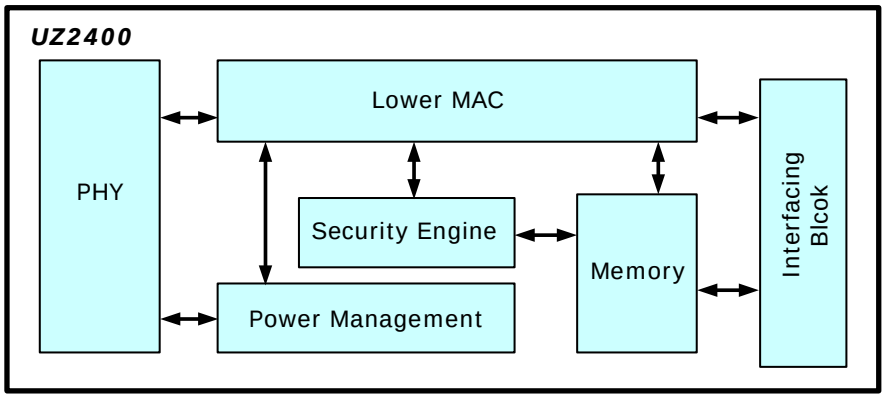


Figure 3 UZ2400 chip block diagram

3.1. PHY Block

The PHY (physical) block is compliant to IEEE 802.15.4-2003 2.4GHz band standard. The architecture is shown in Figure 4.

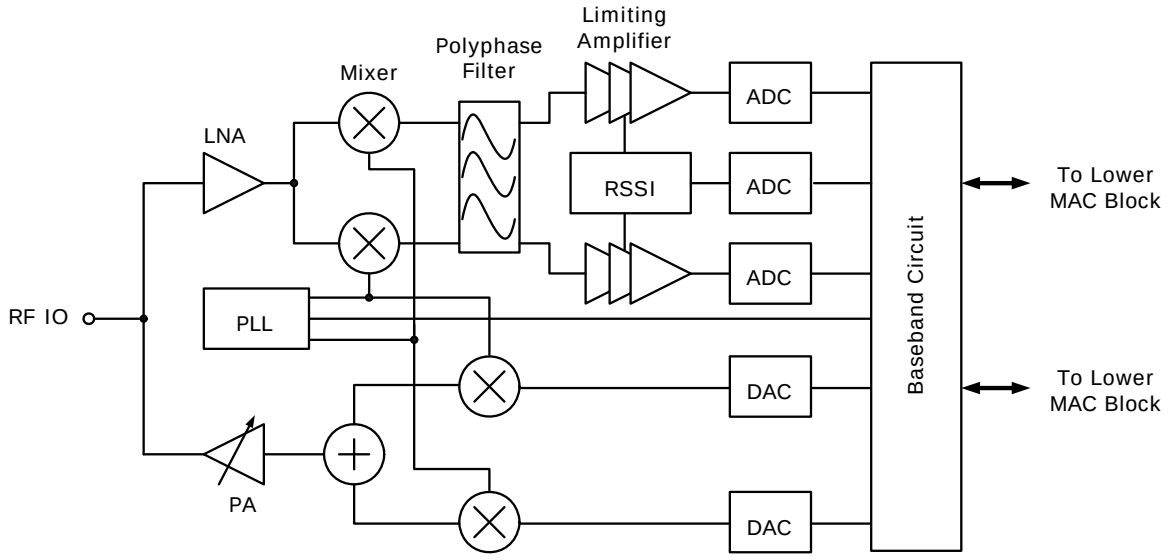


Figure 4 PHY block architecture

3.1.1. IEEE 802.15.4-2003 PHY Introduction

UZ2400 provides a transceiver which is fully compatible to IEEE 802.15.4-2003 2.4GHz band PHY layer specifications. The key features of the PHY layer are described as below.

- Operating frequency range is from 2400 to 2483.5MHz, which includes 16 channels.
- It uses Offset QPSK (OQPSK) modulation to transmit data at 250kbps.
- Direct Sequence Spreading Spectrum (DSSS) is used in baseband algorithm to increase the SNR.
- It provides clear channel assessment (CCA) for CSMA-CA function.
- RSSI signal strength indicator is also provides.

IEEE 802.15.4-2003 compliant packet includes 6 bytes of PHY header and 5~127 bytes of PHY payload. The 6 bytes of PHY header includes 4 bytes of preamble, 1 byte of start-of-frame delimiter (SFD), and 1 byte of payload length. Preamble and SFD are used for receiver packet detection and synchronization. The payload length is valid from 5 to 127 for an IEEE 802.15.4-2003 compliant packet.

The PHY payload includes variable bytes of MAC header, variable bytes of MAC payload and 2 bytes of cyclic redundant check (CRC, also called frame check sum, FCS). The packet format is as below:

PHY header			PHY payload		
Preamble	SFD	Length	MAC header	MAC payload	CRC
4 bytes	1 byte	1 byte	Variable bytes	Variable bytes	2 bytes

Table 4 PHY layer frame format

For more information, please refer to IEEE 802.15.4-2003 standard.

3.1.2. RSSI/ED and LQI

RSSI is used to report the signal strength of a received packet. UZ2400 attaches RSSI value following a received packet in RXFIFO every time a packet is received successfully. The format in RXFIFO is as below:

LSB					MSB
1 Byte	N Byte	N Bytes	2 Byte	1 Byte	1 Byte
Frame length	Header	Payload	FCS	LQI	RSSI

Please refer to Appendix A for RSSI mapping table.

3.1.3. CCA

Clear Channel Assessment (CCA) is designed to detect whether the current channel is occupied by other

devices and used in the CSMA-CA algorithm (see Section 3.2.5). UZ2400 provides three types of CCA functions: CS (Carrier Sense), ED (Energy Detection) and a combination of both.

- CS mode: The CCA/CS mode detects if there is an IEEE802.15.4 2.4G OQPSK signal occupying the current channel. To use this mode, set short register 0x3A bit7-6 to 0x01 and then configure the CS threshold by setting short register 0x3A bit5-2. The recommended threshold value is 0xE.
- ED mode: The CCA/ED mode detects if there is an in-band signal occupying the current channel. To use this mode, set short register 0x3A bit7-6 to 0x10 and then configure the ED threshold by setting short register 0x3F. For the threshold value mapping, please refer to Appendix A.
- Combination of CS and ED mode: This mode checks both the CS and ED results for CCA. To use this mode, set the short register 0x3A bit7-6 to 0x11 and set the CS and ED threshold as described above.

3.2. Lower MAC Block

UZ2400 MAC provides plenty of hardware-assisted features to relieve the CPU/MCU power requirement. TX-MAC performs the CSMA-CA protocol to send a packet automatically. It also generates a 16-bit FCS automatically. In the Beacon-enabled mode, according to the Superframe architecture, TX-MAC will send the packet in normal FIFO during the CAP (contention access period), the packet in GTS1/2 FIFO during the CFP(contention free period) and the packet in beacon FIFO during the Superframe beacon period.

RX-MAC receives packets from the RX-Baseband. The received packet is put into RXFIFO and checked for FCS simultaneously. RX-MAC performs the packet filtering by destination address field and PAN-ID. If both match own identity and the FCS check is passed, an interrupt is issued to CPU/MCU. In the normal mode, unqualified packets are skipped. However, in promiscuous mode, any packet passing the FCS check is accepted and an interrupt will be issued. In the error mode, any packet is accepted with an interrupt issued. RX-MAC also informs TX-MAC to send an acknowledge packet automatically. This happens whenever a packet is successfully received and bit 5 of FCF is set to '1'. This will maintain the timing requirement of the acknowledge packet.

A 16-bit MAC timer is provided to facilitate the generation of the 15.36ms interrupt necessary for the ZigBee application.

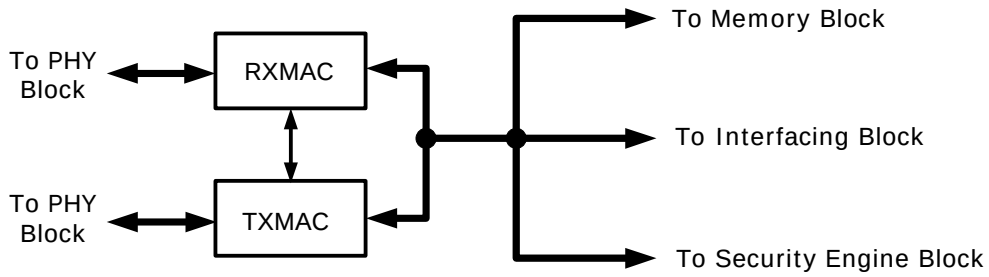


Figure 5 Lower MAC block diagram

3.2.1. IEEE 802.15.4-2003 MAC Introduction

IEEE802.15.4 MAC layer provides reliable wireless packet transactions between two nodes. It also handles data

and command transfer between the network and the physical layers. It handles the following tasks:

- Generating network beacons
- Synchronizing to beacons
- Supporting PAN association and disassociation
- Employing the CSMA-CA mechanism for channel access
- Handling and maintaining the guaranteed time slot mechanism
- Providing a reliable link between two peer MAC entities

The packet format of PHY and MAC layer is given below:

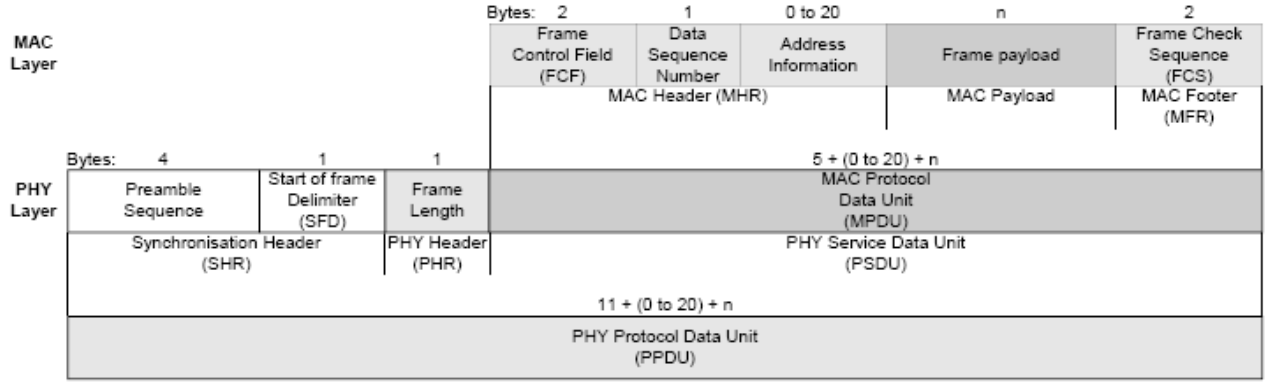


Figure 6 Packet format for PHY and MAC

The frame control field (FCF) format is two bytes as follow:

Bits: 0-2	3	4	5	6	7-9	10-11	12-13	14-15
Frame Type	Security Enabled	Frame Pending	Acknowledge request	Intra PAN	Reserved	Destination addressing mode	Reserved	Source addressing mode

Figure 7 MAC frame control field

The frame check sequence (FCS) is CRC-16. The polynomial is degree 16:

$$G_{16}(x) = x^{16} + x^{12} + x^5 + 1$$

A PAN may be set up in one of the two basic configurations: Beacon-enabled and non-Beacon-enabled. In a non-Beacon-enabled network, devices may communicate with each other at any time after an initial association phase. Channel access and contention are managed using an unslotted CSMA-CA mechanism and any node-level synchronization must be performed at some higher layer. In a beacon-enabled network, the PAN coordinator periodically transmits a beacon which other devices use for both the synchronization and the

determination of the time when to enable transmission and reception of messages. This beacon message is used to define a Superframe structure that all nodes in the PAN should synchronize to. This Superframe structure is shown in the following figure.

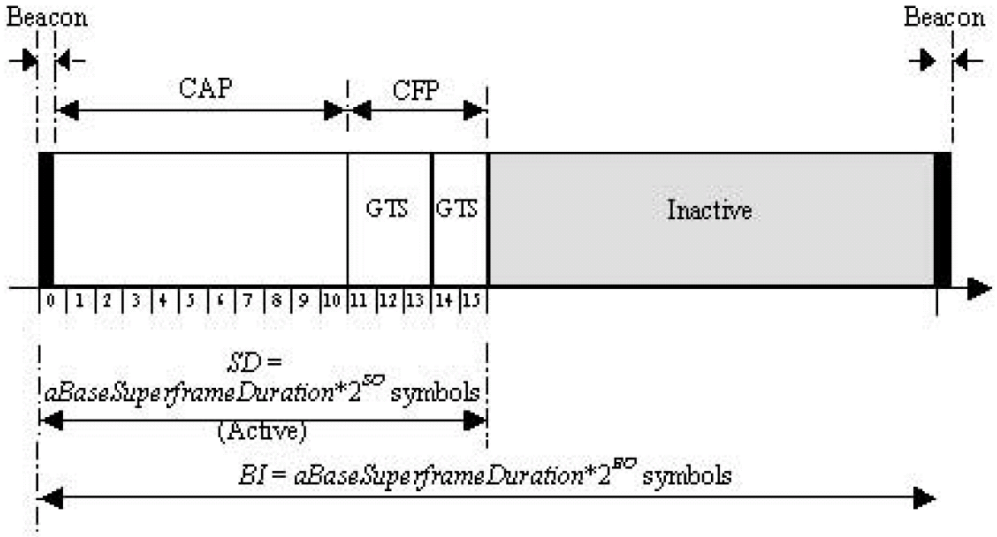


Figure 8 The 802.15.4 MAC Superframe structure

The Superframe is divided into several sections whose lengths are configurable. There is an active period, during which the communication takes place, and an inactive period, during which the devices may turn off their transceivers in order to conserve the power. The active period is divided into 16 equally-spaced slots.

Immediately following the beacon is the contention access period (CAP). During this period, the devices may communicate using a slotted CSMACA mechanism. This is similar to the unslotted CSMA-CA, except that the back-off periods are aligned with the slot boundaries, meaning that the devices are contending for the right to transmit over the entire slots. The CAP must contain at least nine active period slots but may take up all 16.

Following the CAP is an optional contention free period (CFP), which may last up to seven active period slots. In the CFP, the devices are allocated GTS slots by the PAN coordinator. During a GTS, a device has the exclusive access to the channel and does not perform CSMA-CA. During one of these GTSs, a device may either transmit data to or receive data from its PAN coordinator, but not both. The length of a GTS must be an integral multiple of an active period slot. All GTSs must be contiguous in the CFP and are located at the end of the Superframe active period. A device may disable its transceiver during a GTS designated for another device in order to conserve power.

All devices must go through an initial association phase in order to become part of a PAN. This association is prompted by a higher layer service, but it uses primitives defined in the MAC to perform the associations. The MAC allows configurations to be set for starting a device as a PAN as a coordinator, allowing a coordinator to have devices associate with it, and performing the actual association of a device with some coordinator.

Once becoming part of a PAN, the data sent between a device and its coordinator is performed in one of the ways shown in the following figure. Note that acknowledgments are optional in all the transfers from a device to its coordinator, but they are required in transfers from the coordinator to a device. When transferring from a

coordinator to a device, the device must first request the data from the coordinator. In a non-Beacon-enabled network, devices must poll the coordinator for data at an application-specified rate, as there are no beacons to indicate to the device that there is data pending for it.

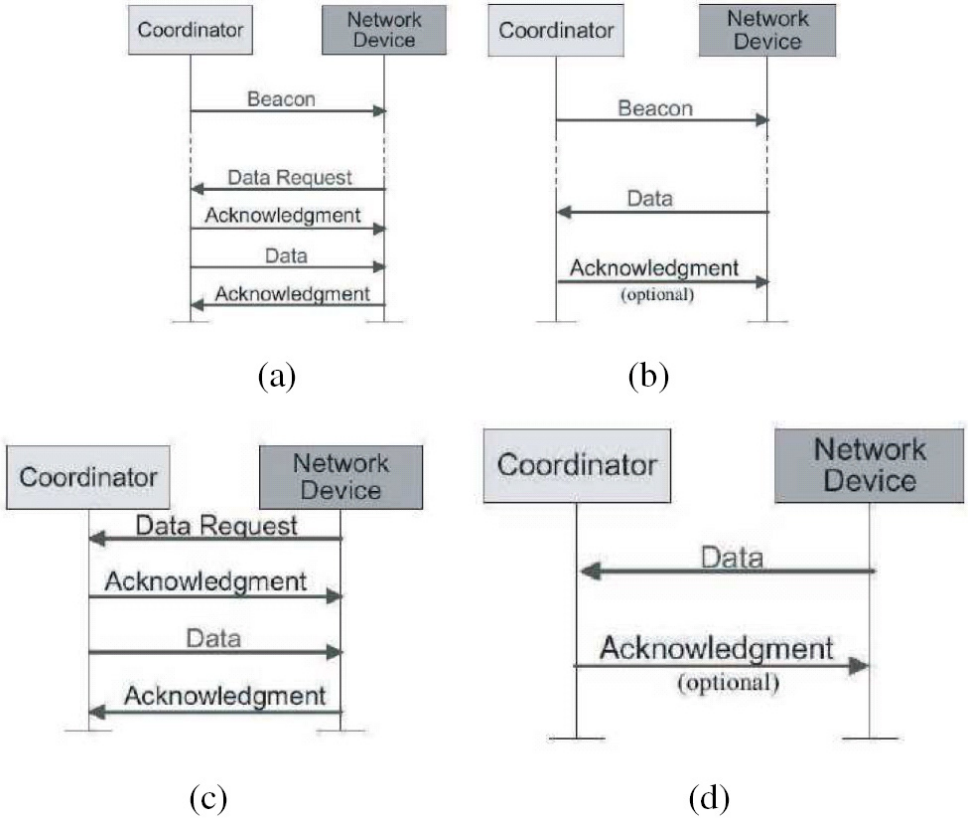


Figure 9 Data transfer between a coordinator and its devices
a)Coordinator to Device with Beacons enabled, b) Device to Coordinator with Beacons enabled, c) Coordinator to Device with Beacons disabled, d)Device to Coordinator with Beacons disabled

3.2.2. MAC Timer

UZ2400 has an internal MAC timer for ZigBee protocol use. It is a 16-bit down-counting timer ticking with half-symbol time (8us for IEEE802.15.4 standard). The beacon interval for ZigBee protocol is multiple times selectable of 15.36ms, which is 1920 times of 8us. Using MAC timer can relieve the timer resource from the MCU. The MAC timer can be triggered by writing HSYMTMR1 register to start downward counting. The timer generates a timer interrupt (half-symbol interrupt) when the down-counting reaches zero. The related registers are as below:

SREG0x28 HSYMTMR0

SREG0x28, HSYMTMR0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
Half-symbol tick timer low byte [7:0]							
R/W-0x00							

Bit 7:0 **HSYMTMR0**: Low byte of 16-bit half-symbol timer.

SREG0x29 HSYMTMR1

SREG0x29, HSYMTMR1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
Half-symbol tick timer low byte [15:8]							
R/W-0x00							

Bit 7:0 **HSYMTMR1**: High byte of 16-bit half-symbol timer.

3.2.3. RXMAC

RXMAC block will do the CRC checking, parsing the received frame type and do the address recognition before storing the received frame in the RXFIFO which is a 128-byte dual port register file. The received frame will be stored in RXFIFO one packet at a time. A byte of length will be appended in front of the MPDU, so that the host can decode the frame correctly. There are also 9 bytes of information attached: LQI, RSSI, Frame Timer (4 bytes), Superframe Counter (3 bytes)

The behavior of RXFIFO follows a certain rule: When a received packet is not filtered or dropped out, a received interrupt/status will be issued. The interrupt is a read-to-clear type to save the host operation time. However, the RXFIFO is flushed only by the following three ways: (1) the host reads the first byte of the packet, (2) the host issues an RX flush and (3) the software reset. Please note that once the first byte of RXFIFO is read, RXFIFO is ready to receive the next packet. So it is suggested that the programmer reads back all data without any interrupt or jumping to other process.

RXMAC recognized a valid packet according to rules provided in Section 7.5.6.2 of IEEE802.15.4-2003 specification. The acceptance rules are:

(1) The frame type subfields shall not contain an illegal frame type.
(2) If the frame type indicates that the frame is a beacon frame, the source PAN identifier shall match macPANId unless macPANId is equal to 0 x ffff, in which case the beacon frame shall be accepted regardless of the source PAN identifier.
(3) If a destination PAN identifier is included in the frame, it shall match macPANId or shall be the broadcast PAN identifier (0xFFFF).
(4) If a short destination address is included in the frame, it shall match either macShortAddress or the broadcast address (0xFFFF). Otherwise, if an extended destination address is included in the frame, it shall match aExtendedAddress.
(5) If only source addressing fields are included in a data or MAC command frame, the frame shall be accepted only if the device is a PAN coordinator and the source PAN identifier matches macPANId.

If the above conditions are met, RXMAC will issue RX interrupt to host device to indicate a valid packet is received. UZ2400 RXMAC also supports promiscuous mode and error mode. Promiscuous mode is supported to receive all FCS-ok packets. Error mode is supported to receive all packets that successfully correlate with the PHY level preamble and delimiter. Under these two conditions, RXMAC issues RX interrupt, too.

UZ2400 RXMAC supports automatic ACK reply. If and only if the five conditions mentioned above are met, and AckReq bit in frame-control field of header of the received packet is set, an ACK packet will be sent by TXMAC automatically in the meantime. The sequence number will be the same as incoming packet.

When an encrypted packet is received, RXMAC will not inform the security module directly. Instead, it issues a security interrupt. Then the host can decide whether to decrypt or ignore it.

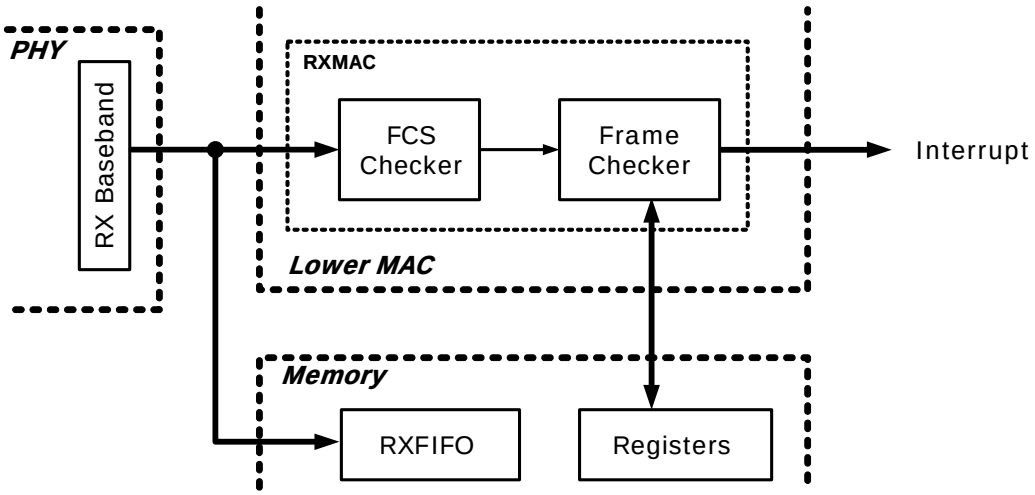


Figure 10 RXMAC block diagram

3.2.4. TXMAC

The block diagram of TXMAC is shown in Figure 11 below. TXMAC performs three major tasks that conform to the IEEE 802.15.4 standard. They are:

- TXFIFO control
- Automatic CSMA-CA and timing alignments.
- Hardware Superframe handling.

For TXFIFO control function, TXMAC controls four FIFOs including the beacon, the normal and the two GTS FIFOs. When each of the FIFOs is triggered, TXMAC performs the CSMA-CA algorithm, sends the packet to TXBB at the right time, handles the retransmission if ACK is required but not received, and generates FCS bytes automatically. Automatic CSMA-CA algorithm performs the timing alignments such as LIFS, SIFS and ACK turnaround time. User can simply program the parameters of CSMA-CA algorithm and TXMAC will perform corresponding tasks automatically.

For hardware Superframe handling under Beacon-enabled operation, TXMAC builds up the timing frame of a Superframe automatically. This greatly alleviates the loading of upper MCU. TXMAC calculates the timing for CAP, CFP, INACTIVE and each time slot then perform corresponding task if there is any. TXMAC sends the beacon, the normal and the GTS FIFOs at the right time of each transmission automatically. This largely reduces the complexity of the Beacon-enabled mode of IEEE 802.15.4.

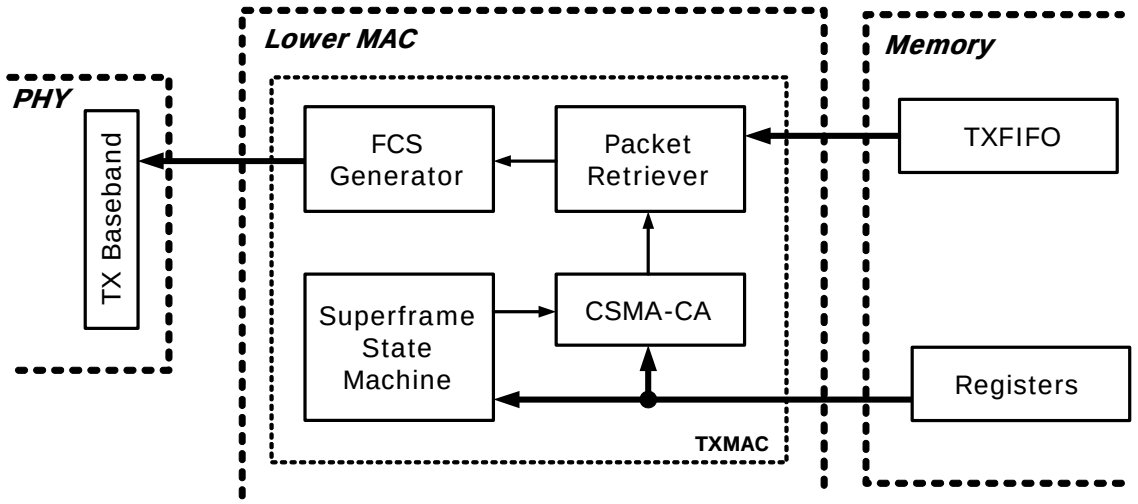


Figure 11 TXMAC block diagram

3.2.5. CSMA-CA

The LR-WPAN uses two types of channel access mechanism, un-slotted CSMA-CA and slotted CSMA-CA. This depends on the network configuration. Non-beacon-enabled networks use an un-slotted CSMA-CA while Beacon-enabled networks use slotted CSMA-CA.

For un-slotted CSMA-CA, each time a device wishes to transmit data frames or MAC commands, it will wait for a random back-off. If the device finds that the channel is idle, it will wait for another extra random back-off before transmitting its data. This extra random back-off reduces the chance of on-air data collision. If a channel is busy, following a random back-off, the device will try to access the channel again. Once the device finds that the channel becomes idle, it will wait for another extra random back-off before transmitting its data. If the channel is always busy and the times of failure is more than macMaxCSMABack-offs (defined in IEEE 802.15.4, this parameter equals 4 by default), the process is considered failed. Acknowledgment frames will be sent without using a CSMA-CA mechanism.

You can modify the parameters of CAMA-CA of UZ2400 at Short register 0x11 as follow.

- SREG0x11[7] defines whether CSMA-CA algorithm is used or not. Set SREG0x11[7] to '1' disables CSMA-CA, otherwise else.
- SREG0x11[4-3] defines the maximum value of the back-off exponent in the CSMA-CA algorithm. Note that if this value is set to 0, collision avoidance is disabled during the first iteration of the algorithm. Also note that for the slotted version of the CSMACA algorithm with the battery life extension enabled, the minimum value of the back-off exponent will be the lesser of 2 and the value of macMinBE.
- SREG0x11[2:0] defines the maximum number of back-offs which the CSMA-CA algorithm will attempt before declaring a channel access failure. The range is between 0 and 5.

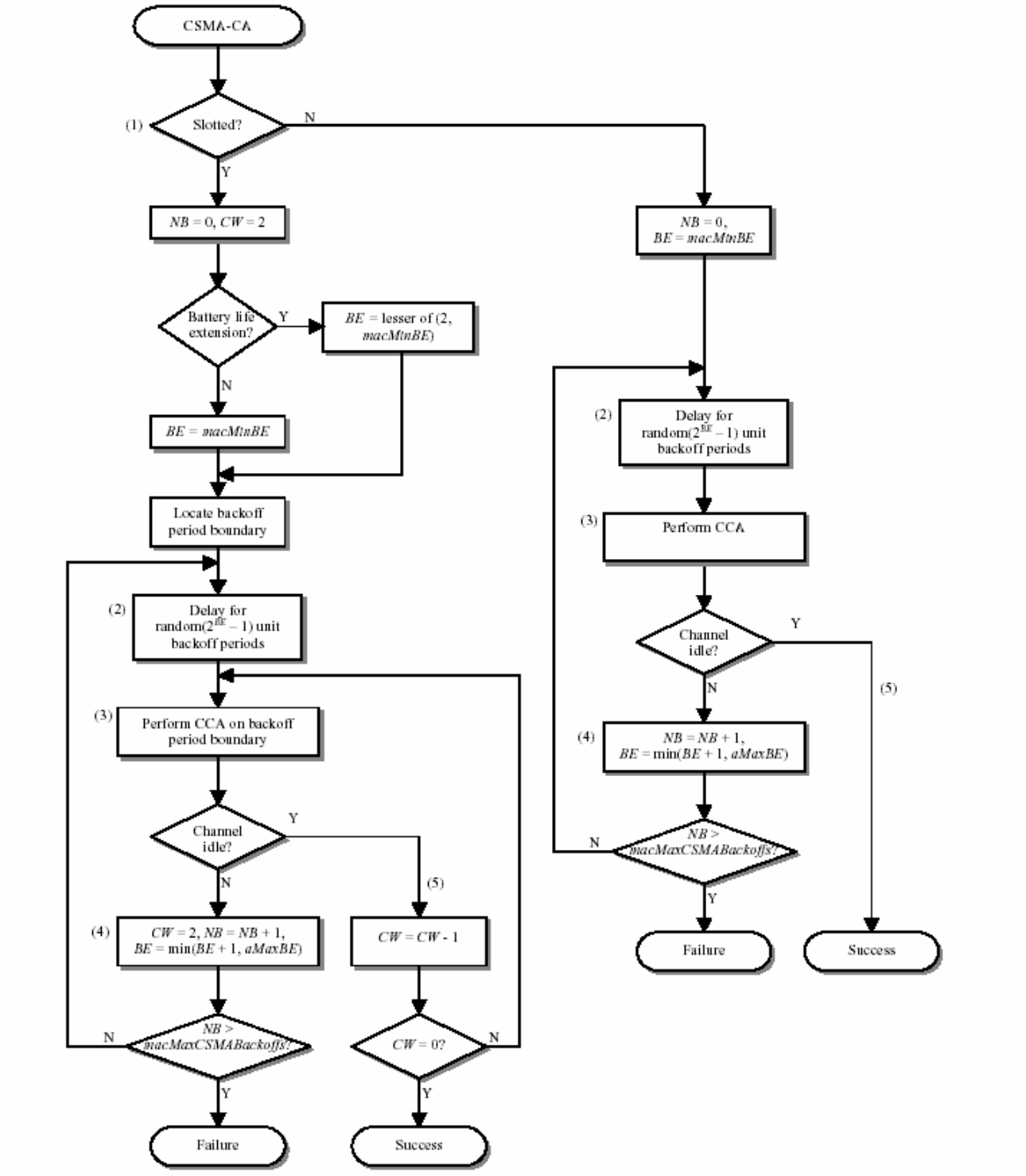


Figure 12 CSMA-CA algorithm

3.3. Memory Block

The memory block (including registers and FIFOs) of UZ2400 is implemented by SRAM. It is composed of registers and FIFOs as shown below:

Registers

- Short register (6-bit short addressing mode register, total 64 bytes)
- Long register (10-bit long addressing mode register, total 128 bytes)

FIFOs

- TX FIFO – Normal (128 bytes)
- TX FIFO – Beacon (128 bytes)
- TX FIFO – GTS1 (128 bytes)
- TX FIFO – GTS2 (128 bytes)
- Security Key FIFO (64 bytes)
- RX FIFO (128 + 16 bytes)

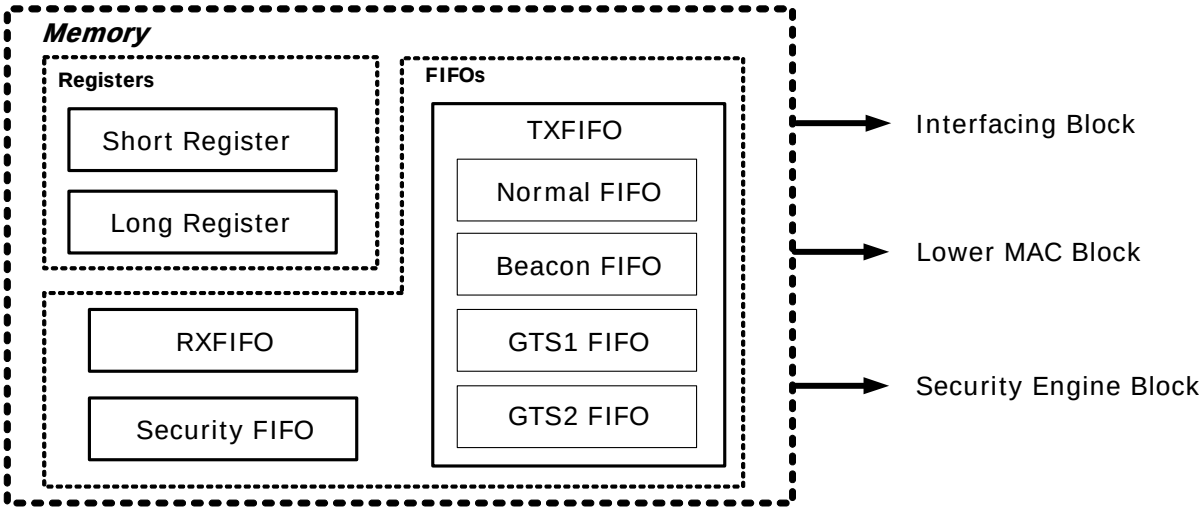


Figure 13 Memory block diagram

FIFO Mapping

Short Address Control Register (64 bytes)

bit [7]	bit [6:1]	bit [0]
Short Address 0	0x3F ~ 0x00	Read/Write 0 1

TXFIFO (512 bytes)

bit [11]	bit [10:1]	bit [0]
Long Address 1	0x1FF ~ 0x000	Read/Write 0 1

Long Address Control Register (128 bytes)

bit [11]	bit [10:1]	bit [0]
Long Address 1	0x27F ~ 0x200	Read/Write 0 1

Security (64 bytes)

bit [11]	bit [10:1]	bit [0]
Long Address 1	0x2BE ~ 0x280	Read/Write 0 1

RXFIFO (128 + 16 bytes)

bit [11]	bit [10:1]	bit [0]
Long Address 1	0x38F ~ 0x37F ~ 0x300	Read/Write 0 1

Registers provide control bits and status flags for UZ2400 operations, including transmission, reception, interrupt control, timer, MAC/baseband/RF parameter settings, security, etc. Short registers are accessed by short addressing mode with valid addresses ranging from 0x00 to 0x3F. Long registers are accessed by long addressing mode with valid addresses ranging from 0x200 to 0x27F. The length of the address differs between the two modes. Please refer to Section 3.7.1 and 3.7.2 for detailed addressing rules for SPI and I^2C interface.

FIFOs serve as the temporary data buffers for data transmission, reception and security keys. Each FIFO holds one packet only at a time. The transmission FIFO is called TXFIFO. TXFIFO is composed of four 128-byte FIFOs for different purposes, namely Normal FIFO, Beacon FIFO, GTS1 FIFO and GTS2 FIFO. The receiving FIFO is called RXFIFO. RXFIFO is composed of one 144-byte FIFO. The final part is called Security Key FIFO. Security Key FIFO is composed of one 64-bite FIFO and is capable of holding four 16-byte security keys for secured operation. The beacon and GTS2 FIFOs share the same security key space. Please refer to Section 4.2 for

further information about registers and FIFOs.

3.3.1. Registers

Short Registers

Short registers are accessed by short addressing mode with valid addresses ranging from 0x00 to 0x3F. Together with long registers, they provide control bits and status flags for UZ2400 operations, including transmission, reception, interrupt control, timer, MAC/baseband/RF parameter settings, security, etc. Short registers are accessed faster than long registers.

Long Registers

Long registers are accessed by long addressing mode with valid addresses ranging from 0x200 to 0x27F. Together with short registers, they provide control bits and status flags for UZ2400 operations, including transmission, reception, interrupt control, timer, MAC/baseband/RF parameter settings, security, etc. Long registers are accessed slower than short registers.

3.3.2. FIFOs

TXFIFO

TXMAC gets data to transmit from four TXFIFOs: beacon, normal, GTS1 and GTS2. According to different conditions, different FIFO is selected. All four TXFIFOs are 128 bytes in length, which can contain one 802.15.4 MAC packet at a time.

In non-beacon-enabled mode, TXMAC always gets data from normal FIFO. In beacon-enabled mode, TXMAC gets data from beacon FIFO during beacon slot. It gets data from normal FIFO during CAP slots and GTS1/2 FIFOs during CFP slots. All of the four FIFOs can be accessed by SPI/I2C interface.

GTS1 and GTS2 FIFOs are ping-pong FIFOs. They are designed for QoS(quality of service) during beacon-enabled mode. The two FIFOs can be assigned to different GTS slots. If they are in the same slot, they take turns within that GTS slot if both are triggered. GTS1/2 FIFO can be triggered before their GTS slot comes. Below is GTS FIFO's behavior:

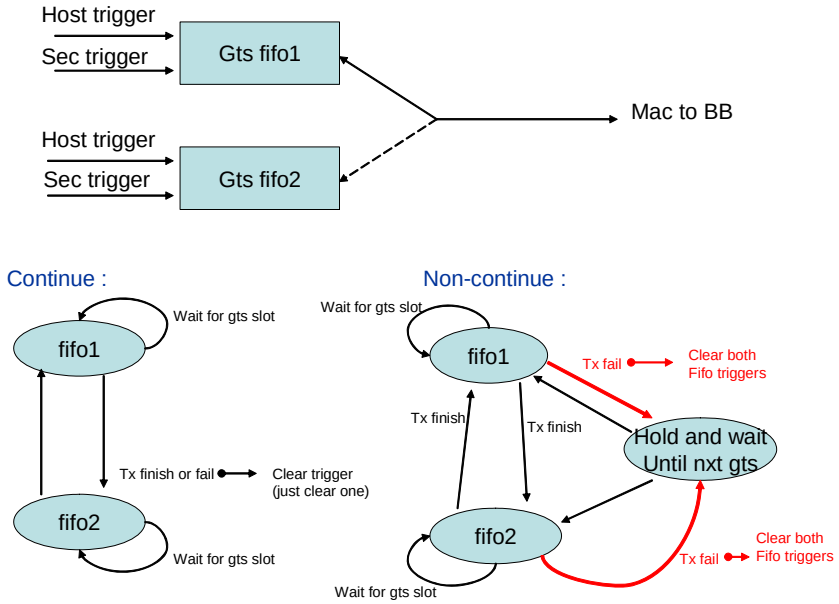


Figure 14 GTS FIFO selection

RXFIFO

RXFIFO is a 144-byte FIFO memory to store the incoming packet. It's designed to store one packet at a time. Section 3.2.3 details the RXMAC behavior.

Security FIFO

Security FIFO holds corresponding key of each FIFO. The address mapping is as below:

Address	Description
280h ~ 28Fh	TX Normal FIFO key
290h ~ 29Fh	TX GTS1 FIFO key
2A0h ~ 2AFh	TX GTS2/Beacon FIFO key
2B0h ~ 2BFh	RX FIFO key

3.4. Power Management Block

Almost all wireless sensor network applications require low-power consumptions to lengthen the battery life. Typical power consumption of a battery-powered device is such that the deployed device could operate over years without replacing its battery. The UZ2400 achieves low active current consumption of both the digital and the RF/analog circuits by controlling the supply voltage and using low-power architecture. The sleep current for UZ2400 can be as low as 2uA only. During the sleep mode, the data in the digital registers/FIFOs are retained. UZ2400 has four power saving modes that will be further described in Section 3.4.5.

3.4.1. Power Supply Scheme

The table below lists the recommended external bypass capacitors for each pin of the UZ2400. For the two power supply pins (pin No.1 and 31), they need an extra bypass capacitor in parallel for decoupling purpose while the rest of the power supply pins require only one bypass capacitor. The path length between the bypass capacitors to each pin should be made as short as possible.

Pin	Symbol	Bypass Capacitor 1	Bypass Capacitor 2
1	VDD_RF1	47 pF	10 nF
4	VDD_RF2	47 pF	
5	VDD_GR	100 nF	
21	VDD_D	10 nF	
31	VDD_BG	47 pF	10 nF
32	VDD_A	47 pF	
35	VDD_PLL	47 pF	
37	VDD_CP	10 nF	
39	VDD_VCO	1 uF	

Table 5 Recommended external bypass capacitors

3.4.2. Voltage Regulator

There is an individual voltage regulator for each supply voltage pin of the UZ2400. No external stabilizing capacitor is needed for each of the voltage regulators. All the regulators supply a 1.8V output to internal circuit nets.

3.4.3. Battery Monitor

UZ2400 provides a function to monitor the system supplied voltage. A 4-bit voltage threshold can be configured so that when the supplied voltage is lower than the threshold, the system will be notified. For battery monitor function, please refer to Section 4.7.

3.4.4. Power-on Reset

UZ2400 has a built-in power-on reset (POR) circuit which automatically resets all digital registers whenever the power is turned on. The 20MHz oscillator circuit starts to lock to the right clock frequency after power-on. The whole process takes 2ms for clock circuit to become stable and complete the power-on reset. It is highly recommended that the user waits at least 2ms before starting to access UZ2400.

3.4.5. Power Modes

The power modes of UZ2400 are classified into the following four modes:

- ACTIVE : Fully turned on with two sub-modes designated as TX-ACTIVE and RX-ACTIVE

- IDLE : RF shutdown mode
- STANDBY : RF/MAC/BB shutdown with sleep clock remains active
- DEEP_SLEEP : All power is shutdown except the power to the digital circuits, register and FIFO data are retained.

The sleep mode mentioned later means both the STANDBY mode and the DEEP_SLEEP mode. The only difference between the STANDBY mode and the DEEP SLEEP mode is the power status of the Sleep clock. The IDLE mode is rarely used because the device should at least always turns on its RX circuit to capture the on-air RF signals.

The power management control is used for the low power operation of the MAC and the baseband modules. It manages to turn on and off the 20MHz clock when the ASIC goes into the sleep mode. By turning off 20MHz clock, the MAC and baseband circuits become inactive regardless whether their power supplies exist or not.

All the digital modules are clock-gated automatically. That means only when a module is functioning, its clock would then be turned on. For example, the clock of the security module is turned off if the security feature is disabled. This approach efficiently decreases a certain amount of current consumption.

With the help of on-chip main and remain counters, UZ2400 is able to switch between ACTIVE and STANDBY modes for both beacon and non-beacon modes. Detailed descriptions are available in Section 3.4.6. If the DEEP_SLEEP mode is desired instead of the STANDBY mode, the host MCU has to control the timing of sleeping process and the Beacon-enabled mode is not suggested under this operation.

3.4.6. Counters for Power Saving Modes

There are two dedicated time counters in UZ2400 for sleep mode operation. One is called main counter and the other is called remain counter. The unit of tick differs between the two counters since the clock for main counter is driven by Sleep clock which is either 100kHz (on-chip internal clock) or 32.768kHz (off-chip external clock). The remain counter is driven by 20MHz clock. The sleeping reference interval is calculated using the combination of the two time counts of main counter and remain counter to achieve timing accuracy.

Sleeping Reference Interval

The sleeping reference interval is composed of three parts. In the beginning, there is the front remain clock period. In the middle, there is the main clock period which is the major component of sleeping reference interval. In the end, there is the rear remain clock period which is identical to the front clock period. The front and rear remain clock periods increase the accuracy of sleeping intervals.

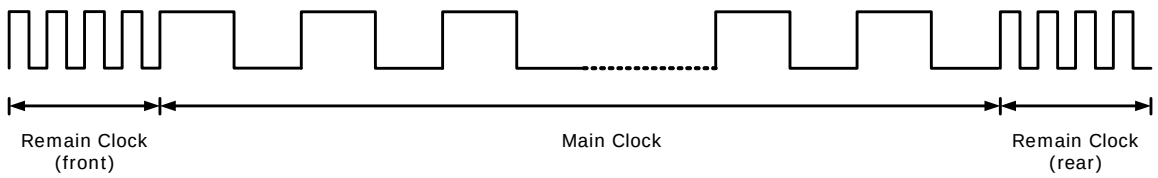


Figure 15 Composition of sleeping reference interval

Sleep Alert (SLPIF, SREG0x31[7])

The sleep alert is issued by TXMAC on the boundary between the active (composed of CAP and CFP) and the inactive period which is defined in the Beacon-enabled mode in IEEE 802.15.4 standard. Sleep alert is an interrupt event which informs the host MCU that the inactive period has been started under Beacon-enabled mode. For Non-beacon-enabled mode, sleep alert is disabled.

Sleep Acknowledgement (SLPACK, SREG0x35[7])

For Beacon-enabled mode, the SLPACK (SREG0x35[7]) should be issued by host MCU to initiate the sleep process. The sleep acknowledgement also turns off the PHY block.

Start Count (StartCnt, LREG0x229[7])

For Non-beacon-enabled mode, the StartCnt (LREG0x229[7]) should be set to "1" to initiate the sleep process. The StartCnt also turns off the PHY block and starts the sleep reference clock under Non-beacon-enabled mode.

Wake-up and Wake-up Alert (WAKEIF, SREG0x31[6])

UZ2400 wakes up when the wake-time (waketime, LREG0x222, LREG0x223) is reached. The 20MHz oscillator is restarted after the wake-up signal asserts itself. Since the 20MHz oscillator needs 2~3 ms to become stable, the 20MHz clock is not enabled immediately once the 20MHz oscillator is restarted. The 20MHz clock will be enabled only when one extra wake-count (WAKECNT, SREG0x35, SREG0x36) is reached.

IEEE 802.15.4 Application Scenarios

The followings are three power saving examples demonstrating the switching between the ACTIVE and the STANDBY modes for typical 802.15.4 application scenarios:

- Beacon-enabled coordinator
- Beacon-enabled device
- Non-beacon-enabled coordinator or device

For Beacon-enabled coordinator, the sum of the main counter and the front and rear remain counters is the beacon interval. Coordinator sends beacon packets according to the interval. A sleep alert is issued by TX_MAC to host MCU at the end of the active period. Host MCU issues a sleep acknowledgement to initiate the sleep process. The coordinator has to prepare the beacon packet in advance. So a "waketime" is designed into the UZ2400 in order to wake it up earlier to allow power on the 20MHz oscillator and make it stable. When the waittime matches the main counter (down counter), the 20MHz clock is enabled. Because it takes certain time for the 20MHz clock to become stable, the clock is not provided until the "waitcnt" is exceeded. Therefore the waittime should be longer than the waitcnt. After the rear remain counter reaches its end, another beacon is transmitted and this gives rise to next Superframe.

For Beacon-enabled device, the sum of the main counter and the front and rear remain counters is the inactive period. A sleep alert is issued by TX_MAC to host MCU at the end of active period. Host MCU issues sleep acknowledgement to initiate the sleep process. The device has to be ready for receiving the beacon packet in advance. So a "waketime" is designed in UZ2400 in order to wake up earlier to allow power on the 20MHz oscillator and make it stable. When the waittime matches the main counter (down counter), the 20MHz clock is

enabled. Because it takes certain time for the 20MHz clock to become stable, the clock is not provided until the "waitcnt" is exceeded. Therefore the waittime should be longer than the waitcnt. Asthe rear remain counter reaches its end, a beacon should be received and this indicates a next Superframe.

In the Non-beacon-enabled mode, the same idea is adopted. The only difference is that the host MCU has to set the StartCnt bit to initiate the sleep process. The sleep reference clock is started right after the StartCnt bit is set. The wake-up process is identical to the beacon mode operation. The actual sleep time is r(front) + m – n as illustrated below.

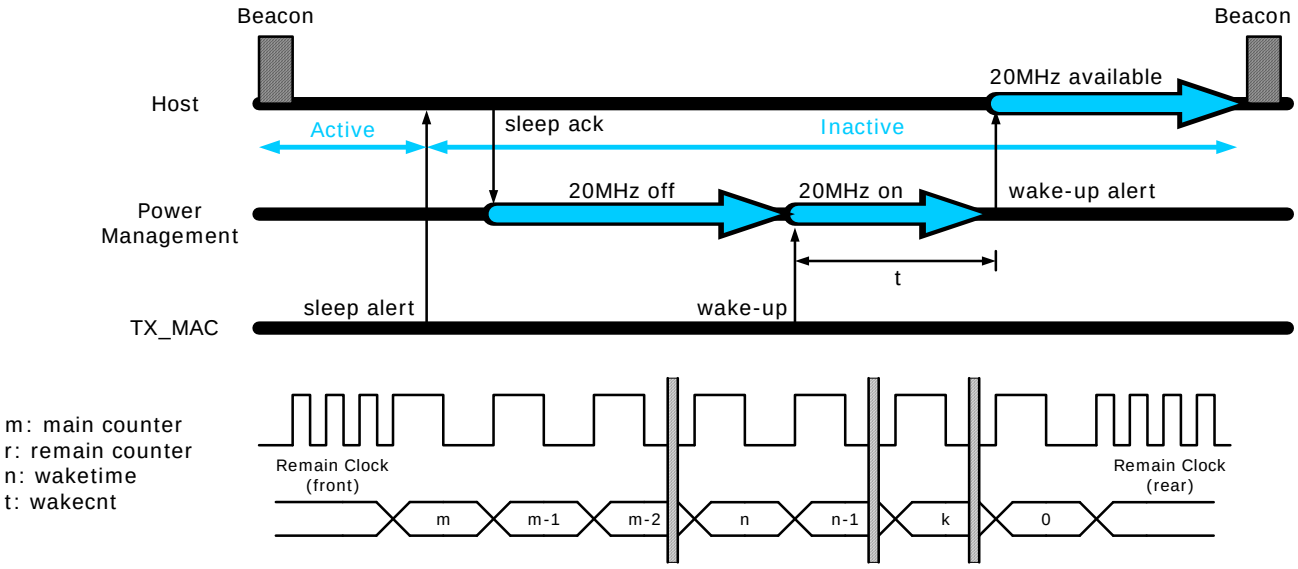


Figure 16 Sleeping timing diagram for Beacon-enabled coordinator

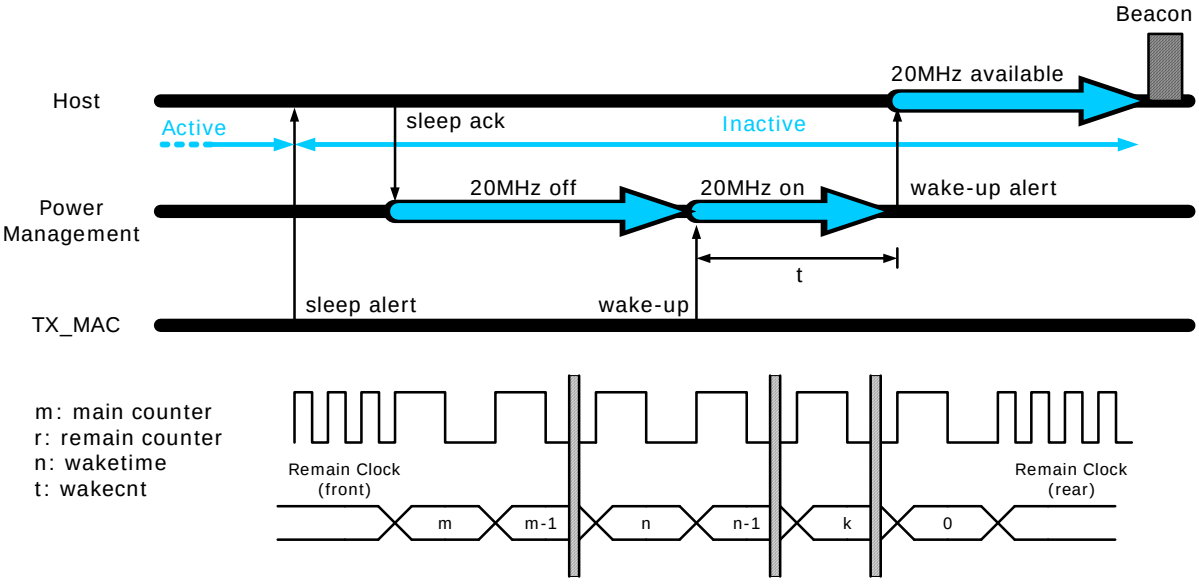


Figure 17 Sleeping timing diagram for Beacon-enabled device

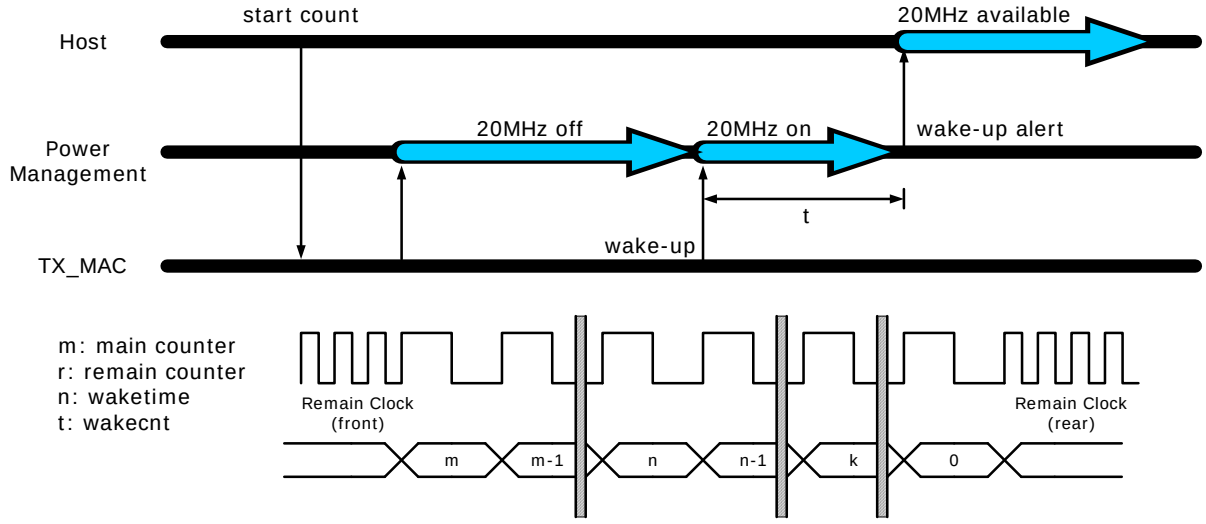


Figure 18 Sleeping timing diagram for Non-beacon-enabled coordinator or device

Main Counter (TXMAINCNT, LREG0x226, LREG0x227, LREG0x228, LREG0x229)

The main counter uses Sleep clock to count. The Sleep clock can be selected by LREG0x207[7:6] between the external 32.76kHz clock or the internal 100kHz clock. An extra clock accuracy calibration should be performed when using the internal 100kHz as Sleep clock. Please refer to Section 4.5.1 for detailed calibration procedure. The count is stored from LREG0x226 to LREG0x229.

Remain Counter (TXREMCNT, LREG0x224, LREG0x225)

The remain counter uses 20MHz clock to count. The count is stored in LREG0x24 and LREG0x25.

Waketime (WAKETIME, LREG0x222, LREG0x223)

The waketime is denoted with the number "n" in the Figure 16, Figure 17 and Figure 18. It indicates the time when the 20MHz oscillator should wake up from the sleep status.

Wake count (WAKECNT, SREG0x35, SREG0x36)

The WAKECNT is the time count "t" in between the restart of the 20MHz oscillator and when it becomes stable and available. It ticks according to the chosen Sleep clock.

Enter STANDBY or DEEP_SLEEP Modes

- STANDBY mode
  - The UZ2400 STANDBY modes can be activated by setting the SLPACK (SREG0x35[7]) under Beacon-enabled mode or setting the StartCnt (LREG0x229[7]) under Non-beacon-enabled mode. When either of these two bits is set, UZ2400 turns off the voltage regulators and the RF circuits enter the sleep mode. During the sleep mode, both long and short registers are accessible and their contents are retained.
- DEEP_SLEEP mode
  - To enter DEEP_SLEEP mode for sleep status, user has to disable the Sleep clock which is always turned-on in STANDBY mode to further reduce the current consumption. DEEP_SLEEP mode is only available under Non-beacon-enabled mode. It is not allowed to turn off the Sleep clock to go into

sleep under Beacon-enabled mode because the Sleep clock has to count the boundaries of Superframe. In Non-beacon-enabled mode, set SLPACK (SREG0x35[7]) to "1" will enforce UZ2400 to sleep without turning on the Sleep clock to generate the sleep reference clock.

Wake-up

UZ2400 has two wake-up modes: timed wake-up and immediate wake-up.

- Timed wake-up
  - Timed wake-up is described in the above under both the beacon and non-beacon modes. However, if user sets both main counter and remain counter to zero, UZ2400 will not wake up unless an immediate wake-up is triggered.
- Immediate wake-up
  - UZ2400 can be awakened externally by WAKE (pin 15). SREG0x0D[5] enables the WAKE pin. SREG0x0D[6] controls the polarity of the WAKE pin. Be sure to set SREG0x22[7] to "1" to enable the Immediate wake-up mode before sleep.
  - UZ2400 can also be awakened by setting SREG0x22[6] to "1" and back to "0", the immediate wake-up mode is then entered.
  - Another fast way to wake up UZ2400 is to set SOFTRST. Setting SREG0x2A[2]="1" resets the power management circuits, including the sleep registers.

3.4.7. Hardware Acknowledgement

Following the IEEE 802.15.4 standard, the request for remote acknowledgement of a transmitted packet can be enabled or disabled by setting its header field. The header format is shown as below:

<table>
<tr><td>Octets: 2</td><td>1</td><td>0/2</td><td>0/2/8</td><td>0/2</td><td>0/2/8</td><td>variable</td><td>2</td></tr>
<tr><td rowspan="2">Frame control</td><td rowspan="2">Sequence number</td><td>Destination PAN identifier</td><td>Destination address</td><td>Source PAN identifier</td><td>Source address</td><td rowspan="2">Frame payload</td><td rowspan="2">FCS</td></tr>
<tr><td colspan="4">Addressing fields</td></tr>
<tr><td colspan="6">MHR</td><td>MAC payload</td><td>MFR</td></tr>
</table>

Figure 34—General MAC frame format

Bits: 0–2	3	4	5	6	7–9	10–11	12–13	14–15
Frame type	Security enabled	Frame pending	Ack. request	Intra-PAN	Reserved	Dest. addressing mode	Reserved	Source addressing mode

Figure 35—Format of the frame control field

Bit 5 of the "Frame control" field indicates whether the frame needs an acknowledgement or not. Users should prepare the header information correctly and write it into TXFIFO. If "Ack request" bit-field is set to "1", the receiver of this packet is required to send the ACK packet back. If the ACK frame from the remote receiver is not received, the transmitter should send the packet again and again till the maximum retransmission times is reached.

UZ2400 has built-in circuit to facilitate the acknowledge protocol automatically. For transmitting side, UZ2400 supports auto-retransmission. For receiving side, UZ2400 supports auto-acknowledgement. Each of the two sides needs to set corresponding registers correctly to utilize the functions.

Auto-retransmission on TX Side

For TXMAC to retransmit a packet automatically when ACK is not received, "TXNACKREQ" (SREG0x1B[2] for TX normal FIFO) is required to be set to "1". Please refer to Section 4.3.1 for more detailed description

Auto-acknowledgement on RX Side

RXMAC of UZ2400 will automatically reply ACK packet by default if "Ack request" in the frame header is set to "1". This auto-acknowledgement feature can be disabled by setting NOACKRSP (SREG0x00[5]) to "1".

3.5. Security Engine Block

The Security module provides the security engine for UZ2400 MAC, which is compatible to IEEE802.15.4-2003 (also adopted by Zigbee). In addition to MAC layer security requirements, UZ2400 also provides a way called "upper-layer security" for network or application layer use. For more detailed information, please refer to Section 4.8.

Following are the features of the UZ2400 Security Engine Block:

- Transmit encryption and receive decryption
- Seven modes of Security suites are provided:
  - AES-CTR
  - AES-CCM-128
  - AES-CCM-64
  - AES-CCM-32
  - AES-CRC-MAC-128
  - AES-CRC-MAC-64
  - AES-CRC-MAC-32
- 64 x 8bits Security RAM for security suite. It stores one receive key and three transmit keys for TXFIFOs. Beacon FIFO and GTS2 FIFO share the same key space since they will not conflict with each other. Normal FIFO and GTS1 FIFO both have their own transmit keys.
- Security of APL and NWK layers can be achieved using the same engine. The upper-layer security function is compliant to ZigBee V1.0 specifications.

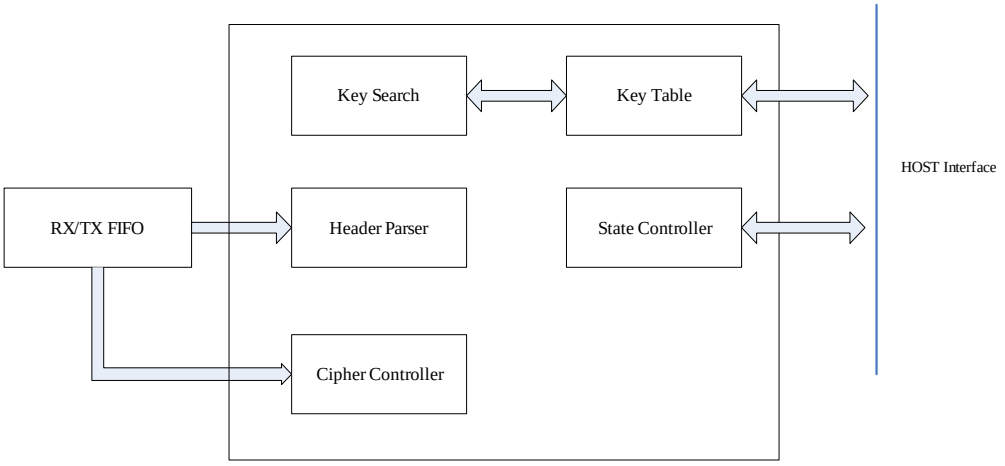


Figure 19 Security engine block diagram

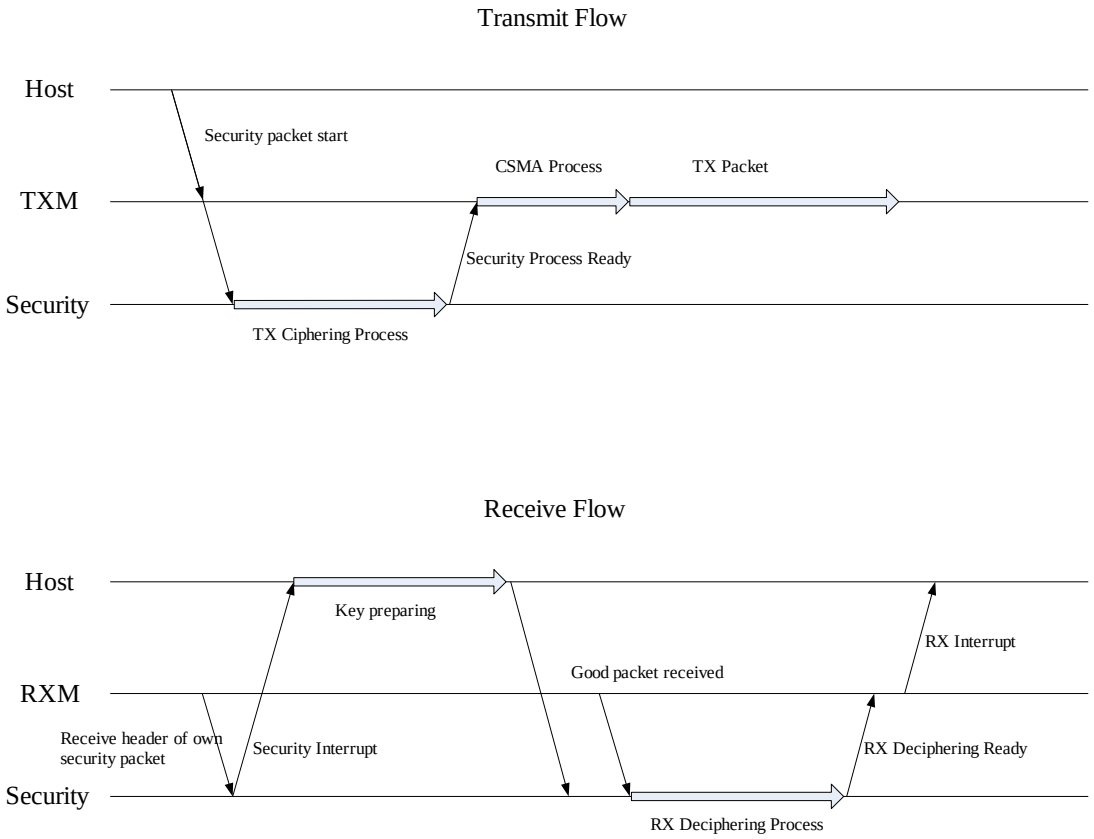


Figure 20 Security engine flow chart

3.6. Analog Circuits

3.6.1. Crystal Oscillators

The table below lists the parameters of the 20 MHz crystal oscillator used in UZ2400. This clock is exportable at pin 26. Optional frequencies are selectable among 20 MHz/10 MHz/5 MHz/2.5 MHz. The crystal can be shared with a host MCU.

By default, 20MHz crystal is suggested for most applications. User has to select 20MHz crystal which meets the following requirements in order to operate UZ2400 properly.

Parameter	Min	Typ	Max	Unit
Crystal Frequency		20		MHz
Crystal Frequency Accuracy	-40		40	ppm

Table 6 Requirements for 20MHz crystal

Parameter	Condition	Min	Typ	Max	Unit
ESR			80		Ohm
C0			5		pF
CL			27		pF
Crystal tuning range			5		pF
Crystal tuning step size			0.5		pF
CRYSTAL TUNING USING					
Start-up time			250		us
Crystal tuning step size	CL=27.5pF		1.2		PPM
Crystal tuning range	CL=22pF		21		PPM

Table 7 On-chip Crystal Frequency Tuning (eCERO FL-200-0006-G)

Parameter	Condition	Min	Typ	Max	Unit
ESR			80		Ohm
C0			1.04		pF
CL			12		pF
Crystal tuning range			8		pF
Crystal tuning step size			0.5		pF
CRYSTAL TUNING USING					
Start-up time			250		us
Crystal tuning step size	CL=27.5pF		-0.6		PPM
Crystal tuning range	CL=22pF		-50		PPM

Table 8 On-chip Crystal Frequency Tuning (NDK NX3225SA)

3.6.2. PLL Frequency Synthesizer

The loop filers of the Phase-Lock Loop (PLL) in the frequency synthesizer are integrated into UZ2400 except one external capacitor which should be connected between pin 40 and the ground. The board layout around pin 40 should be carefully designed to avoid EMI (electro magnetic interference) in order to keep the PLL stable. The recommended value of this external capacitor is 100 pF.

3.6.3. Internal 100kHz Sleep Clock Oscillator for Sleep Clock

There is a free-running 100 kHz sleep clock oscillator integrated into UZ2400. No external component is needed for the operation of this sleep clock. User has to calibrate this 100kHz Sleep clock before an application starts. Please refer to Section 4.5.1 Step 4. for calibration procedures.

3.6.4. 32.768 kHz Crystal Oscillator for Sleep Clock

The table below lists the parameters of the 32.768 kHz crystal oscillator used in UZ2400. The external 32.768kHz crystal greatly enhance the accuracy of this oscillator so that it does not need calibration any more.

Parameter	Min	Typ	Max	Unit
Crystal Frequency		32.768		kHz
Frequency Offset	-20		20	PPM
Shunt Capacitance		33		pF
Series Resistance		10		MΩ
Calibration Time		0.5		msec

Table 9 Requirement for 32.768kHz crystal

3.7. Peripherals

3.7.1. SPI Interface

The SPI module provides slave roles SPI mode 0 interface to read/write the control registers, FIFO and security key table of UZ2400. The features are as below:

- Normal Mode: a simple 4-wire SPI-compatible interface (pins SCLK, SEN, SI and SO) where UZ2400 is the slave.
- Plus Mode: a 2x speed for long address read/write only. It uses SI & SO as SI0 & SI1 while writing long-address data, and as SO1 & SO0 while reading long-address data.
- Enhanced Mode: a 4x speed for long address read/write only. It uses SI, SO, GPIO5, & GPIO4 as SI0, SI1, SI2, & SI3 while writing long-address data, and as SO1, SO0, SO2, & SO3 while reading long-address data.
- Most significant bit (MSB) of all address and data transfer on the SPI interface is done first
- Mode selection: By default, SPI is set to normal mode. To select plus and enhanced modes, SReg0x34[7:6] should be set (by normal SPI operation) to 0x1 as plus mode, and 0x2 as enhanced mode. Afterward, plus or enhanced modes should be used.

SPI Characteristics

Parameter	Symbol	Min	Max	Units	Conditions
SCLK, clock frequency	F_{SCLK}		<10 <5	MHz	10MHz in normal/plus mode 5MHz in turbo mode
SCLK low pulse duration	t_{CL}	50 100		ns	The minimum time SCLK must be low.
SCLK high pulse duration	t_{CH}	50 100		ns	The minimum time SCLK must be high.
SEN setup time	t_{SP}	50		ns	The minimum time SEN must be low before the first positive edge of SCLK.
SEN hold time	t_{NS}	>50 >100		ns	The minimum time SEN must be held low after the last negative edge of SCLK.
MOSI setup	t_{SD}	25		ns	The minimum time data must be ready at MOSI, before the positive edge of SCLK
MOSI hold time	t_{HD}	25		ns	The minimum time data must be held at MOSI, after the positive edge of SCLK.
Rise time	t_{RISE}		25	ns	The maximum rise time for SCLK and SEN.
Fall time	t_{FALL}		25	ns	The maximum fall time for SCLK and SEN.

Table 10 SPI characteristics

SPI Frame Format

Short Address Control Register (64 bytes)

bit [7]	bit [6:1]	bit [0]
Short Address 0	0x3F ~ 0x00	Read/Write 0 1

Long Address Control Register (128 bytes)

bit [11]	bit [10:1]	bit [0]
Long Address 1	0x27F ~ 0x200	Read/Write 0 1

Figure 21 FIFO addressing under SPI mode

SPI Timing Diagrams

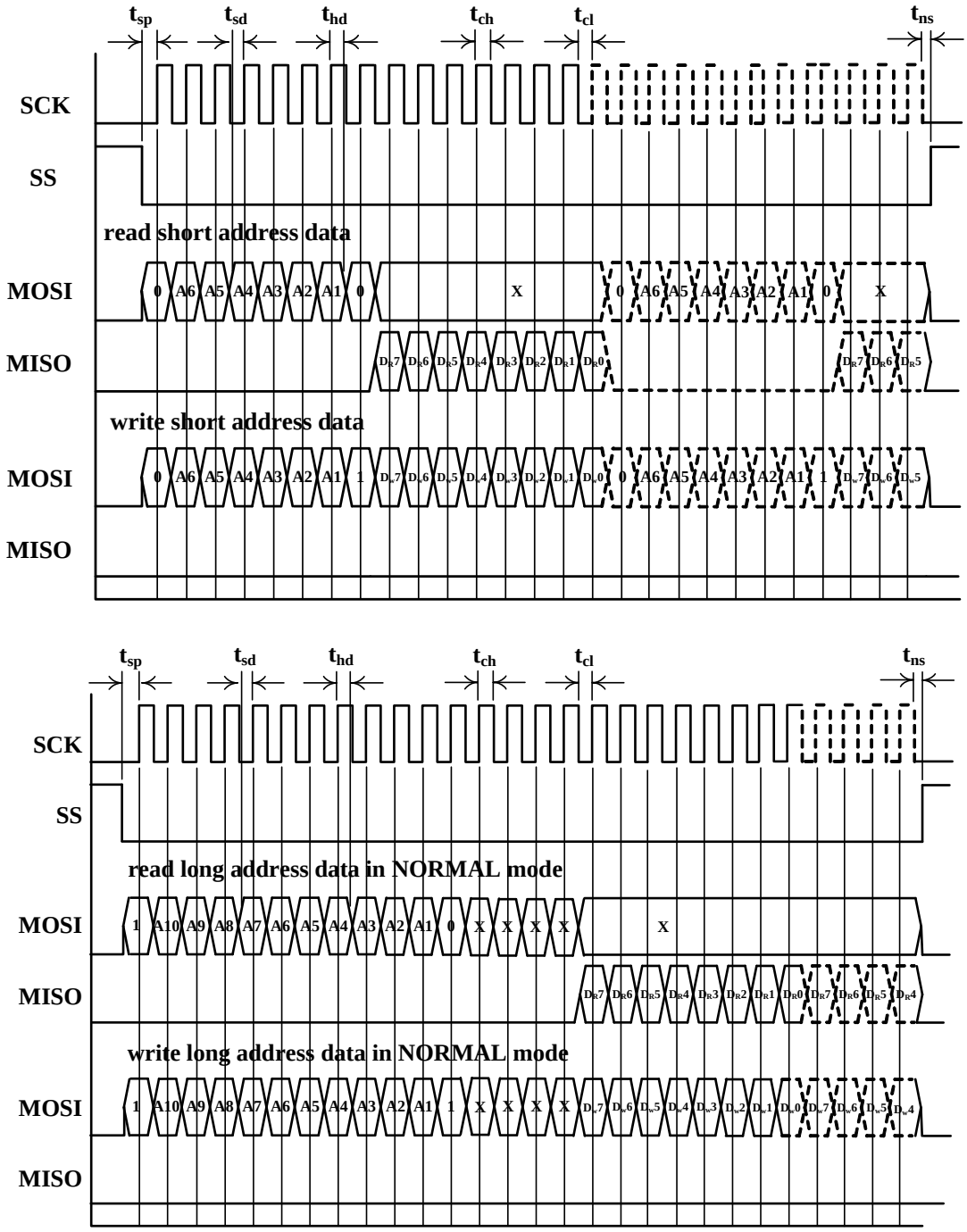


Figure 22 Timing diagram and specification in Normal Mode

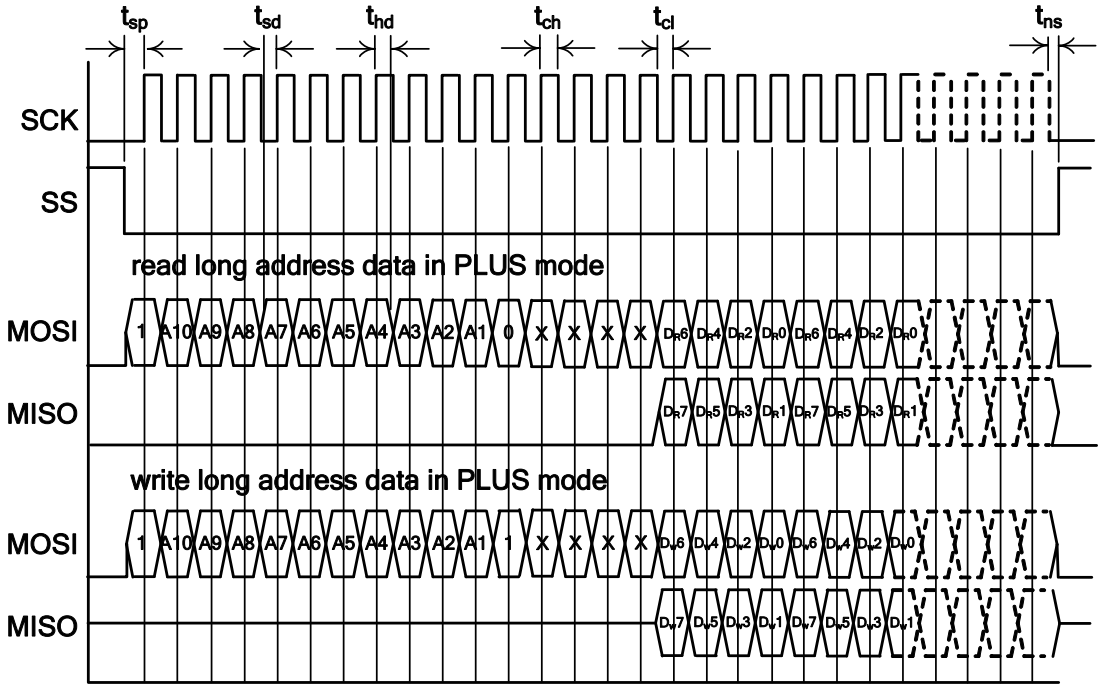


Figure 23 Timing diagram and specification in Plus Mode (Only for long address registers)

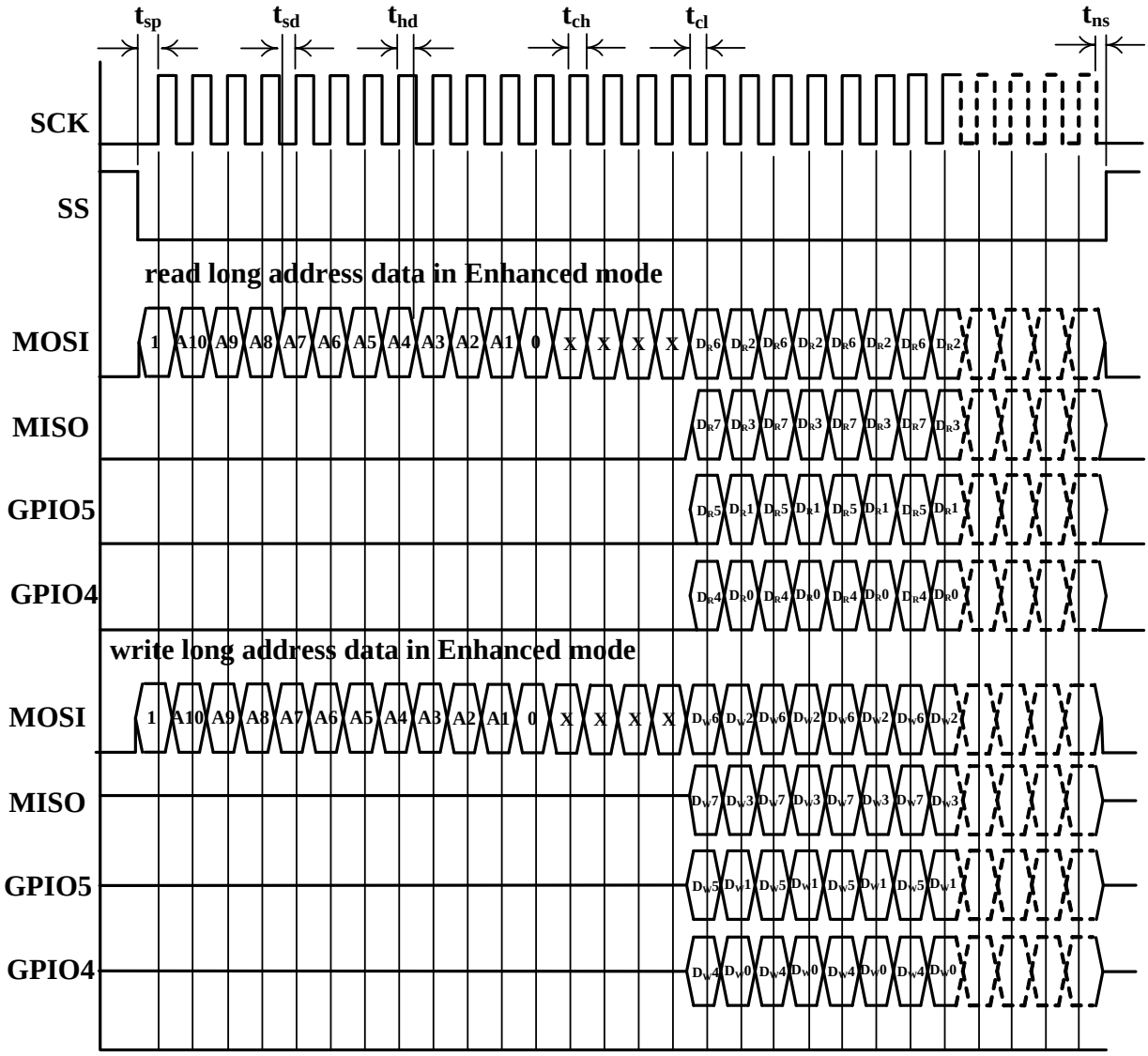


Figure 24 Timing diagram and specification in Enhanced Mode (Only for long address registers)

3.7.2. I²C Interface

UZ2400 provides another serial interface, I²C serial interface, to access the control registers and FIFOs.

Device Operation

- CLOCK and DATA TRANSITIONS: The SDA/SCL pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods will indicate a start or stop condition as defined below.
- START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command.

- STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition.
- ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the UZ2400 in 8-bit words. The UZ2400 sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

Device Addressing

The UZ2400 requires 7-bit device addresses plus control bits-over the two-wire serial bus following a start condition to enable the chip for a read or write operation. The device address word consists of 11001 for the first five most significant bits as shown below. The next 2 bits are b_2 and b_1 which are selected by SCLK and SEN pins respectively. The $11001b_2b_1$ is the I^2C slave address of UZ2400. The programmable part b_2b_1 of the address is defined by hardware pins SCLK and SEN respectively. The last bit b_0 is a control bit. If b_0 is LOW, it means "Write Operation" or else "Read Operation".

SCLK	SEN	Slave Address
0	0	110 0100
0	1	110 0101
1	0	110 0110
1	1	110 0111

Table 11 I^2C device address configuration

Write Operations

A writing operation requires an 8-bit data word address following the slave address word and acknowledgment. Upon receipt of this address, the UZ2400 will again respond with a zero and then clock in the first 8-bit register address. Following the receipt of the 8-bit data word, the UZ2400 will automatically output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition.

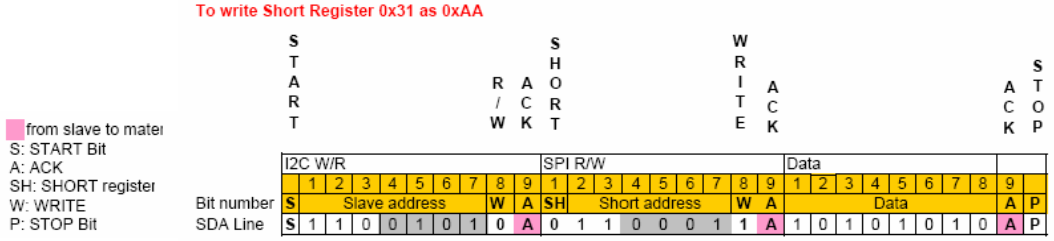
Read Operations

Read operations are initiated the same way as the write operations with the exception that the read/write select bit in the slave address word is set to one.

Once the slave address word and data word address are clocked in and acknowledged by the UZ2400, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The UZ2400 acknowledges the slave address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition

Short Register Write

Example: write short register 0x31 as 0xAA



Short Register Read

Example: read short register 0x31

	I2C R/W										SPI R/W									
Bit count		1	2	3	4	5	6	7	8	9	1	2	3	4	5	6	7	8	9	
	S	Slave address							W	A	S	Short address							W	A	P
Read 0x31 0xaa	S	1	1	0	0	1	0	1	0	A	0	1	1	0	0	0	1	1	A	P

from slave to master
R:Read
Ab: A bar (inverse ACK)

I2C R/W										SPI R/W																			
	1	2	3	4	5	6	7	8	9	1	2	3	4	5	6	7	8	9	1	2	3	4	5	6	7	8	9		
S	Slave address							R	A	S	Short address							R	A	Data								A	P
S	1	1	0	0	1	0	1	1	A	0	1	1	0	0	0	1	0	A	1	0	1	0	1	0	1	0	Ab	P	

Long Register Write

Example: write long register 0x231 as 0xAA

To write Long Register 0x231 as 0xAA

from slave to mater
S: START Bit
A: ACK
L: Long Register
W: WRITE
P: STOP Bit

	START									R/W	ACK	LONG								ACK								WRITE								ACK								ACK							
	I2C W/R											SPI R/W																																					
	1	2	3	4	5	6	7	8	9	1	2	3	4	5	6	7	8	9	1	2	3	4	5	6	7	8	9	1	2	3	4	5	6	7	8	9	1	2	3	4	5	6	7	8	9		
Bit number	S	Slave address							W	A	L	Long address								A	Long Address								W	NA								A	Data								A	P
SDA Line	S	1	1	0	0	1	0	1	0	A	1	1	0	0	0	1	1	0	A	0	0	1	1	×	×	×	×	A	1	0	1	0	1	0	1	0	A	P									

Long Register Read

Example: read short register 0x231

Step1:write address of read

	I2C R/W										SPI R/W																																			
Bit count		1	2	3	4	5	6	7	8	9	1	2	3	4	5	6	7	8	9	1	2	3	4	5	6	7	8	9																			
	S	Slave address							W	A	L	Long address								A	LA								W	NA								A	P										
SDA Line	S	1	1	0	0	1	0	1	0	A	1	1	0	0	0	1	1	0	A	0	0	1	1	0	0	0	0	A	P																			

Step2: read data

	I2C R/W										SPI R/W																																					
	1	2	3	4	5	6	7	8	9	1	2	3	4	5	6	7	8	9	1	2	3	4	5	6	7	8	9	1	2	3	4	5	6	7	8	9											
S	Slave address							R	A	L	Long address								A	LA								R	NA								A	Data								A	P		
S	1	1	0	0	1	0	1	1	A	1	1	0	0	0	1	1	0	A	0	0	1	0	0	0	0	0	A	1	0	1	0	1	0	1	0	Ab	P											

3.7.3. GPIO

UZ2400 has 6 digital GPIOs. Each GPIO can be configured as input or output respectively. When being configured as an output pad, the driving capability is 4mA for GPIO0 and 1mA for GPIO1, GPIO2, GPIO3, GPIO4, and GPIO5.

Besides, GPIO1 and GPIO2 can be configured to control external PA, LNA, switch according to the current RF state, TX or RX. Please refer to Section 4.2.6 for external PA/LNA application configuration.

3.7.4. Interrupt Signal

UZ2400 provides an output interrupt pin (INT) and the polarity of interrupt signal is selectable. UZ2400 issues interrupts to host MCU on eight possible events (For detailed interrupt event description, please see Section 4.2.5). If any event happens, UZ2400 sets the corresponding status bit in SREG0x31. And if the corresponding interrupt mask in SREG0x32 is clear (i.e. equals "0"), interrupt will be issued. If it is set (masked, blocked), interrupt will not be issued, but the status is still present. Interrupt is a read-to-clear operation. Whenever SREG0x31 is read, interrupt and status are cleared. This is beneficial to increase the performance.

UZ2400 issues interrupt according to the following eight events which are described as below:

Sleep alert interrupt (SLPIF)
In Beacon-enabled mode, UZ2400 counts the active and inactive periods. When encountering the inactive period, UZ2400 will issue a sleep alert interrupt to indicate the event, regardless whether it is set to be the coordinator or the device mode.

Wake-up alert interrupt (WAKEIF)
Every time a wake-up event happens, UZ2400 issues the interrupt event.

Half symbol timer interrupt (HSYMTMRIF)
HSYMTMR(16 bits) setting with SREG0x28 and SREG0x29 is an internal timer ticking at half-symbol rate (8 us in IEEE802.15.4 standard). The interrupt is issued when HSYMTMR down counts to "0". Note that HSYMTMR does not reload.

Security interrupt (SECIF)
On receiving a packet with "Security enable" bit set in "Frame control" field of packet header, security interrupt is issued. Normally the host MCU should prepare the security key, NONCE, cipher mode or other necessary information at that moment. Then start or ignore the decryption. Also refer to Section 18 Security Mode.

RX OK interrupt (RXIF)
This interrupt is issued when an available packet is received in RXFIFO. An available packet means that it passes RXMAC filter, which includes FCS check, PANID/address filtering, packet type or promiscuous/error modes.

GTS FIFO 2 release interrupt (TXG2IF)
This interrupt is issued when a packet in GTS FIFO2 is triggered and sent successfully or is triggered and the retransmission is timed out. SREG0x24[4][2] indicate the release status of GTSFIFO2.

GTS FIFO 1 release interrupt (TXG1IF)
This interrupt is issued when a packet in GTS FIFO1 is triggered and sent successfully or is triggered and retransmission is timed out. SREG0x24[3][1] indicates the release status of GTSFIFO1.

TX normal FIFO release interrupt (TXNIF)
This interrupt is issued when a packet in normal FIFO is triggered and sent successfully or is triggered and the

retransmission is timed out. SREG0x24[0] indicates the TX normal FIFO release status.

The interrupt events are indicated in SREG31. The register is “read-to-clear”. Each of the eight interrupts can be masked by setting INTMSK(SREG0x32).

4. Application Guide

Some typical applications are described in this chapter to help designer gains more understanding of the capability of UZ2400.

4.1. Hardware Connection

4.1.1. Typical Application Connection Using SPI Interface

A typical connection using SPI interface is shown below. The MCU serves as master role and UZ2400 serves as slave role.

Balun circuitry: L1/L2/C4/C5, L3, C3
Antenna matching circuitry: L4/C12

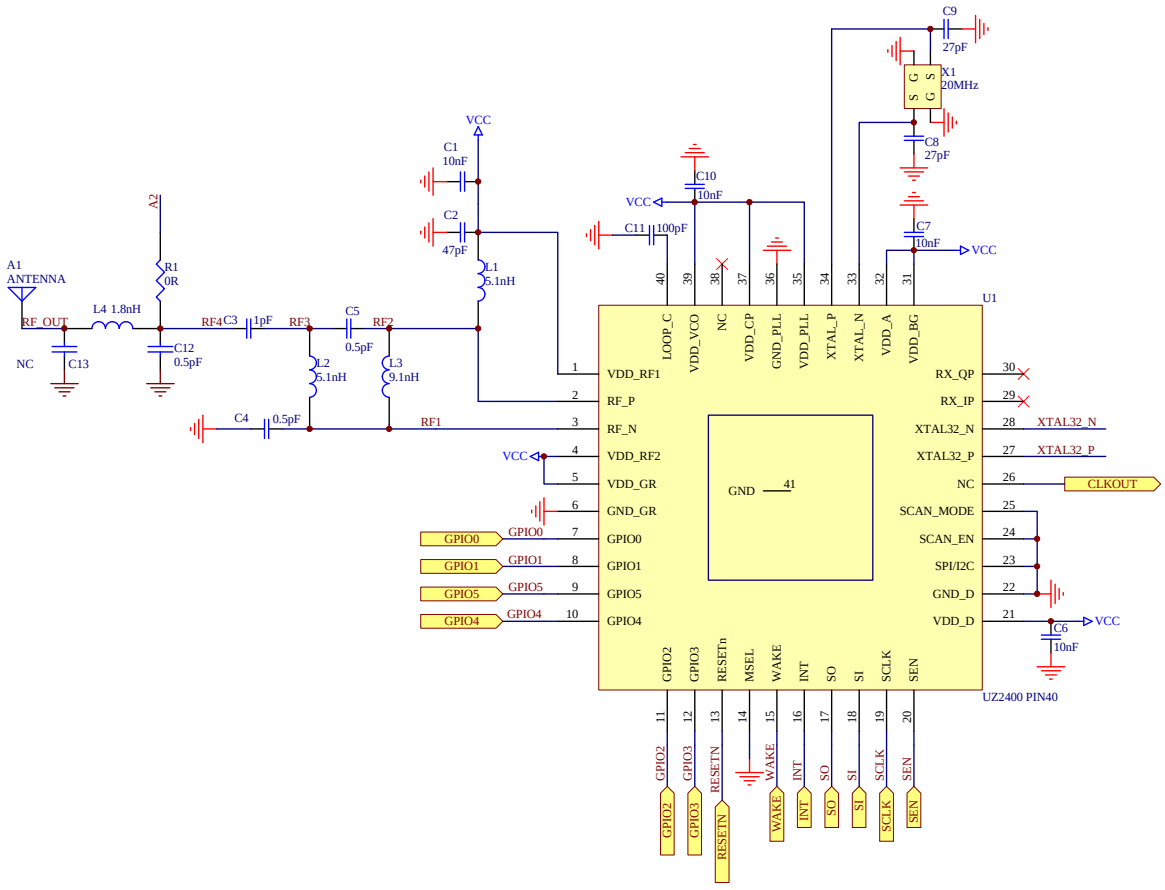


Figure 25 Typical application circuit using SPI interface

4.1.2. Adding External Power Amplifier and Low Noise Amplifier

The following depicts the typical circuit diagram for external PA/LNA enabled design using UBEC UP2268. UP2268 integrates PA, LNA and RF switch.

Balun circuitry: L1/L2/C4/C5, L3, C3
Antenna matching circuitry: L5, C20, C23
PA matching circuitry: C22, L9/C26, L8/C24/C25
LNA matching circuitry: L4/C15, L6, L7/C16

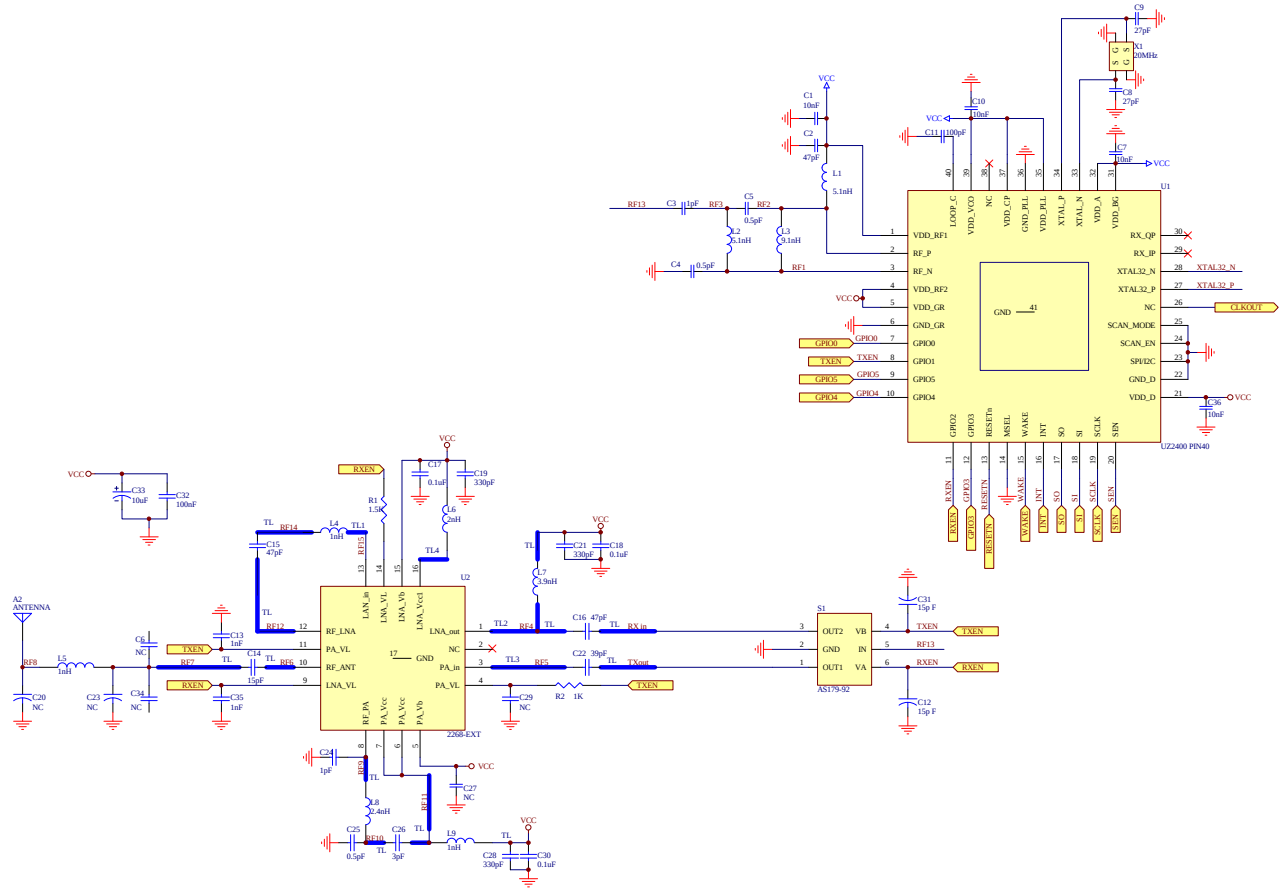


Figure 26 Typical application circuit using external PA/LNA

4.2. Registers and FIFOs

UZ2400 registers and FIFOs can be accessed by both SPI and I^2C interfaces. They are divided into two addressing spaces. One is the short addressing space; the other is the long addressing space.

4.2.1. Memory Space

Figure 27 Memory space diagram

4.2.2. Register Summary

Short Registers

Address	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR
0x00	RXMCR	--		NOACKRSP	--	PANCOORD	COORD	ERRPKT	PROMI	–0- 0000
0x01	PANIDL	PANIDL								0000 0000
0x02	PANIDH	PANIDH								0000 0000
0x03	SADRL	SADRL								0000 0000
0x04	SADRH	SADRH								0000 0000
0x05	EADR0	EADR0								0000 0000
0x06	EADR1	EADR1								0000 0000
0x07	EADR2	EADR2								0000 0000
0x08	EADR3	EADR3								0000 0000
0x09	EADR4	EADR4								0000 0000
0x0A	EADR5	EADR5								0000 0000
0x0B	EADR6	EADR6								0000 0000
0x0C	EADR7	EADR7								0000 0000
0x0D	RXFLUSH	--	WAKEPOL	WAKEPAD	--	ONLYCMD	ONLYDATA	ONLYBCN	RXFLUSH	-000 0000
0x10	ORDER	BO				SO				1111 1111
0x11	TXMCR	NOCSMA	--	SLOTTED	MACMINBE		CSMABF			0001 1100

0x13	SLALLOC	GTS1				CAP			0000 0000
0x18	FIFOEN	FIFOEN	--	TXONTS			TXONT		1-00 1000
0x1A	TXBCNTRIG	--					TXBCNSECEN	TXBCNTRIG	---- --00
0x1B	TXNTRIG	--		PENDACK	INDIRECT	TXNACKREQ	TXNSECEN	TXNTRIG	---- -000
0x1C	TXG1TRIG	TXG1IFETRY		TXG1SLOT		TXG1ACKREQ	TXG1SECEN	TXG1TRIG	0000 0000
0x1D	TXG2TRIG	TXG2IFETRY		TXG2SLOT		TXG2ACKREQ	TXG2SECEN	TXG2TRIG	0000 0000
0x1E	ESLOTG23	GTS3				GTS2			0000 0000
0x1F	ESLOTG45	GTS5				GTS4			0000 0000
0x20	ESLOTG67	--				GTS6			---- 0000
0x21	TXPEND	--					GTSSWITCH	--	---- --0-
0x22	WAKECTL	IMMWAKE	REGWAKE	--					00-- ----
0x24	TXSR	TXRETRY		CCAFAIL	TXG2FNT	TXG1FNT	TXG2S	TXG1S	TXNS 0000 0000
0x25	TXBCNMSK	TXBCNMSK	--						0--- ----
0x26	GATECLK	--				ENGTS	--		---- 0---
0x28	HSYMTMR0	HSYMTMR0							0000 0000
0x29	HSYMTMR1	HSYMTMR1							0000 0000
0x2A	SOFTRST	--					RSTPWR	RSTBB	RSTMAC ---- -0--
0x2C	SECCR0	SECIGNORE	SECSTART	RXCIPHER			TXNCIPHER		0000 0000
0x2D	SECCR1	--	TXBCIPHER			SNIFMODE	--	DISDEC	DISENC -000 --00
0x2E	TXPEMISP	TXPET				MISP			0111 0101
0x30	RXSR	--	UPSECERR	BATIND	--				-00- ----
0x31	ISRSTS	SLPIF	WAKEIF	HSYMTMRIF	SECIF	RXIF	TXG2IF	TXG1IF	TXNIF 0000 0000
0x32	INTMSK	SLPMSK	WAKEMSK	HSYMTMRMSK	SECMSK	RXMSK	TXG2MSK	TXG1MSK	TXNMSK 1111 1111
0x33	GPIO	--		GPIQ5	GPIQ4	GPIQ3	GPIQ2	GPIQ1	GPIQ0 --00 0000
0x34	SPIGPIO	SPIMODE		GPDIR5	GPDIR4	GPDIR3	GPDIR2	GPDIR1	GPDIR0 0000 0000
0x35	SLPACK	SLPACK	WAKECNT						0000 0000
0x36	RFCTL	20MOFF	--	WAKECNTEXT			RFRESET	--	0--0 00--
0x37	SECCR2	UPDEC	UPENC	TXG2CIPHER			TXG1CIPHER		0000 0000
0x38	BBREG0	--						TURBO	---- ---0
0x39	BBREG1	--					RXDECODEINVERSION	--	---- -0--
0x3A	BBREG2	CCAMODE		CCATH				--	0100 10--
0x3B	BBREG3	PREVALIDTH				PREDETTH		--	1101 100-
0x3C	BBREG4	CSTH			PRECNT		TXDACEDGE	RXADCEDGE	1001 1100
0x3E	BBREG6	RSSIMODE1	RSSIMODE2	--				RSSIRDY	00-- ---1
0x3F	BBREG7	RSSITHCCA							0000 0000

Table 12 Short address register list

Long Registers

Address	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR
0x200	RFCTRL0	CHANNEL				RFOPT				0000 0000
0x202	RFCTRL2	RFPLL	RSSIDC		RSSISLOPE		--			0000 0---
0x203	RFCTRL3	TXPOWL		TXPOWF			--			0000 0---
0x205	RFCTRL5	BATTH				--				0000 ----
0x206	RFCTRL6	TXFIL	--	20MRECVR		BATMONEN	--			0-00 0---
0x207	RFCTRL7	SLPCLK		--				CLKDIV		00-- --00
0x208	RFCTRL8	--			RFVCO	--				---0 ---0
0x209	SLPCAL1	SLPCAL1								0000 0000
0x20A	SLPCAL2	SLPCAL2								0000 0000
0x20B	SLPCAL3	CALRDY	--		CALEN	SLPCAL3				0--0 0000
0x211	CLKIRQCR	--						IRQPOL	CLK32KOFF	---- --00
0x220	SCLKDIV	I2CWDTEN	--		SCLKDIV					0-00 0000
0x222	WAKETIMEL	WAKETIMEL								0000 1010
0x223	WAKETIMEH	--					WAKETIMEH			---- -000
0x224	TXREMCNTL	TXREMCNTL								0000 0000
0x225	TXREMCNTH	TXREMCNTH								0000 0000
0x226	TXMAINCNT0	TXMAINCNT0								0000 0000
0x227	TXMAINCNT1	TXMAINCNT1								0000 0000
0x228	TXMAINCNT2	TXMAINCNT2								0000 0000
0x229	TXMAINCNT3	STARTCNT	TXMAINCNT3							0000 0000
0x22F	TESTMODE	--			RSSIWAIT		TESTMODE			---0 1000
0x230	ASSOEADR0	ASSOEADR0								0000 0000
0x231	ASSOEADR1	ASSOEADR1								0000 0000
0x232	ASSOEADR2	ASSOEADR2								0000 0000
0x233	ASSOEADR3	ASSOEADR3								0000 0000
0x234	ASSOEADR4	ASSOEADR4								0000 0000
0x235	ASSOEADR5	ASSOEADR5								0000 0000
0x236	ASSOEADR6	ASSOEADR6								0000 0000
0x237	ASSOEADR7	ASSOEADR7								0000 0000
0x238	ASSOSADR0	ASSOSADR0								0000 0000
0x239	ASSOSADR1	ASSOSADR1								0000 0000
0x240 | 0x24C	UPNONCE									

Table 13 Long address register list

4.2.3. Security Buffers

Security buffer stores the security keys. These keys will be needed for secured data packet transferring.

Address	Description
280h ~ 28Fh	TX normal FIFO key
290h ~ 29Fh	GTS1 FIFO key
2A0h ~ 2AFh	GTS2/Beacon FIFO key
2B0h ~ 2BFh	RX FIFO key

Table 14 Security buffer mapping

4.2.4. Initialization

After UZ2400 is powered up, some registers need to be configured before the data transmission or reception. The procedure is described as below.

Step 1.

Perform software reset by writing SREG0x2A to '0x07'.

Address mode	Addr	Register Name	Descriptions	Setting Value(hex)
SREG	0x2A	SOFTRST	Software reset	0x07

SREG0x2A SOFTRST

SREG0x2A, SOFTRST							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
reserved					RSTPWR	RSTBB	RSTMAC
					WT-0	WT-0	WT-0

Bit 2 **RSTPWR**: Power management reset
Write "1" to perform reset.

Bit 1 **RSTBB**: Baseband reset
Write "1" to perform reset.

Bit 0 **RSTMAC**: MAC reset
Write "1" to perform reset.

Step 2.

Set the registers according to the following table. Shouldn't we calibrate the TX output power??

Address mode	Addr	Register Name	Descriptions	Setting Value(hex)
SREG	0x3A	BBREG2	Set CCA mode to ED	0x80
SREG	0x3E	BBREG6	Append RSSI value in Rx packets	0x40

SREG	0x3F	RSSIYHCCA	ED threshold for CCA	0x60
SREG	0x18	FIFOEN	Increase TXON time	0x98
SREG	0x2E	TXPEMISP	VCO calibration period	0x95
SREG	0x35	SLPACK	20MHz clock recovery time	0x5F
LREG	0x201	RFCTL1	RF optimized control	0x01
LREG	0x202	RFCTL2	RF optimized control	0x80
LREG	0x206	RFCTL6	RF optimized control	0x90
LREG	0x207	RFCTL7	RF optimized control	0x80
LREG	0x208	RFCTL8	RF optimized control	0x10
LREG	0x220	SCLKDIV	sleep clock frequency control	0x01
SREG	0x32	INTMSK	Enable all interrupt	0x00

SREG0x3A BBREG2

SREG0x3A, BBREG2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
CCAMODE		CCATH				reserved	
R/W-0b01		0b0010					

Bit 7-6 **CCAMODE**: CCA mode selection
0b00: reserved
0b01: Carrier sense (CS) mode, detect IEEE 802.15.4 signals
0b10: Energy detection (ED) mode, detect in-band signals
0b11: Combination of carrier sense mode and energy detection mode

Bit 5-2 **CCATH**: CCA carrier sense threshold
NOTE: suggested value is 0b1110

SREG0x3E BBREG6

SREG0x3E, BBREG6							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
RSSIMODE1	RSSIMODE2	reserved					RSSIRDY
WT-0	R/W-0						R-1

Bit 7 **RSSIMODE1**: RSSI mode 1 enable
1: calculate RSSI for firmware request, will be clear to "0" when RSSI calculation is finished.

Bit 6 **RSSIMODE2**: RSSI mode 2 enable
1: calculate RSSI for each received packet, the RSSI value will be stored in RXFIFO.
0: no RSSI calculation for received packet.

Bit 0 **RSSIRDY**: RSSI ready signal for **RSSIMODE1** use
If **RSSIMODE1** is set, this bit will be cleared to "0" until RSSI calculation is done. When RSSI calculation is finished and the RSSI value is ready, this bit will be set to "1" automatically.

SREG0x3F BBREG7

SREG0x3F, BBREG7							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
RSSITHCCA							
R/W-0x0							

Bit 7-0 **RSSITHCCA**: CCA-ED threshold

Note: If the in-band signal strength is larger than the threshold, the channel is busy. The 8-bit value can be mapped to a certain power level according to Appendix A.

SREG0x18 FIFOEN

SREG0x18, FIFOEN							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
FIFOEN	reserved	TXONTS				TXONT	
R/W-1		R/W-0x2				R/W-0x0	

Bit 7 **FIFOEN**: TXFIFO and RXFIFO output enable manual control
1: TXFIFO and RXFIFO are always output enabled.
Note: Setting Bit7 value to "0" is forbidden, or fatal error will occur.
Bit 5-2 **TXONTS**: The last symbol number before TX. The minimum value is "1".
Bit 1-0 **TXONT**: The period that rfmode1 active before TX.

SREG0x2E TXPEMISP

SREG0x2E, TXPEMISP							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXPET				MISP			
R/W-0111				R/W-0101			

Bit 7-4 **TXPET**: For VCO circuit calibration.
Bit 3-0 **MISP**: For CSMA-CA and GTS circuit calibration.

The recommend value for TXPEMISP is 0x95. Please do not use other values for this register.

SREG0x35 SLPACK

SREG0x35, SLPACK							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SLPACK	WAKECNT						
WT-0	R/W-0000000						

Bit 7 **SLPACK**: Sleep acknowledge. Set this bit to "1" will cause UZ2400 enter the sleep mode immediately. This bit will be automatically cleared to "0".

Bit 6-0 **WAKECNT**: System clock (20MHz) recovery time
Note: In the initial procedure, set **WAKECNT** to 0x5F to optimize the performance.

LREG0x201 RFCTL1

LREG0x201, RFCTRL1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
reserved							VCOCTL
							R/W-0

Bit 0 **VCOCTL**: RF VCO current control
1: the recommended value for RF optimization.

LREG0x202 RFCTL2

LREG0x202, RFCTRL2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
PLLCTL	RSSIDC		RSSISLOPE		reserved		
R/W-0	R/W-0b00		R/W-0b00				

Bit 7 **PLLCTL**: RF Phase Lock Loop (PLL) control
1: the recommended value for RF optimization. This needs to be set before the RF transmission and reception.
Bit 6-5 **RSSIDC**: RSSI DC level shift.
Note: 0b11 is not allowed.
Bit 4-3 **RSSISLOPE**: RSSI range control.
Note: 0b11 is not allowed.

LREG0x206 RFCTL6

LREG0x206, RFCTL6							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TXFIL	reserved	20MRECVR		BATEN	reserved		
R/W-0		R/W-0b00		R/W-0			

Bit 7 **TXFIL**: TX filter control
1: the recommended value for RF optimization.
Bit 5-4 **20MRECVR**: 20MHz clock recovery time (recovery from sleep) control
10: less than 1 ms
Otherwise: less than 3ms
Bit 3 **BATEN**: Battery monitor enable
1: Battery monitor is enabled.
0: Battery monitor is disabled.

LREG0x207 RFCTL7

LREG0x207, RFCTL7							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SLPCLK		reserved					
R/W-0b00							

Bit 7-6 **SLPCLK**: Sleep clock source selection
10: internal ring oscillator
01: external crystal
Otherwise: Do not use other value
Note: If the external 32.768kHz crystal is not connected, SLPCLK needs to be set to 10.

LREG0x208 RFCTL8

LREG0x208, RFCTL8							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved			RFVCO	reserved			
			R/W-0				

Bit 4 RFVCO: VCO control. Recommend value is "1".

LREG0x220 SCLKDIV

LREG0x220, SCLKDIV							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
I2CWDTEN	reserved		SCLKDIV				
R/W-0			R/W-0b00000				

Bit 7 **I2CWDTEN**: I^2C watchdog timer enable
1: enable
0: disable
Bit 4-0 **SCLKDIV**: sleep clock division selection.
n: the sleep clock is divided by 2^n before being fed to logic circuit.
Note: If internal ring oscillator is used, 0b0001 is the recommended value.

SREG0x32 INTMSK

SREG0x32, INTMSK							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SLPMSK	WAKEMSK	HSYMTMRMSK	SECMSK	RXMSK	TXG2MSK	TXG1MSK	TXNMSK
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 7 **SLPMSK**: Sleep alert interrupt mask
Bit 6 **WAKEMSK**: Wake-up alert interrupt mask
Bit 5 **HSYMTMRMSK**: Half symbol timer interrupt mask
Bit 4 **SECMSK**: security interrupt mask
Bit 3 **RXMSK**: RX receive interrupt mask

Bit 2 **TXG2MSK**: TX GTS2 FIFO transmission interrupt mask

Bit 1 **TXG1MSK**: TX GTS1 FIFO transmission interrupt mask

Bit 0 **TXNMSK**: TX Normal FIFO transmission interrupt mask

1: the interrupt is masked, and hence the INT pin will not change even if an interrupt occurs.

0: the interrupt is not masked.

Step 3.

Set RF operation channel. UZ2400 operates in the 2.4 GHz Industry, Scientific, and Medical (ISM) unlicensed band. The operating frequency is divided into 16 channels. If user wants to select any operating channel, RFCTL0(LREG0x200) should be configured as the following table.

Address mode	Addr	Register Name	Descriptions	Setting Value(hex)
LREG	0x200	RFCTL0	Set RF operation channel	List as Table 8.

Channel Name	Frequency	Register Address	Set Value(hex)
Channel 11	2405 MHz	0x200	02
Channel 12	2410 MHz	0x200	12
Channel 13	2415 MHz	0x200	22
Channel 14	2420 MHz	0x200	32
Channel 15	2425 MHz	0x200	42
Channel 16	2430 MHz	0x200	52
Channel 17	2435 MHz	0x200	62
Channel 18	2440 MHz	0x200	72
Channel 19	2445 MHz	0x200	82
Channel 20	2450 MHz	0x200	92
Channel 21	2455 MHz	0x200	A2
Channel 22	2460 MHz	0x200	B2
Channel 23	2465 MHz	0x200	C2
Channel 24	2470 MHz	0x200	D2
Channel 25	2475 MHz	0x200	E2
Channel 26	2480 MHz	0x200	F2

Table 15 RF operation channel settings

LREG0x200 RFCTRL0

LREG0x200, RFCTRL0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
CHANNEL				RFOPT			
R/W-0b0000				R-0b0000			

Bit 7-4 **CHANNEL**: RF channel number. IEEE 802.15.4 2.4GHz band channels (11~26) are mapped as follows.

0b0000: channel 11 (2405MHz)

0b0001: channel 12 (2410MHz)

0b0010: channel 13 (2415MHz)
0b1111: channel 26 (2480MHz)

Bit 3-0 **RFOPT**: Optimize RF control
0b0010 is the recommended value for RF optimization.

Step 4.

After the operation channel is set, RF state machine should be reset by setting RFCTL(SREG0x36) to "0x04" and then setting RFCTL(SREG0x36) to "0x00". After reset, 192us should be waiting for VCO calibration to calibrate PLL block to the correct frequency.

Address mode	Addr	Register Name	Descriptions	Setting Value(hex)
SREG	0x36	RFCTL	Reset RF state machine	0x04
SREG	0x36	RFCTL	Reset RF state machine	0x00

By finishing all the above six steps, a basic initialization procedure is done. This configuration procedure is valid for most of the application conditions.

4.2.5. Interrupt Configuration

UZ2400 issues hardware interrupt via pin 16 to host MCU. There are two related registers that need to be set correctly with respect to designer's application. The interrupt status can be read from ISRSTS (SREG0x31). The interrupt is by default sent to the host MCU as a falling edge signal. The interrupt should be configured in the step 2 of the initialization procedure by setting INTMSK(SREG0x32) whose description is omitted here. All the interrupts are masked (disabled) by default.

Address mode	Addr	Register Name	Descriptions
SREG	0x31	ISRSTS	Interrupt status
SREG	0x32	INTMSK	Interrupt masks
LREG	0x211	CLKIRQCR	32kHz Clock and interrupt polarity configuration register

SREG0x31 ISRSTS

SREG0x31, ISRSTS							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SLPIF	WAKEIF	HSYMTMRIF	SECIF	RXIF	TXG2IF	TXG1IF	TXNIF
RC-0	RC-0	RC-0	RC-0	RC-0	RC-0	RC-0	RC-0

Bit 7 **SLPIF**: Sleep alert interrupt bit
0: Otherwise
1: Sleep alert interrupt occurred

Bit 6 **WAKEIF**: Wake-up alert interrupt bit
0: Otherwise

1: Wake-up interrupt occurred

Bit 5 **HSYMTMRIF**: Half symbol timer interrupt bit
0: Otherwise
1: Half symbol timer interrupt occurred

Bit 4 **SECIF**: Security key request interrupt bit
0: Otherwise
1: Security key request interrupt occurred

Bit 3 **RXIF**: RX receive interrupt bit
0: Otherwise
1: RX receive interrupt occurred

Bit 2 **TXG2IF**: TX GTS2 FIFO transmission interrupt bit
0: Otherwise
1: GTS2 transmission interrupt occurred

Bit 1 **TXG1IF**: TX GTS1 FIFO transmission interrupt bit
0: Otherwise
1: GTS1 transmission interrupt occurred

Bit 0 **TXNIF**: TX Normal FIFO transmission interrupt bit
0: Otherwise
1: TX Normal FIFO transmission interrupt occurred

LREG0x211 CLKIRQCR

LREG0x211, CLKIRQCR							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
Reserved						IRQPOL	CLK32KOFF
--						R/W-0	R/W-0

Bit 1 **IRQPOL**: Interrupt edge polarity bit
0: Falling edge
1: Rising edge

Bit 0 **CLK32KOFF**: SLPCLK disable bit
0: Enable
1: Disable

4.2.6. External Power Amplifier Configuration

Set LREG0x22F to 0x0F to enable PA function. This register setting integrates the PA enable and RF Switch Control (TX branch, RX branch) by utilizing pin GPIO0, pin GPIO1, and pin GPIO2. If UZ2400 is in TX mode, the pin GPIO0 (enable the external PA) and pin GPIO1 (TX branch enable) will be pulled HIGH, and the pin GPIO2 (RX branch enable) will be pulled LOW automatically. If UZ2400 is in RX mode, the pin GPIO0 and pin GPIO1 will be pulled LOW, and the pin GPIO2 will be pulled HIGH automatically. That is, it automatically changes the status of the external PA and the TX/RX branch corresponding to the UZ2400 TX or RX modes.

- TX mode: GPIO0 HIGH, GPIO1 HIGH, GPIO2 LOW
- RX mode: GPIO0 LOW, GPIO1 LOW, GPIO2 HIGH

LREG0x22F TESTMODE

LREG0x22F, TESTMODE							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
reserved			RSSIWAIT		TESTMODE		
			R/W-0b01		R/W-000		

Bit 4-3 **RSSIWAIT**: RSSI state machine parameter.
0b01 is the optimized value.

Bit 2-0 **TESTMODE**: UZ2400 test mode using GPIO
0b101: Single-tone test mode.
0b111: GPIO0, GPIO1, GPIO2 are configured to control external PA, LNA or switch as discussed above.

4.2.7. Turbo Mode Configuration

UZ2400 provides a Turbo mode to transmit and receive data at a higher rate of 625kbps compared to the standard 250kbps. That is, the data rate is 2.5 times faster than the IEEE 802.15.4-2003. Turbo mode provides an added capability for applications which require a higher data rate. The application circuit does not need any modification for Turbo mode application.

To use UZ2400 Turbo mode, the following registers need to be configured as below.

Address mode	Addr	Register Name	Descriptions	Setting Value(hex)
SREG	0x38	BBREG0	Enable Turbo mode	0x01
SREG	0x3B	BBREG3	Configure baseband circuit	0x58
SREG	0x3C	BBREG4	Configure baseband circuit	0x5C
SREG	0x2A	SOFTRST	Reset baseband circuit	0x02

SREG0x38 BBREG0

SREG0x38, BBREG0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
reserved							TURBO
reserved							R/W-0

Bit 0 **TURBO**: enable UZ2400 625kbps Turbo mode
1: Turbo mode
0: Normal mode

SREG0x3B BBREG3

SREG0x3B, BBREG3							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
PREVALIDTH				PREDETTH			reserved
R/W-1101				R/W-100			

Bit 7-4 **PREVALIDTH**: Baseband decoder parameter
1101: normal mode (250kbps) optimized value
0011: turbo mode (625kbps) optimized value
Do not use other values

Bit 3-1 **PREDETTH**: Baseband decoder parameter
100 is the optimized value for both the normal and the turbo modes.

SREG0x3C BBREG4

SREG0x3C, BBREG4							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
CSTH			PRECNT			TXDACEDGE	RXADCEDGE
R/W-100			R/W-111			R/W-0	R/W-0

Bit 7-5 **CSTH**: Baseband decoder parameter.
100: normal mode (250kbps) optimized value
010: turbo mode (625kbps) optimized value
Do not use other values

Bit 4-2 **PRECNT**: Baseband decoder parameter
111 is the optimized value for both the normal and the turbo mode.

Bit 1 **TXDACEDGE**: Tx DAC latch time selection.
1: DAC latch the I/Q data at clock negative edge
0: DAC latch the I/Q data at clock positive edge

Bit 0 **RXADCEDGE**: Rx ADC latch time selection
1: ADC value is latched at clock negative edge
0: ADC value is latched at clock positive edge

4.3. Typical TX Operations

The TXMAC inside the UZ2400 will automatically generate the preamble and Start-of-Frame delimiter fields when transmitting. Additionally, the TXMAC can generate any padding (if needed), and the CRC, if configured to do so. The host MCU must generate and write all other frame fields into the buffer memory for transmission described as followings.

4.3.1. Transmit Packet in Normal FIFO

To send a packet in normal FIFO, there are several steps to follow:

Step 1.

Fill in Normal FIFO with packet to send. FCS or MIC is not necessary. The format is as follows

LSB			MSB
1 Byte	1 Bytes	N Bytes	N Bytes
Header length	Frame length	Header	Payload

Table 16 Normal FIFO format

Step 2.

Set ackreq (SREG0x1B[2]) if acknowledgement from the receiver is required. If Ackreq is set, UZ2400 automatically retransmit the packet if there is no acknowledgement sent back. UZ2400 will retransmit the packet till the Max trial times specified by IEEE 802.15.4 is reached.

Step 3.

Set the trigger bit (SREG0x1B[0]) to send packet. This bit will be automatically cleared. At this time, TXMAC will perform CSMA-CA and send the packet at the right moment.

Step 4.

Wait for the interrupt/status (SREG0x31[0])

Step 5.

If retransmit is required, check SREG0x24[0] to see if it is successful. "Successful" means that the ACK was received. If no retransmission is required, SREG0x31[0] indicates the packet is transmitted. Retransmission times can be read at SREG0x24[7:6].

SREG0x1B TXNTRIG

SREG0x1B, TXNTRIG							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
reserved			PENDACK	INDIRECT	TXNACKREQ	TXNSECEN	TXNTRIG
-			R-0	R/W-0	R/W-0	R/W-0	WT-0

Bit 4 **PENDACK**: Indication of incoming ACK packet with pending-bit set to '1'.

Bit 3 **INDIRECT**: Activate indirect transmission – coordinator only.

Bit 2 **TXNACKREQ**: Transmit a packet with ACK packet expected. If ACK is not received, UZ2400 retransmits.

Bit 1 **TXNSECEN**: Transmit a packet which needs to be encrypted

Bit 0 **TXNTRIG**: Trigger TXMAC to transmit the packet inside TX normal FIFO.

SREG0x24 TXSR

SREG0x24, TXSR							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXRETRY		CCAFAIL	TXG2FNT	TXG1FNT	TXG2S	TXG1S	TXNS
R-0b00		R-0	R-0	R-0	R-0	R-0	R-0

Bit 7-6 **TXRETRY**: Retry times of the most recent TXNFIFO transmission.

Bit 5 **CCAFAIL**: Channel busy causes CSMA-CA fails.

Bit 4 **TXG2FNT**: GTS2 FIFO transmission fails due to not enough time before end of GTS.
Bit 3 **TXG1FNT**: GTS1 FIFO transmission fails due to not enough time before end of GTS.
Bit 2 **TXG2S**: GTS2 FIFO release status
1: Fail (retry count exceed)
0: OK
Bit 1 **TXG1S**: GTS1 FIFO release status
1: Fail (retry count exceed)
0: OK
Bit 0 **TXNS**: Normal FIFO release status
1: Fail (retry count exceed)
0: OK

4.3.2. Transmit Packet in GTS FIFO

This section describes how to trigger GTS FIFO to send the packet. As for the setting using GTS in the beacon mode, please refer to Section 4.5. To send a packet in GTS FIFO, there are several steps to follow:

Step 1.
Fill in GTS FIFO with packet to send. FCS or MIC is not necessary. The format is the same as normal FIFO.

Step 2.
Set Ackreq(SREG0x1C[2], SREG0x1D[2]) if re-transmission is required. If Ackreq is set, UZ2400 automatically retransmit the packet for which there is no acknowledgement sent back. UZ2400 will retransmit the packet till the Max trial times specified by IEEE 802.15.4 is reached or the CFP is ended.

Step 3.
Set the corresponding GTS slot number to decide when to send this packet in FIFO. (SREG0x1C[5:3], SREG0x1D[5:3])

Step 4.
Set the retransmission time at SREG0x1C[7:6] or SREG0x1D[7:6].

Step 5.
Set the trigger bit (SREG0x1C[0], SREG0x1D[0]) to send the packet. This bit will be automatically cleared. At this time, TXMAC will wait until the corresponding GTS slot sends the packet at that moment.

Step 6.
Wait for the interrupt/status (SREG0x31[1], SREG0x31[2])

Step 7.
If retransmit is required, check SREG0x24[1] or SREG0x24[2] to see if it is successful. "Successful" means that ACK was received. If no retransmission is required, SREG0x31[1] or SREG0x31[2] indicates the packet is transmitted. Retransmission times can be read at SREG0x1C[7:6] or SREG0x1D[7:6].

SREG0x1C TXG1TRIG

SREG0x1C, TXG1TRIG							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXG1IFETRY		TXG1SLOT			TXG1ACKREQ	TXG1SECEN	TXG1TRIG
R/W-0b00		R/W-0b000			R/W-0	R/W-0	WT-0

Bit 7-6 **TXG1IFETRY**: Retry times of GTSFIFO1
Write: limited retry times of the packet
Read: retry times of the successfully transmitted packet

Bit 5-3 **TXG1SLOT**: GTS slot that GTSFIFO1 occupies

Bit 2 **TXG1ACKREQ**: Transmit a packet with ACK packet expected. If ACK is not received, UZ2400 retransmits.

Bit 1 **TXG1SECEN**: Transmit a packet which needs to be encrypted

Bit 0 **TXG1TRIG**: Trigger TXMAC to transmit the packet inside TX GTS1 FIFO.

SREG0x1D TXG2TRIG

SREG0x1D, TXG2TRIG							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXG2IFETRY		TXG2SLOT			TXG2ACKREQ	TXG2SECEN	TXG2TRIG
R/W-0b00		R/W-0b000			R/W-0	R/W-0	WT-0

Bit 7-6 **TXG2IFETRY**: Retry times of GTSFIFO2
Write: limited retry times of the packet
Read: retry times of the successfully transmitted packet

Bit 5-3 **TXG2SLOT**: GTS slot that GTSFIFO2 occupies

Bit 2 **TXG2ACKREQ**: Transmit a packet with ACK packet expected. If ACK is not received, UZ2400 retransmits.

Bit 1 **TXG2SECEN**: Transmit a packet which needs to be encrypted

Bit 0 **TXG2TRIG**: Trigger TXMAC to transmit the packet inside TX GTS2 FIFO.

4.3.3. Transmit Packet in Beacon FIFO

To send a packet in beacon FIFO, there are several steps to follow:

Step 1.
Fill in Beacon FIFO with packet to send. FCS or MIC is not necessary. The format is the same as the normal FIFO.

Step 2.
Set the trigger bit (SREG1B[0]) to send the packet This bit will be automatically cleared.

Step 3.
In non-beacon enable mode, beacon FIFO is prior to normal FIFO. In beacon-enable mode, beacon will be sent at the beginning of the Superframe. There is no successful status is to be read.

4.3.4. Transmit Packet with Security Encryption

To send a secured packet TXFIFO, there are several steps to follow:

Step 1.
Fill in one of the four TXFIFOs that you want to send with encryption. The format is the same as the normal FIFO.

Step 2.
Fill in the corresponding key into the key table memory

Normal FIFO key	LREG: 0x280 – 0x28F
GTS1 FIFO key	LREG: 0x290 – 0x29F
GTS2/Beacon FIFO key	LREG: 0x2A0 – 0x2AF

Step 3.
Fill in cipher mode

Normal FIFO cipher mode	SREG0x2C[2:0]
Beacon FIFO cipher mode	SREG0x2D[6:4]
GTS1 FIFO cipher mode	SREG0x37[2:0]
GTS2 FIFO cipher mode	SREG0x37[5:3]

Step 4.
Trigger to encrypt the content in the FIFO and send it

Normal FIFO	SREG0x1B[1:0] = "11"
Beacon FIFO	SREG0x1A[1:0] = "11"
GTS1 FIFO	SREG0x1C[1:0] = "11"
GTS2 FIFO	SREG0x1D[1:0] = "11"

Step 5.

Wait for FIFO to release the interrupt/status as plaintext packet does.

SREG0x2C SECCR0

SREG0x2C, SECCR0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SECIGNORE	SECSTART	RXCIPHER			TXNCIPHER		
WT-0	WT-0	R/W-0b000			R/W-0b000		

Bit 7 **SECIGNORE**: set this bit to ignore the decryption process when there is no matching key for the incoming packet.

Bit 6 into **SECSTART**: set this bit to start the decryption process when a matching key is found and written the security key FIFO.

Bit 5-3 **RXCIPHER**: select one of the seven cipher modes below for RX packet in RXFIFO.

0b000: None
0b001: AES-CTR
0b010: AES-CCM-128
0b011: AES-CCM-64
0b100: AES-CCM-32
0b101: AES-CBC-MAC-128
0b110: AES-CBC-MAC-64
0b111: AES-CBC-MAC-32

Bit 2-0 **TXNCIPHER**: select one of the seven cipher modes below for TX packet in TX normal FIFO. The mode settings are the same as RXCIPHER.

SREG0x2D SECCR1

SREG0x2D, SECCR1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
reserved	TXBCIPHER			SNIFMODE	reserved	DISDEC	DISENC
	R/W-0			R/W-0		R/W-0	R/W-0

Bit 6-4 **TXBCIPHER**: TX cipher mode selection of beacon FIFO.

0x0: None
0x1: AES-CTR
0x2: AES-CCM-128
0x3: AES-CCM-64
0x4: AES-CCM-32
0x5: AES-CBC-MAC-128
0x6: AES-CBC-MAC-64
0x7: AES-CBC-MAC-32

Bit 3 **SNIFMODE**: Sniffer mode. Note: Set this bit "0" when using the 16-bit half-symbol timer.

Bit 1 **DISDEC**: Disable the decryption process. Even if the "security" bit in MAC header is detected, UZ2400 does not generate a security interrupt

Bit 0 **DISENC**: Disable encryption process. Even if TX security is enabled, UZ2400 does not encrypt.

SREG0x37 SECCR2

SREG0x37, SECCR2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
UPDEC	UPENC	TXG2CIPHER			TXG1CIPHER		
WT-0	WT-0	R/W-0b000			R/W-0b000		

Bit 7 **UPDEC**: Upper security decryption mode. Set this bit when doing upper decryption using TX normal FIFO.

Bit 6 **UPENC**: Upper security encryption mode. Set this bit when doing upper encryption using TX normal FIFO.

Bit 5-3 **TXG2CIPHER**: TX cipher mode selection of GTS 2 FIFO. The mode settings are the same as those for RXCIPHER.

Bit 2-0 **TXG1CIPHER**: TX cipher mode selection of GTS 1 FIFO. The mode settings are the same as those for RXCIPHER.

4.4. Typical RX Operations

UZ2400 RX PHY filters all incoming signal and tracks the synchronization symbols. When preamble of an IEEE802.15.4 packet is found, the packet is demodulated and stored in the RXFIFO. At the same time, RXMAC starts calculating the frame FCS byte by byte and checking after having received a whole packet.
In the normal mode, RXMAC filters the MAC header and skips those packets not being sent to own addresses. If the packet is acceptable and needs an acknowledgement, RXMAC will inform TXMAC to send ACK packet automatically. In the promiscuous mode, the RXMAC receives all packets with correct FCS. In the error mode, the RXMAC will receive all packets.

4.4.1. Receive Packet in RXFIFO

LSB					MSB
1 Byte	N Byte	N Bytes	2 Byte	1 Byte	1 Byte
Frame length	Header	Payload	FCS	LQI	RSSI

Frame length (in bytes) includes the header, the payload and FCS (2 bytes), it does not include LQI(1 byte) and RSSI(1 byte). When a packet passes the baseband filtering (preamble and delimiter), it goes into RXMAC. RXMAC performs several levels of packet filtering. Default mode is the address-recognition mode, which can filter those packets not being sent to this device and/or others conforming to IEEE 802.15.4-2003 Section 7.5.6.2 specifications. Promiscuous mode will receive all packets with successful FCS. The error mode will receive all packets passing the baseband filtering (SREG0x00[1:0]). RXMAC can further filter "Command Only", "Beacon Only" and "Data Only" packets at SREG0x0D[3:1]. When a received packet passes the filters discussed above and has the correct FCS, an "RXOK interrupt" is issued at SREG0x31[3]. The host MCU can read the whole packet inside the RXFIFO. The RXFIFO is flushed when the first and the last byte of the

received packet is read or the host triggers a "RX flush" at SREG0x0D[0].

4.4.2. Receive Packet with Security Decryption

Configure UZ2400 to receive and decrypt ciphered packet can be done by the following steps:

Step 1.

When a packet comes with the security enabled bit set in the frame control field of the packet header, an security interrupt (SREG0x31[4]) is issued right after the complete packet header is received. Security interrupt indicates the host MCU that the coming packet needs to be properly deciphered. Then the host MCU should perform the key searching and fill in the key table in RXFIFO register.

RXFIFO key	LREG: 0x2B0 – 0x2BF

Besides setting RXFIFO key, the host MCU should also perform cipher mode decision and set the corresponding cipher mode in SREG0x2C[5:3].

Step 2.

After both the key and cipher modes are set, the security engine should be configured and enabled by properly setting SREG0x2C. If the RXFIFO key does not match with the received packet, the following decryption process should be disabled by setting SECIGNORE (SREG0x2C[7]). Security engine can be enabled by setting SECSTART (SREG0x2C[6]).

Step 3.

After the packet is successfully decrypted, RX interrupt is issued to the host MCU to notify that the whole receiving and decryption process has been done correctly.

SREG0x2C SECCR0

SREG0x2C, SECCR0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SECIGNORE	SECSTART	RXCIPHER			TXNCIPHER		
WT-0	WT-0	R/W-0			R/W-0		

Bit 7 **SECIGNORE**: set this bit to ignore the decryption process when there is no matching key can be found for the incoming packet.

Bit 6 **SECSTART**: set this bit to start the decryption process when a matching key is found and write into the security key FIFO.

Bit 5-3 **RXCIPHER**: select one of the seven cipher modes below for RX packet in RXFIFO.

0x0: None
0x1: AES-CTR
0x2: AES-CCM-128
0x3: AES-CCM-64
0x4: AES-CCM-32
0x5: AES-CBC-MAC-128

0x6: AES-CBC-MAC-64
0x7: AES-CBC-MAC-32

Bit 2-0 **TXNCIPHER**: select one of the seven cipher modes for TX packet in TX normal FIFO. The mode settings are the same as those for RXCIPHER.

4.5. Beacon Mode Operations

4.5.1. Beacon Mode Setting

Beacon Mode for Coordinator

Step 1.

Configure the UZ2400 to the slotted mode by setting SREG0x11[5] to "1".

Step 2.

Configure the UZ2400 as the PAN Coordinator by setting SREG0x00[3] to "1".

Step 3.

Prepare the beacon frame content and fill in the TxBeacon FIFO.

Step 4.

Calibrate the sleep clock frequency:

- First, users need to select the source of the sleep clock. If the internal sleep clock is used, set LREG0x207[7:6] to "10". Or if an external crystal is used, set LREG0x207[7:6] to "01".
- UZ2400 uses a 20MHz system clock to calibrate the sleep clock frequency. To do the calibration, set LREG0x20B[4] to "1", and then keep polling LREG0x20B until LREG0x20B[7] becomes "1". After LREG0x20B[7] becomes "1", LREG0x20B[3:0], LREG0x20A, LREG0x209 form a 20-bit value C. Then the period of sleep clock (Pslowclock) can be calculated by the following equation,

$$P_{sleepclock} = \frac{50 \times C}{16}(ns)$$

- If the sleep clock frequency is higher than the expected value, users can configure LREG0x220[4:0] to slow the clock rate. The new clock period $P_{sleepclock\_new}$ is obtained by the following equation,

$$P_{sleepclock\_new} = P_{sleepclock\_ori} \times 2^{LREG0x220[4:0]}$$

Step 5.

Enable the beacon interrupt mask by setting SREG0x25[7] to "1"

Step 6

Configure the 20MHz clock recovery time by setting SREG0x35[6:0] to 0x5F. This is used for UZ2400 20MHz clock to recover from the sleep mode.

Step 7.

Calculate the main counter/remain counter according to BO and SO. Configure the BO and SO values by setting SREG0x10. After configuring BO and SO, the beacon frame will be sent immediately. For GTS setting,

please refer to Section 4.5.1.

Beacon Mode for Device

Step 1.

Configure UZ2400 to the slotted mode by setting SREG11[5] to "1".

Step 2.

Set SREG0x23 to 0x15 for more accurate timing alignment.

Step 3.

Calibrate the sleep clock frequency the same way as step 4 for the Coordinator.

Step 4.

Program the coordinator address for timing alignment at LREG0x230 ~ LREG0x239.

Step 5.

Note that a device will align a beacon frame only when the source address of the beacon frame is identical to LREG0x230~LREG0x237 (64 bits extended address mode) or LREG0x238~LREG0x239 (16 bits short address mode)

Step 6.

Parse the received beacon frame to obtain BO and SO. Calculate the main counter/remain counter according to BO and SO. For GTS setting, please refer to Section 4.5.2.

4.5.2. Beacon Mode GTS Setting

GTS for Coordinator

Step 1.

Enable GTS FIFO clock by setting SREG0x26 to 0x08.

Step 2.

Configure CAP and CFP. Program the end slot of CAP and each GTS.

- SREG0x13 for CAP and 1st GTS.
- SREG0x1E for 2nd GTS and 3rd GTS.
- SREG0x1F for 4th GTS and 5th GTS.
- SREG0x20[3:0] for 6th GTS.

Note that there is no end slot configuration for 7th GTS. This is because if 7th GTS is present, then the end slot of the 7th GTS must be 15(0x0F, the last slot of active period).

Step 3.

Enable continuous GTS FIFO switch by setting SREG0x21[1] to "1" so that whenever a GTS transmission error occurs, the GTS still switches to another FIFO. If GTS needs to stay at the current FIFO when a transmission error occurs, please ignore this step.

GTS for Devices

Step 1.

Enable GTS FIFO clock by setting SREG0x26 to 0x08.

Step 2.

Parse the received beacon frame to obtain GTS allocation information. Then program the end slot of CAP and each GTS the same way as step 2 for the Coordinator.

Step 3.

Enable continuous GTS FIFO switch by setting SREG0x21[1] to "1" so that whenever a GTS transmission error occurs, the GTS still switches to another FIFO. If GTS needs to stay at the current FIFO when a transmission error occurs, please ignore this step.

4.6. Power Saving Mode Operations

Please refer to Section 3.4 Power Management for detailed descriptions. The following provides an example setting for both the beacon-enable and non-beacon enable modes:

4.6.1. Power Saving for Non-beacon-enabled Mode

For coordinator or device to sleep 5 ms and then wake-up:

5(ms) = 163 * 30.517(us) (when Sleep clock = 32.768K) + 515*50(ns) (System clock = 20MHz)

So we have the Main-counter = 163(0xA3), Remain-counter = 515(0x203).

To ensure working under a stable 20MHz clock, it is suggested to wait for 3 ms after waked up. The combination of RFCTL[4:3] (SREG0x36[4:3]) and SLPACK[6:0] (SREG0x35[6:0]) indicates the WAKECNT value, which is waiting period, 3 ms is suggested here, divided by the sleep clock period, P_{sleep_clock}. (ms)

- P_{sleep_clock} equals to 1/32.768k in the case of using external 32.768KHz sleep clock, and the value of SLPACK (SREG0x35) is around 0x5F
- For the use of internal clock, P_{sleep_clock} needs to be derived through the calibration procedure in advance. Please refer to section 4.5.1 step 4 for the procedure

Step 1.

Set main counter, remain counter and WAKECNT

- LREG0x224 = 0x03: remain counter[7:0]
- LREG0x225 = 0x02: remain counter[9:8]
- LREG0x226 = 0xA3: main counter[7:0]
- LREG0x227 = 0x00: main counter[15:8]
- LREG0x228 = 0x00: main counter[23:16]
- {SREG0x36[4:3], SREG0x35[6:0]} = 0x5F: WAKECNT (For main clock to wake-up and stable, in this case set to 3 ms)

Step 2.

Set SLPACK to put coordinator/device to sleep.

- LREG0x229[7] = 1: Sleep ACK to put device/coordinator to sleep

4.6.2. Power Saving for Beacon-enabled Mode

The counting of the main-clock and the remain-clock are the same as the non-beacon enable mode. However, it depends on the Superframe architecture of beacon mode. The difference between the coordinator and the device in the beacon-enable mode is the counting period. For the coordinator, the period is the whole Superframe interval. For the device, the period is only for the inactive interval.

For Beacon-enabled mode, SREG0x35[7] should be set to start to sleep. While LREG0x229[7] should be set to start to sleep for Non-beacon-enabled mode.

For Superframe settings, refer to Section 4.5.2.

4.6.3. External Wake-up Mode

There are three modes for external wake-up. One is waken by external pin triggering another is waken by register triggering, and the other is by software reset.

SREG0x22[7] controls the mode switch: "1"(external pin), "0"(register).

SREG0x22 WAKECTL

SREG0x22, WAKECTL							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
IMMWAKE	REGWAKE	reserved					
R/W-0	R/W-0						

Bit 7 **IMMWAKE**: Immediate wake-up mode enables.

Bit 6 **REGWAKE**: Register-triggered wake-up signal. It should be cleared to "0" by host MCU.

Waken by External Pin

Step 1.

Configure pin 15 (WAKE) polarity,

- SREG0x0D[6] = set polarity of WAKE pin
  1d'1: active HIGH
  1d'0: active LOW
- SREG0x0D[5] = 1d'1: the external wakeup from pad mode is enable
- SREG0x22[7] = 1d'1: immediate wake-up mode enable

Step 2.

<Put device to sleep according to Section 4.6.1 or 4.6.2>

Waken by Register

Step 1.

Enable immediate wake-up

- SREG0x22[7] = 1d'1: immediate wake-up mode enable

Step 2.

<Put device to sleep according to Section 4.6.1 or 4.6.2>

Step 3.

- SREG0x22[6]=1d'1: wake up device
- SREG0x22[6]=1d'0: clear this bit to release wake-up event

4.7. Battery Monitor Operations

Step 1.

Set the battery monitor threshold at LREG0x205[7:4].

Step 2.

Enable the battery monitor by setting the LREG0x206[3] to "1".

Step 3.

Read the battery-low indicator at SREG0x30[5]. If this bit is set, it means that the supply voltage is lower than the threshold.

LREG0x205 RFCTRL5

LREG0x205, RFCTRL5							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
BATTH				reserved			
R/W-0b000				-			

Bit 7-4 **BATTH**: Battery monitor threshold value corresponding to voltage supply

0b1110 : 3.5V
0b1101 : 3.3V
0b1100 : 3.2V
0b1011 : 3.1V
0b1010 : 2.8V
0b1001 : 2.7V
0b1000 : 2.6V
0b0111 : 2.5V
Other: out of operation voltage

4.8. Upper Cipher Encryption and Decryption Operations

4.8.1. Upper Cipher Encryption

User TXNFIFO to perform the upper cipher encryption:

Step 1.
Fill in TXNFIFO with the following format:

LSB			MSB
1 Byte	1 Bytes	N Bytes	N Bytes
Header length	Frame length	Header	Payload

Step 2. Write NONCE (13 bytes) at LREG0x240~0x24C.

Step 3.
Set SREG0x37[6] = "1".

Step 4.
Set TXNFIFO security key.

Step 5.
Set the cipher mode of TXNFIFO at SREG0x2C[2:0].

Step 6.
Trigger TXNFIFO to send by setting SREG0x1B[0].

Step 7
Check ISRSTS(SREG0x31[0]="1") and TXSR(SREG0x24[0]="0"), meaning the ciphering is done.

Step 8.
Read back TXNFIFO to get the result.

4.8.2. Upper Cipher Decryption

Use TXNFIFO to perform upper cipher decryption:

Step 1.
Fill in TXNFIFO with the following format:

LSB			MSB
1 Byte	1 Bytes	N Bytes	N Bytes
Header length	Frame length	Header	Payload

Step 2.
Write NONCE (13 bytes) at LREG0x240~0x24C.

Step 3.
Set SREG0x37[7] = "1".

Step 4.
Set TXNFIFO security key.

Step 5.
Set the cipher mode of TXNFIFO at SREG0x2C[2:0].

Step 6.
Trigger TXNFIFO to send by setting SREG0x1B[0].

Step 7.
Check ISRSTS(SREG0x31[0]="1") and TXSR(SREG0x24[0]="0"), meaning the ciphering is done.

Step 8.
Read back TXNFIFO to get the result.

Step 9.
Check RXSR(SREG0x30[6]) for MIC check error. If it's '0', then it's ok.

SREG0x37 SECCR2

SREG0x37, SECCR2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
UPDEC	UPENC	TXG2CIPHER			TXG1CIPHER		
WT-0	WT-0	R/W-0			R/W-0		

Bit 7 **UPDEC**: Upper security decryption mode. Set this bit when doing the upper decryption using TX normal FIFO.

Bit 6 **UPENC**: Upper security encryption mode. Set this bit when doing the upper encryption using TX normal FIFO.

Bit 5-3 **TXG2CIPHER**: TX cipher mode selection of GTS 2 FIFO. The mode settings are the same as those for RXCIPHER.

Bit 2-0 **TXG1CIPHER**: TX cipher mode selection of GTS 1 FIFO. The mode settings are the same as those for RXCIPHER.

SREG0x2C SECCR0

SREG0x2C, SECCR0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SECIGNORE	SECSTART	RXCIPHER			TXNCIPHER		
WT-0	WT-0	R/W-0			R/W-0		

Bit 7 **SECIGNORE**: set this bit to ignore the decryption process when there is no matching key for the incoming packet.

Bit 6 **SECSTART**: set this bit to start the decryption process when a matching key is found and write into security key FIFO.

Bit 5-3 **RXCIPHER**: select one of the seven cipher modes below for RX packet in RXFIFO.
0x0: None
0x1: AES-CTR
0x2: AES-CCM-128
0x3: AES-CCM-64
0x4: AES-CCM-32
0x5: AES-CBC-MAC-128
0x6: AES-CBC-MAC-64
0x7: AES-CBC-MAC-32

Bit 2-0 **TXNCIPHER**: select one of the seven cipher modes for TX packet in TX normal FIFO. The mode settings are the same as RXCIPHER.

LREG0x240-0x24C Upper Nonce

LREG0x240-0x24C, Upper Nonce							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
UPNONCE – 13 bytes							
R/W-0							

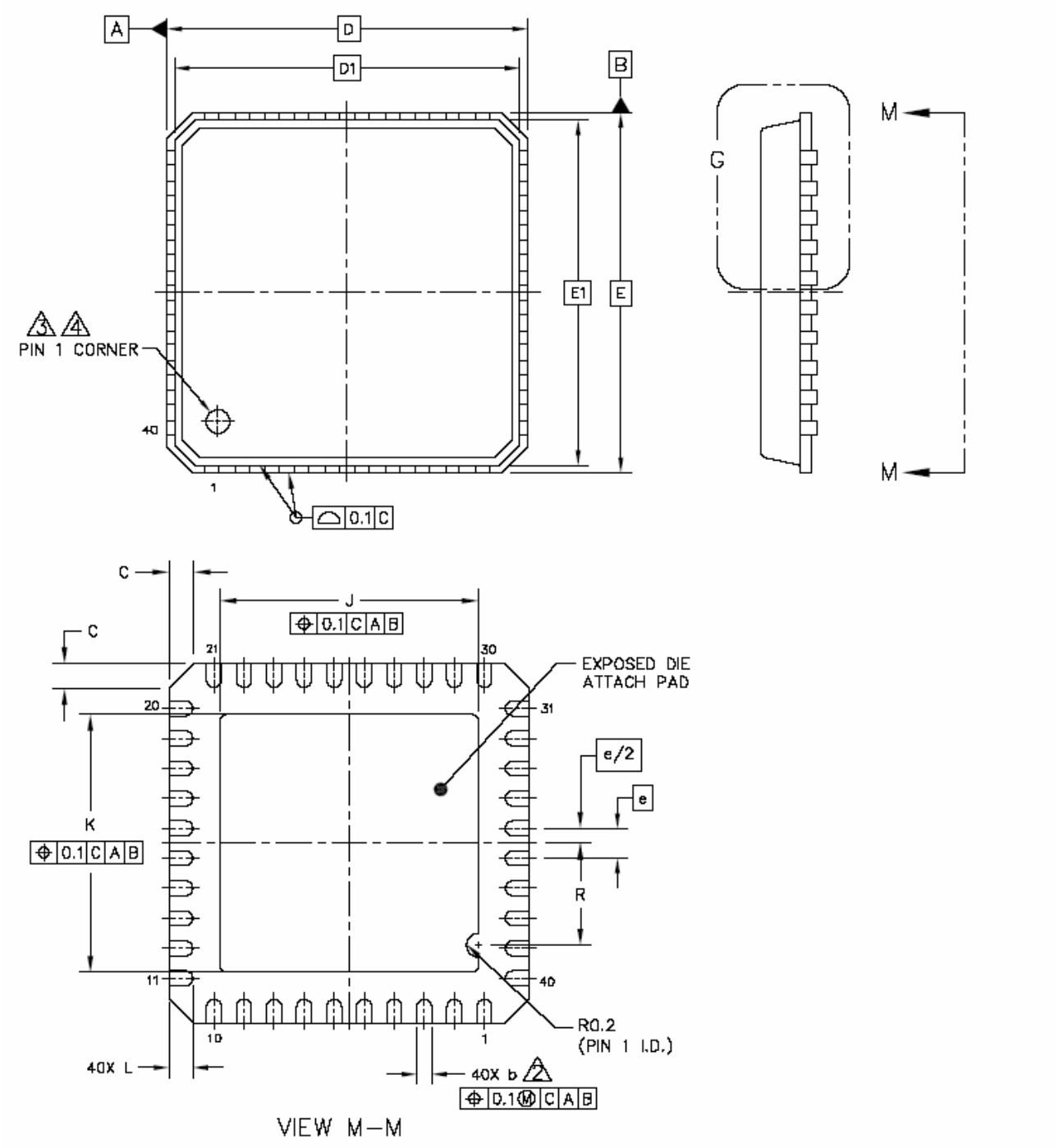
Bit 7-0 **UPNONCE**: set the 13-byte NONCE field of CCM/CCM* protocol. Refer to IEEE802.15.4-2003 ANNEC-B for detail. Generally speaking, these fields should be provided by key management protocol of the upper layer (i.e. network/application).

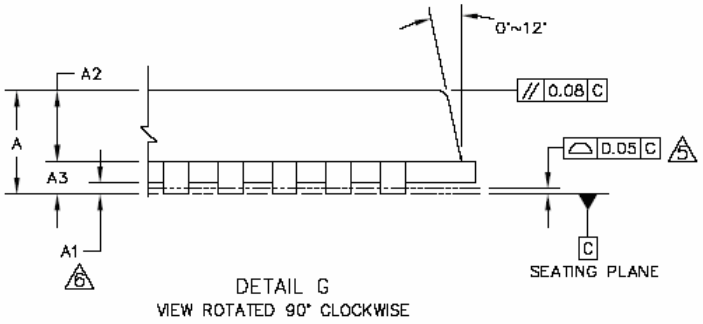
5. Package Information

5.1. Package Drawing

The QFN-40 package outline is given below.

QFN-40, 6x6mm²





DIM	MIN	NOM	MAX
A	0.8		0.9
A1	0	0.02	0.05
A2	0.65		0.69
A3		0.203 REF	
b	0.18	0.23	0.3
C	0.24	0.42	0.6
D		6 BSC	
D1		5.75 BSC	
E		6 BSC	
E1		5.75 BSC	
e		0.5 BSC	
J	4.2	4.3	4.4
K	4.2	4.3	4.4
L	0.3	0.4	0.5
R	1.6	1.7	1.8

NOTES

2. DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.2 AND 0.25mm FROM TERMINAL TIP.
3. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
4. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
5. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
6. APPLIED ONLY TO TERMINALS.

UNIT	DIMENSION AND TOLERANCES	REFERENCE DOCUMENT
UNIT	ASME_Y14.5M	JEDEC–MO–220–C

5.2. Package Soldering

5.2.1. Background

UZ2400 is housed in a small 40-pin lead-free QFN 6x6 mm2 package. The packaged part passes the Level 3 pre-condition testing.

5.2.2. Reference Reflow Temperature Curve

Figure 28 is a reference temperature curve for the SMD package IR reflow. Different equipment may have different optimized reflow conditions. The user may need to modify the reflow profile to suit the particular equipment used in order to maximize the yield.

Pb-free SMD Package IR Reflow Profile

Step#	Profile Feature	Condition / Duration
Step 1	Ramp-up rate	1.5-3℃ /sec
Step 2	Preheat : 150~ 200℃ (Ta-Tb)	t1-t2: 60~80 sec
Step 3	Ramp-up rate (T_L to T_P)	1.5-3℃ /sec
	Temperature maintained above 220℃ (T_L)	t_L : 80~150 sec
Step 4	Peak temperature (T_P)	260+0/-5℃
	Time within 5℃ of actual peak temperature	30±10 sec
Step 5	Ramp-down rate	6℃/sec. Max.
Note: Time 25℃ to peak temperature: 8 minutes max.		

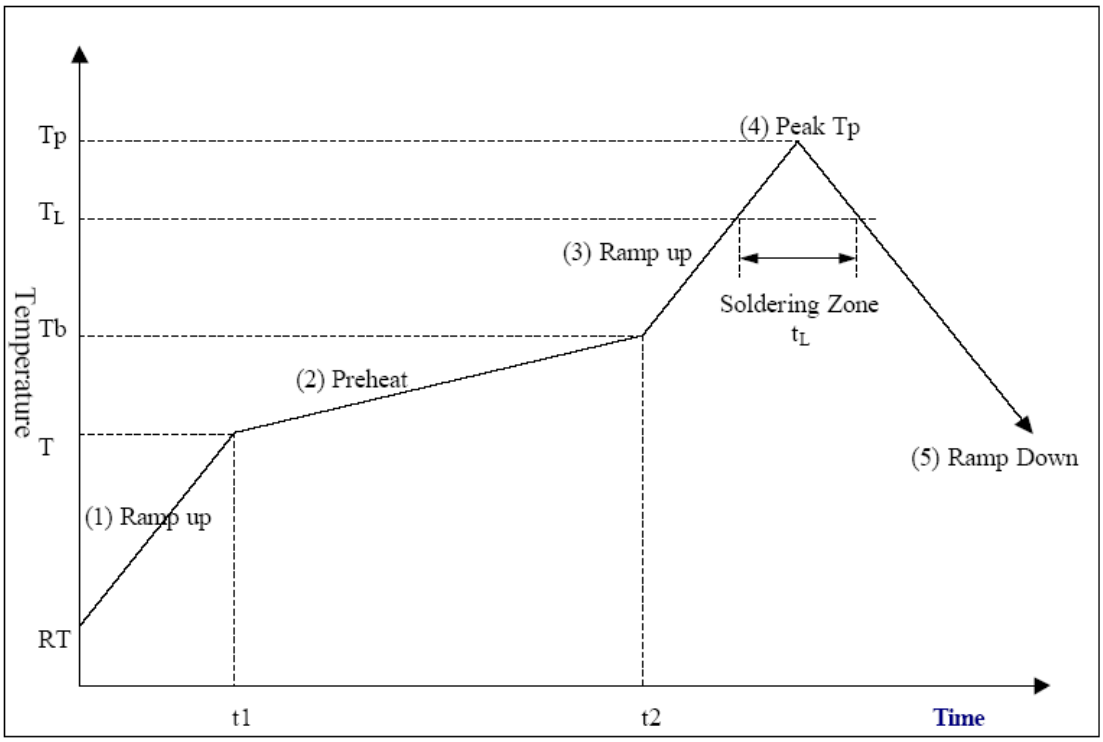


Figure 28 Reference SMD package IR reflow profile

Appendix A. RSSI Mapping Table

RSSI versus Input Power

Input Power (dBm)	RSSI (hex)	Input Power (dBm)	RSSI (hex)	Input Power (dBm)	RSSI (hex)
-100	00	-73	49	-46	D4
-99	00	-72	4E	-45	D8
-98	00	-71	53	-44	DD
-97	00	-70	59	-43	E1
-96	00	-69	5F	-42	E4
-95	00	-68	64	-41	E9
-94	00	-67	6B	-40	EF
-93	00	-66	6F	-39	F5
-92	00	-65	75	-38	FA
-91	00	-64	79	-37	FD
-90	00	-63	7D	-36	FE
-89	01	-62	81	-35	FF
-88	02	-61	85	-34	FF
-87	05	-60	8A	-33	FF
-86	09	-59	8F	-32	FF
-85	0D	-58	94	-31	FF
-84	12	-57	99	-30	FF
-83	17	-56	9F	-29	FF
-82	1B	-55	A5	-28	FF
-81	20	-54	AA	-27	FF
-80	25	-53	B0	-26	FF
-79	2B	-52	B7	-25	FF
-78	30	-51	BC	-24	FF
-77	35	-50	C1	-23	FF
-76	3A	-49	C6	-22	FF
-75	3F	-48	CB	-21	FF
-74	44	-47	CF	-20	FF

RSSI is used to report the signal strength of a received packet. UZ2400 attaches RSSI value following a received packet in RXFIFO every time a packet is received successfully. Please refer to Section 4.4.1 for the data format of RXFIFO.

Appendix B. TX Power Configuration

Default output power is 0dBm. Summation of "large" and "small" tuning decreases the output power.

LREG0x203 RFCTL3

LREG0x203, RFCTRL3							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXPOWL		TXPOWF			reserved		
R/W-0b00		R/W-0b000					

Bit 7-6 **TXPOWL**: Large scale control for TX power in dB
0b00: 0 dB
0b01: -10 dB
0b10: -20 dB
0b11: -30 dB

Bit 5-3 **TXPOWF**: Fine scale control for TX power in dB
0b000: 0 dB
0b001: -0.5 dB
0b010: -1.2 dB
0b011: -1.9 dB
0b100: -2.8 dB
0b101: -3.7 dB
0b110: -4.9 dB
0b111: -6.3 dB

Appendix C. Register Descriptions

Register Types

Register Type	Description
R/W	Read/Write register
WT	Write to trigger register, automatically cleared by hardware
RC	Read to clear register
R	Read-only register
R/W1C	Read/Write "1" to clear register

C.1 Short Registers (SREG0x00~SREG0x3F)

SREG0x31 ISRSTS

SREG0x31, ISRSTS							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SLPIF	WAKEIF	HSYMTMRIF	SECIF	RXIF	TXG2IF	TXG1IF	TXNIF
RC-0	RC-0	RC-0	RC-0	RC-0	RC-0	RC-0	RC-0

Bit 7 **SLPIF**: Sleep alert interrupt bit
0: Otherwise
1: Sleep alert interrupt occurred

SREG0x00 RXMCR

SREG0x00, RXMCR							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
reserved		NOACKRSP	reserved	PANCOORD	COORD	ERRPKT	PROMI
		R/W-0		R/W-0	R/W-0	R/W-0	R/W-0

Bit 5 **NOACKRSP**: Disable automatic acknowledge ACK response.
0: Otherwise
1: Disable automatic acknowledge
Bit 3 **PANCOORD**: Set the device as a PAN Coordinator.
Bit 2 **COORD**: Set the device as a Coordinator.
Bit 1 **ERRPKT**: Accept all kinds of packet including CRC error.
Bit 0 **PROMI**: Accept all kinds of packet with CRC OK.

SREG0x01 PANIDL

SREG0x01, PANIDL							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
PANIDL							
R/W-0x00							

Bit 7-0 **PANIDL**: The device's PAN address[7:0].

SREG0x02 PANIDH

SREG0x02, PANIDH							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
PANIDH							
R/W-0x00							

Bit 7-0 **PANIDH**: The device's PAN address[15:8].

SREG0x03 SADRL

SREG0x03, SADRL							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SADRL							
R/W-0x00							

Bit 7-0 **SADRL**: The device's 16-bit short address[7:0].

SREG0x04 SADRH

SREG0x04, SADRH							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SADRH							
R/W-0x00							

Bit 7-0 **SADRH**: The device's 16-bit short address[15:8].

SREG0x05 EADR0

SREG0x05, EADR0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
EADR0							
R/W-0x00							

Bit 7-0 **EADR0**: The device's 64-bit extended address[7:0].

SREG0x06 EADR1

SREG0x06, EADR1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
EADR1							
R/W-0x00							

Bit 7-0 **EADR1**: The device's 64-bit extended address[15:8].

SREG0x07 EADR2

SREG0x07, EADR2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
EADR2							
R/W-0x00							

Bit 7-0 **EADR2**: The device's 64-bit extended address[23:16].

SREG0x08 EADR3

SREG0x08, EADR3							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
EADR3							
R/W-0x00							

Bit 7-0 **EADR3**: The device's 64-bit extended address[31:24].

SREG0x09 EADR4

SREG0x09, EADR4							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
EADR4							
R/W-0x00							

Bit 7-0 **EADR4**: The device's 64-bit extended address[39:32].

SREG0x0A EADR5

SREG0x0A, EADR5							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
EADR5							
R/W-0x00							

Bit 7-0 **EADR5**: The device's 64-bit extended address[47:40].

SREG0x0B EADR6

SREG0x0B, EADR6							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
EADR6							
R/W-0x00							

Bit 7-0 **EADR6**: The device's 64-bit extended address[55:48].

SREG0x0C EADR7

SREG0x0C, EADR7							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
EADR7							
R/W-0x00							

Bit 7-0 **EADR7**: The device's 64-bit extended address[63:56].

SREG0x0D RXFLUSH

SREG0x0D, RXFLUSH							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
reserved	WAKEPOL	WAKEPAD	reserved	ONLYCMD	ONLYDATA	ONLYBCN	RXFLUSH
	R/W-0	R/W-0		R/W-0	R/W-0	R/W-0	WT-0

Bit 6 **WAKEPOL**: Set polarity of WAKE signal.
0: Active low
1: Active high
Bit 5 **WAKEPAD**: Turn on pad of the WAKE pin (pin 15).
Bit 3 **ONLYCMD**: Only command packet is allowed to receive.
Bit 2 **ONLYDATA**: Only data packet is allowed to receive.
Bit 1 **ONLYBCN**: Only beacon packet is allowed to receive.
Bit 0 **RXFLUSH**: Flush RXFIFO. This will not modify the data in RXFIFO but return pointers to zero. This bit is write to clear.

SREG0x10 ORDER

SREG0x10, ORDER							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
BO				SO			
R/W-0xF				R/W-0xF			

Bit 7-4 **BO**: Beacon order for how often coordinator transmit a beacon frame.
Bit 3-0 **SO**: Superframe order, specifies the length of the active portion of the superframe including the beacon frame.

0<=**SO**<=**BO**<=0xF, if **BO** is 0x0F, no beacon will be transmitted (i.e, no superframe structure). If **SO** is 0xF, there is no active portion in superframe.

SREG0x11 TXMCR

SREG0x11, TXMCR							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
NOCSMA	reserved	SLOTTED	MACMINBE		CSMABF		
R/W-0		R/W-0	0x3		0x4		

Bit 7 **NOCSMA**: No CSMA-CA algorithm when transmitting in unslotted mode with SREG0x21[1] set.
Bit 5 **SLOTTED**: Enable slotted mode.
Bit 4-3 **MACMINBE**: Minimum value of back-off exponent of CSMA-CA algorithm. Please refer to IEEE 802.15.4-2003 Table 71.
Bit 2-0 **CSMABF**: Maximum number of back-offs. Please refer to IEEE 802.15.4-2003 Table 71.

SREG0x13 SLALLOC

SREG0x13, SLALLOC							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
GTS1				CAP			
R/W-0x0				R/W-0x0			

Bit 7-4 **GTS1**: End slot number of GTS1.
Bit 3-0 **CAP**: End slot number of CAP.

SREG0x18 FIFOEN

SREG0x18, FIFOEN							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
FIFOEN	reserved	TXONTS				TXONT	
R/W-1		R/W-0x2				R/W-0x0	

Bit 7 **FIFOEN**: TXFIFO and RXFIFO output enable manual control.
1: TXFIFO and RXFIFO are always output enabled.
Note: Setting Bit7 value to "0" is forbidden, or fatal error will occur.
Bit 5-2 **TXONTS**: The last symbol number before TX. The minimum value is "1".
Bit 1-0 **TXONT**: The period that rfmode1 active before TX.

SREG0x1A TXBCNTRIG

SREG0x1A, TXBCNTRIG							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
reserved						TXBCNSECEN	TXBCNTRIG
						R/W-0	WT-0

Bit 1 **TXBCNSECEN**: Security enable for beacon FIFO.
0: Otherwise
1: Enable

Bit 0 **TXBCNTRIG**: Trigger TXMAC to send the packet in TX beacon FIFO.

SREG0x1B TXNTRIG

SREG0x1B, TXNTRIG							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
reserved			PENDACK	INDIRECT	TXNACKREQ	TXNSECEN	TXNTRIG
-			R-0	R/W-0	R/W-0	R/W-0	WT-0

Bit 4 **PENDACK**: Indication of incoming ACK packet with pending-bit set to '1'.
Bit 3 **INDIRECT**: Activate indirect transmission – coordinator only.
Bit 2 **TXNACKREQ**: Transmit a packet with ACK packet expected. If ACK is not received, UZ2400 retransmits.
Bit 1 **TXNSECEN**: Transmit a packet which needs to be encrypted
Bit 0 **TXNTRIG**: Trigger TXMAC to transmit the packet inside TX normal FIFO.

SREG0x1C TXG1TRIG

SREG0x1C, TXG1TRIG							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXG1IFETRY		TXG1SLOT			TXG1ACKREQ	TXG1SECEN	TXG1TRIG
R/W-0b00		R/W-0b000			R/W-0	R/W-0	WT-0

Bit 7-6 **TXG1IFETRY**: Retry times of GTSFIFO1
Write: limited retry times of the packet
Read: retry times of the successfully transmitted packet
Bit 5-3 **TXG1SLOT**: GTS slot that GTSFIFO1 occupies
Bit 2 **TXG1ACKREQ**: Transmit a packet with ACK packet expected. If ACK is not received, UZ2400 retransmits.
Bit 1 **TXG1SECEN**: Transmit a packet which needs to be encrypted
Bit 0 **TXG1TRIG**: Trigger TXMAC to transmit the packet inside TX GTS1 FIFO.

SREG0x1D TXG2TRIG

SREG0x1D, TXG2TRIG							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXG2IFETRY		TXG2SLOT			TXG2ACKREQ	TXG2SECEN	TXG2TRIG
R/W-0b00		R/W-0b000			R/W-0	R/W-0	WT-0

Bit 7-6 **TXG2IFETRY**: Retry times of GTSFIFO2
Write: limited retry times of the packet
Read: retry times of the successfully transmitted packet
Bit 5-3 **TXG2SLOT**: GTS slot that GTSFIFO2 occupies
Bit 2 **TXG2ACKREQ**: Transmit a packet with ACK packet expected. If ACK is not received, UZ2400 retransmits.

Bit 1 **TXG2SECEN**: Transmit a packet which needs to be encrypted

Bit 0 **TXG2TRIG**: Trigger TXMAC to transmit the packet inside TX GTS2 FIFO.

SREG0x1E ESLOTG23

SREG0x1E, ESLOTG23							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
GTS3				GTS2			
R/W-0x0				R/W-0x0			

Bit 7-4 **GTS3**: End slot number of GTS3.

Bit 3-0 **GTS2**: End slot number of GTS2.

SREG0x1F ESLOTG45

SREG0x1F, ESLOTG45							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
GTS5				GTS4			
R/W-0x0				R/W-0x0			

Bit 7-4 **GTS5**: End slot number of GTS5.

Bit 3-0 **GTS4**: End slot number of GTS4.

SREG0x20 ESLOTG67

SREG0x20, ESLOTG67							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
reserved				GTS6			
				R/W-0x0			

Bit 3-0 **GTS6**: End slot number of GTS6.

SREG0x21 TXPEND

SREG0x21, TXPEND							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
reserved						GTSSWITCH	reserved
						R/W-0	

Bit 1 **GTSSWITCH**: Continue GTS FIFO switch in CFP.

SREG0x22 WAKECTL

SREG0x22, WAKECTL							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
IMMWAKE	REGWAKE	reserved					
R/W-0	R/W-0						

Bit 7 **IMMWAKE**: Immediate wake-up mode enable.
Bit 6 **REGWAKE**: Register-triggered wake-up signal. Should be cleared to "0" by host MCU.

SREG0x24 TXSR

SREG0x24, TXSR							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXRETRY		CCAFAIL	TXG2FNT	TXG1FNT	TXG2S	TXG1S	TXNS
R-0b00		R-0	R-0	R-0	R-0	R-0	R-0

Bit 7-6 **TXRETRY**: Retry times of the most recent TXNFIFO transmission.
Bit 5 **CCAFAIL**: Channel busy causes CSMA-CA fails.
Bit 4 **TXG2FNT**: GTS2 FIFO transmission fails due to not enough time before end of GTS.
Bit 3 **TXG1FNT**: GTS1 FIFO transmission fails due to not enough time before end of GTS.
Bit 2 **TXG2S**: GTS2 FIFO release status
1: Fail (retry count exceed)
0: OK
Bit 1 **TXG1S**: GTS1 FIFO release status
1: Fail (retry count exceed)
0: OK
Bit 0 **TXNS**: Normal FIFO release status
1: Fail (retry count exceed)
0: OK

SREG0x25 TXBCNMSK

SREG0x25, TXBCNMSK							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXBCNMSK	reserved						
R/W-0							

Bit 7 **TXBCNMSK**: TX beacon FIFO interrupt mask
1: the interrupt is masked, and hence the INT pin will not change even if an interrupt occurs.
0: the interrupt is not masked.

SREG0x26 GATECLK

SREG0x26, GATECLK							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
reserved				ENGTS	reserved		
				R/W-0			

Bit 3 **ENGTS**: Always enable GTS clock.

SREG0x28 HSYMTMR0

SREG0x28, HSYMTMR0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
Half-symbol tick timer low byte [7:0]							
R/W-0x00							

Bit 7:0 **HSYMTMR0**: Low byte of 16-bit half-symbol timer.

SREG0x29 HSYMTMR1

SREG0x29, HSYMTMR1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
Half-symbol tick timer low byte [15:8]							
R/W-0x00							

Bit 7:0 **HSYMTMR1**: High byte of 16-bit half-symbol timer.

SREG0x2A SOFTRST

SREG0x2A, SOFTRST							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
reserved					RSTPWR	RSTBB	RSTMAC
					WT-0	WT-0	WT-0

Bit 2 **RSTPWR**: Power management reset
Write "1" to perform reset.

Bit 1 **RSTBB**: Baseband reset
Write "1" to perform reset.

Bit 0 **RSTMAC**: MAC reset
Write "1" to perform reset.

SREG0x2C SECCR0

SREG0x2C, SECCR0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SECIGNORE	SECSTART	RXCIPHER			TXNCIPHER		
WT-0	WT-0	R/W-0b000			R/W-0b000		

Bit 7 **SECIGNORE**: set this bit to ignore the decryption process when there is no matching key for the incoming packet.

Bit 6 **SECSTART**: set this bit to start the decryption process when a matching key is found and written into the security key FIFO.

Bit 5-3 **RXCIPHER**: select one of the seven cipher modes below for RX packet in RXFIFO.
0b000: None
0b001: AES-CTR
0b010: AES-CCM-128
0b011: AES-CCM-64
0b100: AES-CCM-32
0b101: AES-CBC-MAC-128
0b110: AES-CBC-MAC-64
0b111: AES-CBC-MAC-32

Bit 2-0 **TXNCIPHER**: select one of the seven cipher modes below for TX packet in TX normal FIFO. The mode settings are the same as RXCIPHER.

SREG0x2D SECCR1

SREG0x2D, SECCR1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
reserved	TXBCIPHER			SNIFMODE	reserved	DISDEC	DISENC
	R/W-0b000			R/W-0		R/W-0	R/W-0

Bit 6-4 **TXBCIPHER**: TX cipher mode selection of beacon FIFO.
0b000: None
0b001: AES-CTR
0b010: AES-CCM-128
0b011: AES-CCM-64
0b100: AES-CCM-32
0b101: AES-CBC-MAC-128
0b110: AES-CBC-MAC-64
0b111: AES-CBC-MAC-32

Bit 3 **SNIFMODE**: Sniffer mode. Note: Set this bit "0" when using the 16-bit half-symbol timer.

Bit 1 **DISDEC**: Disable the decryption process. Even if the "security" bit in MAC header is detected, UZ2400 does not generate a security interrupt

Bit 0 **DISENC**: Disable encryption process. Even if TX security is enabled, UZ2400 does not encrypt.

SREG0x2E TXPEMISP

SREG0x2E, TXPEMISP							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXPET				MISP			
R/W-0111				R/W-0101			

Bit 7-4 **TXPET**: For VCO circuit calibration.
Bit 3-0 **MISP**: For CSMA-CA and GTS circuit calibration.

The recommend value for TXPEMISP is 0x95. Please do not use other values for this register.

SREG0x30 RXSR

SREG0x30, RXSR							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
reserved	UPSECERR	BATIND	reserved				
	R/W1C-0	R-0					

Bit 6 **UPSECERR**: MIC error in upper layer security mode.
Bit 5 **BATIND**: Low-battery indicator.

SREG0x31 ISRSTS

SREG0x31, ISRSTS							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SLPIF	WAKEIF	HSYMTMRIF	SECIF	RXIF	TXG2IF	TXG1IF	TXNIF
RC-0	RC-0	RC-0	RC-0	RC-0	RC-0	RC-0	RC-0

Bit 7 **SLPIF**: Sleep alert interrupt bit
0: Otherwise
1: Sleep alert interrupt occurred
Bit 6 **WAKEIF**: Wake-up alert interrupt bit
0: Otherwise
1: Wake-up interrupt occurred
Bit 5 **HSYMTMRIF**: Half symbol timer interrupt bit
0: Otherwise
1: Half symbol timer interrupt occurred
Bit 4 **SECIF**: Security key request interrupt bit
0: Otherwise
1: Security key request interrupt occurred
Bit 3 **RXIF**: RX receive interrupt bit
0: Otherwise
1: RX receive interrupt occurred
Bit 2 **TXG2IF**: TX GTS2 FIFO transmission interrupt bit
0: Otherwise

1: GTS2 transmission interrupt occurred

Bit 1 **TXG1IF**: TX GTS1 FIFO transmission interrupt bit
0: Otherwise
1: GTS1 transmission interrupt occurred

Bit 0 **TXNIF**: TX Normal FIFO transmission interrupt bit
0: Otherwise
1: TX Normal FIFO transmission interrupt occurred

SREG0x32 INTMSK

SREG0x32, INTMSK							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SLPMSK	WAKEMSK	HSYMTMRMSK	SECMSK	RXMSK	TXG2MSK	TXG1MSK	TXNMSK
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 7 **SLPMSK**: Sleep alert interrupt mask
Bit 6 **WAKEMSK**: Wake-up alert interrupt mask
Bit 5 **HSYMTMRMSK**: Half symbol timer interrupt mask
Bit 4 **SECMSK**: security interrupt mask
Bit 3 **RXMSK**: RX receive interrupt mask
Bit 2 **TXG2MSK**: TX GTS2 FIFO transmission interrupt mask
Bit 1 **TXG1MSK**: TX GTS1 FIFO transmission interrupt mask
Bit 0 **TXNMSK**: TX Normal FIFO transmission interrupt mask
1: the interrupt is masked, and hence the INT pin will not change even if an interrupt occurs.
0: the interrupt is not masked.

SREG0x33 GPIO

SREG0x33, GPIO							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
reserved		GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 5 **GPIO5**: The status of GPIO5. Both read and write operations are allowed.
Bit 4 **GPIO4**: The status of GPIO4. Both read and write operations are allowed.
Bit 3 **GPIO3**: The status of GPIO3. Both read and write operations are allowed.
Bit 2 **GPIO2**: The status of GPIO2. Both read and write operations are allowed.
Bit 1 **GPIO1**: The status of GPIO1. Both read and write operations are allowed.
Bit 0 **GPIO0**: The status of GPIO0. Both read and write operations are allowed.

SREG0x34 SPIGPIO

SREG0x34, SPIGPIO							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SPIMODE		GPDIR5	GPDIR4	GPDIR3	GPDIR2	GPDIR1	GPDIR0
R/W-0b00		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 7-6 **SPIMODE**: Select the mode for SPI interface.
0b00: Normal SPI mode
0b01: PLUS SPI mode
0b10: Enhanced SPI mode
Bit 5 **GPDIR5**: The direction of GPIO5.
Bit 4 **GPDIR4**: The direction of GPIO4.
Bit 3 **GPDIR3**: The direction of GPIO3.
Bit 2 **GPDIR2**: The direction of GPIO2.
Bit 1 **GPDIR1**: The direction of GPIO1.
Bit 0 **GPDIR0**: The direction of GPIO0.
0: Input direction
1: Output direction

SREG0x35 SLPACK

SREG0x35, SLPACK							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SLPACK	WAKECNT						
WT-0	R/W-0000000						

Bit 7 **SLPACK**: Sleep acknowledge. Set this bit to "1" will cause UZ2400 enter the sleep mode immediately. This bit will be automatically cleared to "0".
Bit 3-0 **WAKECNT**: System clock (20MHz) recovery time
Note: In the initial procedure, set **WAKECNT** to 0x5F to optimize the performance.

SREG0x36 RFCTL

SREG0x36, RFCTL							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
reserved			WAKECNTEXT		RFRST	RFTXMODE	RFRXMODE
			R/W-00		R/W-0	R/W-0	R/W-0

Bit 4 -3 **WAKECNTEXT**: 20MHz clock recovery time extension bits
Bit 2 **RFRST**: RF state reset.
Reset RF state. RF state must be reset in order to change the RF channels.
Write "1" and then write "0" to accomplish the reset operation.
Bit 1 **RFTXMODE**: RF is forced into TX mode.
Bit 0 **RFRXMODE**: RF is forced into RX mode

SREG0x37 SECCR2

SREG0x37, SECCR2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
UPDEC	UPENC	TXG2CIPHER			TXG1CIPHER		
WT-0	WT-0	R/W-0b000			R/W-0b000		

Bit 7 **UPDEC**: Upper security decryption mode. Set this bit when doing upper decryption using TX normal FIFO.

Bit 6 **UPENC**: Upper security encryption mode. Set this bit when doing upper encryption using TX normal FIFO.

Bit 5-3 **TXG2CIPHER**: TX cipher mode selection of GTS 2 FIFO. The mode settings are the same as those for RXCIPHER.

Bit 2-0 **TXG1CIPHER**: TX cipher mode selection of GTS 1 FIFO. The mode settings are the same as those for RXCIPHER.

SREG0x38 BBREG0

SREG0x38, BBREG0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
reserved							TURBO
							R/W-0

Bit 0 **TURBO**: enable UZ2400 625kbps Turbo mode
1: Turbo mode
0: Normal mode

SREG0x39 BBREG1

SREG0x39, BBREG1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
reserved					RXDECODEINVERSION	reserved	
					R/W-0		

Bit 2 **RXDECODEINVERSION**: 1: RX decoded symbol sign invert

SREG0x3A BBREG2

SREG0x3A, BBREG2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
CCAMODE		CCATH				reserved	
R/W-0b01		0b0010					

Bit 7-6 **CCAMODE**: CCA mode selection
00: reserved
01: Carrier sense (CS) mode, detect IEEE 802.15.4 signals

10: Energy detection (ED) mode, detect in-band signals
11: Combination of carrier sense mode and energy detection mode

Bit 5-2 **CCATH**: CCA carrier sense threshold
NOTE: suggested value is 0b1110

SREG0x3B BBREG3

SREG0x3B, BBREG3							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
PREVALIDTH				PREDETTH			reserved
R/W-0b1101				R/W-0b100			

Bit 7-4 **PREVALIDTH**: Baseband decoder parameter
0b1101: normal mode (250kbps) optimized value
0b0011: turbo mode (625kbps) optimized value
Do not use other values

Bit 3-1 **PREDETTH**: Baseband decoder parameter
0b100 is the optimized value for both the normal and the turbo modes.

SREG0x3C BBREG4

SREG0x3C, BBREG4							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
CSTH			PRECNT			TXDACEDGE	RXADCEDGE
R/W-100			R/W-111			R/W-0	R/W-0

Bit 7-5 **CSTH**: Baseband decoder parameter.
100: normal mode (250kbps) optimized value
010: turbo mode (625kbps) optimized value
Do not use other values

Bit 4-2 **PRECNT**: Baseband decoder parameter
111 is the optimized value for both the normal and the turbo mode.

Bit 1 **TXDACEDGE**: Tx DAC latch time selection.
1: DAC latch the I/Q data at clock negative edge
0: DAC latch the I/Q data at clock positive edge

Bit 0 **RXADCEDGE**: Rx ADC latch time selection
1: ADC value is latched at clock negative edge
0: ADC value is latched at clock positive edge

SREG0x3E BBREG6

SREG0x3E, BBREG6							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
RSSIMODE1	RSSIMODE2	reserved					RSSIRDY
WT-0	R/W-0						R-1

Bit 7 **RSSIMODE1**: RSSI mode 1 enable
1: calculate RSSI for firmware request, will be clear to "0" when RSSI calculation is finished.
Bit 6 **RSSIMODE2**: RSSI mode 2 enable
1: calculate RSSI for each received packet, the RSSI value will be stored in RXFIFO.
0: no RSSI calculation for received packet.
Bit 0 **RSSIRDY**: RSSI ready signal for **RSSIMODE1** use
If **RSSIMODE1** is set, this bit will be cleared to "0" until RSSI calculation is done. When RSSI calculation is finished and the RSSI value is ready, this bit will be set to "1" automatically.

SREG0x3F BBREG7

SREG0x3F, BBREG7							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
RSSITHCCA							
R/W-0x0							

Bit 7-0 **RSSITHCCA**: CCA-ED threshold

Note: If the in-band signal strength is larger than the threshold, the channel is busy. The 8-bit value can be mapped to a certain power level according to Appendix A.

C.2 Long Registers (LREG0x200~LREG0x27F)

LREG0x200 RFCTRL0

LREG0x200, RFCTRL0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
CHANNEL				RFOPT			
R/W-0b0000				R-0b0000			

Bit 7-4 **CHANNEL**: RF channel number. IEEE 802.15.4 2.4GHz band channels (11~26) are mapped as follows.
0b0000: channel 11 (2405MHz)
0b0001: channel 12 (2410MHz)
0b0010: channel 13 (2415MHz)
0b1111: channel 26 (2480MHz)
Bit 3-0 **RFOPT**: Optimize RF control
0b0010 is the recommended value for RF optimization.

LREG0x202 RFCTL2

LREG0x202, RFCTRL2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
PLLCTL	RSSIDC		RSSISLOPE		reserved		
R/W-0	R/W-0b00		R/W-0b00				

Bit 7 **PLLCTL**: RF Phase Lock Loop (PLL) control
1: the recommended value for RF optimization. This needs to be set before the RF transmission and reception.

Bit 6-5 **RSSIDC**: RSSI DC level shift.
Note: 0b11 is not allowed.

Bit 4-3 **RSSISLOPE**: RSSI range control.
Note: 0b11 is not allowed.

LREG0x203 RFCTL3

LREG0x203, RFCTRL3							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXPOWL		TXPOWF			reserved		
R/W-0b00		R/W-0b000					

Bit 7-6 **TXPOWL**: Large scale control for TX power in dB
0b00: 0 dB
0b01: -10 dB
0b10: -20 dB
0b11: -30 dB

Bit 5-3 **TXPOWF**: Fine scale control for TX power in dB
0b000: 0 dB
0b001: -0.5 dB
0b010: -1.2 dB
0b011: -1.9 dB
0b100: -2.8 dB
0b101: -3.7 dB
0b110: -4.9 dB
0b111: -6.3 dB

LREG0x205 RFCTRL5

LREG0x205, RFCTRL5							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
BATTH				reserved			
R/W-0b000				-			

Bit 7-4 **BATTH**: Battery monitor threshold value corresponding to voltage supply
0b1110 : 3.5V

0b1101 : 3.3V
0b1100 : 3.2V
0b1011 : 3.1V
0b1010 : 2.8V
0b1001 : 2.7V
0b1000 : 2.6V
0b0111 : 2.5V
Other : out of operation voltage

LREG0x206 RFCTL6

LREG0x206, RFCTL6							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TXFIL	reserved		20MRECVR	BATEN	reserved		
R/W-0			R/W-0b00	R/W-0			

Bit 7 **TXFIL**: TX filter control
1: the recommended value for RF optimization.
Bit 4 **20MRECVR**: 20MHz clock recovery time (recovery from sleep) control
1: less than 1 ms
0: less than 3ms
Bit 3 **BATEN**: Battery monitor enable
1: Battery monitor is enabled.
0: Battery monitor is disabled.

LREG0x208 RFCTL8

LREG0x208, RFCTL8							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved			RFVCO	reserved			
			R/W-0				

Bit 4 **RFVCO**: VCO control. Recommend value is "1".

LREG0x209 SLPCAL1

LREG0x209, SLPCAL1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SLPCAL1							
R-0x0							

Bit 7-0 **SLPCAL1**: SLPCAL[7:0]. Calibration counter which calibrates sleep clock. SLPCAL[19:0] indicates

the timing of 16 sleep clock cycles. The unit is 50ns, counted by 20MHz.

LREG0x20A SLPCAL2

LREG0x20A, SLPCAL2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SLPCAL2							
R-0x0							

Bit 7-0 **SLPCAL2**: SLPCAL[15:8]. Calibration counter which calibrates sleep clock. SLPCAL[19:0] indicates the timing of 16 sleep clock cycles. The unit is 50ns, counted by 20MHz.

LREG0x20B SLPCAL3

LREG0x20B, SLPCAL3							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
CALRDY	reserved		CALEN	SLPCAL3			
R-0			WT-0	R-0b0000			

Bit 7 **CALRDY**: SLPCAL status indicator.
0: Not ready
1: Calibration counter finished the counting for 16 cycles of sleep clock. SLPCAL[19:0] is ready to be read.
Bit 4 **CALEN**: Set this bit to "1" to start calibration counter.
Bit 3-0 **SLPCAL3**: SLPCAL[19:16]. Calibration counter which calibrates sleep clock. SLPCAL[19:0] indicates the timing of 16 sleep clock cycles. The unit is 50ns, counted by 20MHz.

LREG0x211 CLKIRQCR

LREG0x211, CLKIRQCR							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
reserved						IRQPOL	CLK32KOFF
--						R/W-0	R/W-0

Bit 1 **IRQPOL**: Interrupt edge polarity bit
0: Falling edge
1: Rising edge
Bit 0 **CLK32KOFF**: SLPCLK disable bit
0: Enable
1: Disable

LREG0x220 SCLKDIV

LREG0x220, SCLKDIV							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0

I2CWDTEN	reserved	SCLKDIV
R/W-0		R/W-0b00000

Bit 7 **I2CWDTEN**: I^2C watchdog timer enable
1: enable
0: disable

Bit 4-0 **SCLKDIV**: sleep clock division selection.
n: the sleep clock is divided by 2^n before being fed to logic circuit.
Note: If internal ring oscillator is used, 0b0001 is the recommended value.

LREG0x222 WAKETIMEL

LREG0x222, WAKETIMEL							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
WAKETIMEL							
R/W-0xA							

Bit 7 **WAKETIMEL**: WAKETIME[7:0]. WAKETIME is a down counter which is counted by sleep clock. WAKETIME should be larger than WAKECNT (SREG0x35[6:0]). WAKETIME must be larger than one in any case.

LREG0x223 WAKETIMEH

LREG0x223, WAKETIMEH							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
					WAKETIMEH		
					R/W-0b000		

Bit 2-0 **WAKETIMEH**: WAKETIME[10:8]. WAKETIME is a down counter which is counted by sleep clock. WAKETIME should be larger than WAKECNT (SREG0x35[6:0]). WAKETIME must be larger than one in any case.

LREG0x224 TXREMCNTL

LREG0x224, TXREMCNTL							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXREMCNTL							
R/W-0x0							

Bit 7-0 **TXREMCNTL**: TXREMCNT[7:0]. Lower byte of remain counter.

LREG0x225 TXREMCNTH

LREG0x225, TXREMCNTH							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXREMCNTH							
R/W-0x0							

Bit 7-0 **TXREMCNTH**: TXREMCNT[15:8]. Higher byte of remain counter.

LREG0x226 TXMAINCNT0

LREG0x226, TXMAINCNT0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXMAINCNT0							
R/W-0x0							

Bit 7-0 **TXMAINCNT0**: TXMAINCNT[7:0]. Bit 7 to bit 0 of main counter.

LREG0x227 TXMAINCNT1

LREG0x227, TXMAINCNT1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXMAINCNT1							
R/W-0x0							

Bit 7-0 **TXMAINCNT1**: TXMAINCNT[15:8]. Bit 15 to bit 8 of main counter.

LREG0x228 TXMAINCNT2

LREG0x228, TXMAINCNT2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXMAINCNT2							
R/W-0x0							

Bit 7-0 **TXMAINCNT2**: TXMAINCNT[23:16]. Bit 23 to bit 16 of main counter.

LREG0x229 TXMAINCNT3

LREG0x229, TXMAINCNT3							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
STARTCNT	reserved				TXMAINCNT3		
WT-0					R/W-0b000		

Bit 7 **STARTCNT**: Trigger sleep mode in un-slotted mode (**BO** = 0xF and **SLOTTED** = 0b0). Will retrun to 0 when wake-up

Bit 2-0 **TXMAINCNT3**: TXMAINCNT[25:24]. Bit 25 and bit 24 of main counter.

LREG0x22F TESTMODE

LREG0x22F, TESTMODE							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
reserved			RSSIWAIT		TESTMODE		
			R/W-0b01		R/W-000		

Bit 4-3 **RSSIWAIT**: RSSI state machine parameter.
0b01 is the optimized value.

Bit 2-0 **TESTMODE**: UZ2400 test mode using GPIO
0b101: Single-tone test mode.
0b111: GPIO0, GPIO1, GPIO2 are configured to control external PA, LNA or switch as discussed above.

LREG0x230 ASSOEADR0

LREG0x230, ASSOEADR0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
ASSOEADR0							
R/W-0x0							

Bit 7-0 **ASSOEADR0**: ASSOEADR[7:0]. Bit 7 to bit 0 of 64-bit long address of associated Coordinator.

LREG0x231 ASSOEADR1

LREG0x231, ASSOEADR1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
ASSOEADR1							
R/W-0x0							

Bit 7-0 **ASSOEADR1**: ASSOEADR[15:8]. Bit 15 to bit 8 of 64-bit long address of associated Coordinator.

LREG0x232 ASSOEADR2

LREG0x232, ASSOEADR2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
ASSOEADR2							
R/W-0x0							

Bit 7-0 **ASSOEADR2**: ASSOEADR[23:16]. Bit 23 to bit 16 of 64-bit long address of associated Coordinator.

LREG0x233 ASSOEADR3

LREG0x233, ASSOEADR3							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0

ASSOEADR3
R/W-0x0

Bit 7-0 **ASSOEADR3**: ASSOEADR[31:24]. Bit 23 to bit 16 of 64-bit long address of associated Coordinator.

LREG0x234 ASSOEADR4

LREG0x234, ASSOEADR4							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
ASSOEADR4							
R/W-0x0							

Bit 7-0 **ASSOEADR4**: ASSOEADR[39:32]. Bit 31 to bit 24 of 64-bit long address of associated Coordinator.

LREG0x235 ASSOEADR5

LREG0x235, ASSOEADR5							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
ASSOEADR5							
R/W-0x0							

Bit 7-0 **ASSOEADR5**: ASSOEADR[47:40]. Bit 39 to bit 32 of 64-bit long address of associated Coordinator.

LREG0x236 ASSOEADR6

LREG0x236, ASSOEADR6							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
ASSOEADR6							
R/W-0x0							

Bit 7-0 **ASSOEADR6**: ASSOEADR[55:48]. Bit 47 to bit 40 of 64-bit long address of associated Coordinator.

LREG0x237 ASSOEADR7

LREG0x237, ASSOEADR7							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
ASSOEADR7							
R/W-0x0							

Bit 7-0 **ASSOEADR7**: ASSOEADR[63:56]. Bit 55 to bit 48 of 64-bit long address of associated Coordinator.

LREG0x238 ASSOSADR0

LREG0x238, ASSOSADR0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
ASSOSADR0							
R/W-0x0							

Bit 7-0 **ASSOSADR0**: ASSOSADR[7:0]. Bit 7 to bit 0 of 16-bit short address of associated Coordinator.

LREG0x239 ASSOSADR1

LREG0x239, ASSOSADR1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
ASSOSADR1							
R/W-0x0							

Bit 7-0 **ASSOSADR1**: ASSOSADR[15:8]. Bit 15 to bit 8 of 16-bit short address of associated Coordinator.

LREG0x240 ~ LREG0x24C UPNONCE

LREG0x240 ~ LREG 0x24C, UPNONCE							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
UPNONCE							
R/W-0x0							

Bit 7-0 **UPNONCE**: **UPNONCE** is 13-byte data. The lease significant byte is stored in LREG0x240 while the most significant byte is stored in LREG0x24C.

Revision History

Revision	Date	Description of Change
1.0	2007/6/6	1. Document format restructure. 2. Debugging related registers /bits were changed into reserved. (updated on 2008/3/7)
1.1	2008/6/19	1. Revise 4.6.1 setting of SLPACK (SREG0x35). 2. Correct description of bit 5 of SCLKDIV (LREG0x220). 3. Add setting of LREG0x201 (RFCTL1) to 0x01 in 4.2.4 initialization. 4. Delete redundant RESET step (step 3) in 4.2.4 initialization sequence. 5. Revise description in section 4.6.3 External Wake-up mode and delete "Waken by Power Management Reset". 6. Revise wait time requirement after initialization in 4.2.4 initialization. 7. Update the value of the RF sensitively components in 4.1.1 and 4.1.2. 8. Correct the Long Register Name of BBREG4(0x3c) in Table 12 Short address register list. 9. Add Crystal Specific Parameters in 3.6.1 Crystal oscillators. 10. Correct GATECLK Bit 3 (SREG0x26) in Appendix C. Register Descriptions. 11. Add setting of SREG 0x2A (SOFTRST) to 0x02 in 4.2.7 turbo mode and revise 4.2.7 setting value of BBREG3 (SREG 0x3B). 12. Correct BBREG3 bit 7-4 (SREG 0x3B) in Appendix C. Register Descriptions. 13. Correct 5.2.2 note description of Pb-free SMD package IR reflow profile. 14. Delete 4.6.3 Waken by power management reset.
1.2	2008/7/17	1. Correct description in 3.6.2 PLL Frequency Synthesizer 2. Correct description in section 3.6.3 Internal 100kHz Sleep Clock Oscillator for Sleep Clock
1.3	2008/08/28	1. Correct the Pin assignment of Pin27 and Pin28. 2. Add description of SREG0x39 (BBREG1) 3. Delete Clock out information 4. Add FIFO Mapping 5. Revise SPI frame format 6. Modify LREG 0X206 RFCTL6.

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