Compact Series CPLD Device Data Sheet

(DS03001， V1.5)

(2021.12.30)

revision history

date	revision	description
2018.8.24	V.01	initial release
2019.6.14	V1.0	1. Added D -type device description and device package information, added SSBG256 and MBG324 packages 2. Modify Compact Series CPLD Device Resources Logic resources for PGC4K devices and embedded Flash for all devices capacity 3. Modify the number of global dedicated clock pins to a maximum of 8 4. Note that the supported hot- plug level is level 2 5. Add output delay function , modify the maximum delay supported to 3100ps 6. The output accuracy of the modified on-chip oscillator is ±5.5% 7. Updated dual-boot description, D -type devices especially support embedded Flash self-loading dual- boot function 8. Updated DC and AC characteristics 9. 2.5ms power-on reset time for updated devices 10. Embedded Flash self-loading changed its name to main self- loading
2019.8.22	V1.1	1. Delete RSDS level and SLVS level 2. Instructions for increasing the total capacity of embedded Flash 3. Update package information 4. IO of PGC1K device Bank statistics distinguish L -type devices from G -type devices 5. IO from a packaging perspective bank distribution and top view
2019.11.9	V1.2	1. Correct the number of FFs of the device and the distributed ram size of the PGC1K 2. delete table 25 Power-on reset time for configuration mode AC characteristics, increase device power-on initialization time 3. Corrected size of MBG324 package 4. fix IO The maximum delay value of Delay , increase the delay step parameter
2020.4.1	V1.3	1. Main features and Table 2-5 add support for RSDS -like differential standards 2. Modify the notes in Table 1-1 to improve the definition of the embedded Flash space available to users and the maximum capacity of embedded Flash 3. Modify the statistical unit of distributed ram capacity in Table 1-1 to Kbits 4. Corrected Table 1-1 Maximum capacity of embedded flash of PGC7K 5. Modify the description of global clock in chapter 2.3 6. Added the description of OSC output frequency discontinuity in chapter 2.5 7. Improve the description of embedded flash power supply in chapter 2.7 8. Improve the status of IO in chapter 2.8 9. Modify the operation mode of UID in chapter 2.10 , only support read operation, not write operation 10. Added remarks for LVDS input and output in Table 2-5 , and modified the VCCIO of MIPI input 11. Add Table 2-6 Step delay of the I/O delay unit 12. Add Table 2-7 OSC output frequency 13. Updated Table 3-1 Minimum working voltage limit 14. Corrected VPDNEXT in Table 3-6 15. Correction to Table 3-8 DC Characteristics of LVTTL33 16. Add Table 3-9 VID index of LVDS DC characteristics 17. Added Figure 3-2 , Figure 3-3 , Figure 3-4 Voltage waveforms for differential level standards 18. Increase the programming and erasing current of the embedded Flash programming and erasing current PGC1KG 19. Increase the global clock dynamic switching hold time in Table 4-2 20. Modify Table 4-7 IO The MIPI interface performance of Buffer performance is 900Mbps 21. Add Table 4-7 A note on MIPI performance 22. Added table 4-8 LVDS1:2 performance

		23. Removed Table 4-2 , Table 4-8 Device Speed Grade - 7 24. add disclaimer 25. Removed speed grade for Compact family CPLD device naming - 7 26. Modify Table 1-3 and add 2 user guides 27. Delete the operating procedures and precautions, transportation and storage, unpacking and inspection, quality assurance and after-sales service, etc. 28. Table 4-3 The PLL AC characteristic increases the pulse width of the reset signal RST
2020.8.6	V1.4	1. Added PGC10KD device information, Table 1-1 Added PGC10K resource information for Compact series CPLD device resources , Table 1-2 CPLD package and I/O number increase PGC10KD-MBG484 package information 2. Table 1-1 adds remarks to describe the maximum capacity of embedded Flash available to users of PGC1KG and PGC1KL respectively 3. Table 1-1 describes the information for increasing storage capacity when DRM resources are used 4. Delete Table 1-1 I/O of Compact Series CPLD Device Resources Bank information, please refer to the package manual of each device 5. Update Table 1-2 CPLD package and I/O number , delete PGC4KD-MBG400 , add device description that supports slave and configuration mode 6. Added Figure 2-1 PGC1KL Top view of bank distribution , table 2-4 adds PGC10K and remarks 7. in 2.4.1 IO Perfect I/O in Buffer (IOB) Description of BANK power supply 8. Add Table 2-8 OSC Accuracy List for CPLD Devices 9. Removed APB bus performance for 2.6 Embedded Hardcore , see also " Compact Series CPLD Embedded Hardcore User Guide " 10. Complete Table 3-3 Note 2 for Recommended Device Operating Conditions 11. Change Table 3-7 Hot Swap Electrical Parameters I_{DK} Maximum and Minimum Units 29. Update Table 4-3 Parameter of $f_{PFD\ of}$ PLL AC characteristics , the range is 20MHz to 40MHz when divided by fraction
2021.12.30	V1.5	1. Updated configuration and testing , and added support for prohibiting CRAM readback to protect user information security 2. Modify the external power supply voltage VCC , input I/O voltage , tri- state voltage , the voltage boundary value of the Bank voltage VCCIO ; delete the note 3 of the CPLD 's allowable limit operating conditions "the allowable withstand time of undershoot to -2V is less than 20ns , and the allowable withstand time of overshoot to (V_{IHMAX} +2)V is less than 20ns" 3. Added Figure 3-1 Schematic diagram of the overshoot and undershoot of the input signal and Table 3-2 Allowable overshoot requirements under 10 -year service life conditions 4. Single- ended I/O DC characteristics increase the IOL/IOH value of LVCMOS25 5. BLVDS DC Characteristics Increase V_{ID} Minimum 6. LVPECL33 DC Characteristics Increase V_{ID} Minimum 7. Quiescent current increases PGC10KD data 8. Remove embedded Flash programming and erasing currents 9. The main self- loading time increases the PGC10KD data 10. Add Table 4-1 AC characteristic parameters of DRM , Table 4-2 Clock AC Characteristics , Table 4-7 IO Buffer performance , Table 4- 8 " -5 " data for high speed data transfer performance list 12. Table 4-4 Configuration Mode AC Characteristics Refresh Device Power-Up Initialization Time

This document mainly describes the product model and resource scale list, function description, and DC and AC characteristics of the Compact series CPLD devices of Shenzhen Ziguang Tongchuang Electronics Co., Ltd. (hereinafter referred to as Ziguang Tongchuang). A comprehensive understanding is convenient for users to select devices.

1. General introduction of Compact series CPLD

Compact series devices are low-cost, high-density IO and non-volatile CPLD products manufactured by 55nm process, using advanced packaging technology to provide instant start-up function when power-on; LUT4 capacity covers 1300~ 9900; including special Memory module (DRM), a variety of on-chip clock resources, multi-functional I/O resources, rich wiring resources, integrated SPI, I2C and timer counters and other hard cores. The Compact series CPLD also supports multiple configuration modes, supports remote upgrade and dual-boot functions, and provides functions such as UID Unique Identification) to protect the user's design security.

Compact series CPLD devices include G (general purpose), L (low power consumption) and D (support main self-loading dual-boot function) three versions, support two speed grades -5 and -6, of which -6 is the fastest grade. G-type and D-type devices support external power supply voltage V_{CC} of 2.5V or 3.3V, and the core voltage is generated by the internal LDO circuit, and the core voltage VCC $_{CORE}$ is 1.2 V; L-type devices only support V_{CC} as 1.2V VCC_{CORE} is the same as V_{CC}. Each I/O Bank power supply of CPLD device is powered by its corresponding VCCIO independently, supporting 1.2V, 1.5V, 1.8V, 2.5V and 3.3V.

1.1 Main features

- **Flexible Architecture**
  - Logic Resources 1300-9900 equivalent LUT4
  - User I/O up to 384
- **Versatile I/O**
  - Supports different types of I/O interface

    —— LVCMOS33/LVCMOS25

    /LVCMOS18/LVCMOS15

    / LVCMOS12

    ----- LVTTL33

    ——PCI33

    ——LVDS /MLVDS/LVPECL33

    /BLVDS25/RSDS

    ------ MIPI
  - Support level 2 hot swap
  - Optional Internal Differential Input Termination Resistors 100Ω
  - Programmable slew rate
  - Programmable weak pull-up or weak pull-down
  - Contains input, output and tri-state registers
  - Supports IDDR (1:2) and ODDR (2:1)
  - Contains I/O delay unit
- **Dedicated storage module**
  - single DRM Provides 9Kbits storage
  - Supports a variety of working modes, including dual-port (DP) RAM , simple dual-port (SDP) RAM , single-port (SP) RAM or ROM mode, and FIFO mode
  - Dual port RAM and simple dual port RAM Support dual- port mixed data bit width
  - Support byte enable function
- **Support high-speed data transmission**
  - OSERDES Support 4:1 , 7:1 , 8:1
  - ISERDES Support 1:4 , 1:7 , 1:8
- **Clock resource**
  - 8 global clock lines and 8 global signal lines supporting up to 400MHz
  - 4 I/O Clock network , supports up to 600MHz
  - Supports up to 2 PLLs
- **Various configuration methods and applications**
  - JTAG support configure
  - Support main self-loading
  - Main SPI support configure
  - Slave SPI configure
  - Support from I2C – configure
  - Support from and configure
  - Support dual-boot function
  - Support remote upgrade
  - Support for compressed bitstreams
- **Embedded hard core**
  - 2 I^2C hardcore
  - 1 SPI hardcore
  - 1 timer / counter
  - 1 on-chip oscillator
- **Application field**
  - Consumer electronics products
  - Computing and Storage
  - wireless communication
  - Industrial Control System
  - autonomous driving system

1.2 Device Resources and Packaging Information

Compact Series CPLDs Devices have different resource sizes. The resource list of different types of CPLDs is shown in Table 1-1:

Table 1-1 Compact Series CPLDs Device Resources

Resource Name		PGC1K	PGC2K	PGC4K	PGC7K	PGC10K
CLM	LUT5	1064	2024	3968	5920	8256
	Equivalent LUT4	1276	2428	4761	7104	9907
	FF	1596	3036	5952	8880	12384
	distributed ram (Kbits)	11	16	39	56	78
DRM	9K [1]	7	8	11	26	45
	Maximum Capacity (Kbits)	63	72	99	234	405
PLL		1	1	2	2	2
User-available embedded Flash maximum capacity (Kbits) [2]		80 [3]	80	1520	2070	3016
Embedded Flash Maximum Capacity (Kbits) [4]		664	664	2560	3616	5120
Hardcore	I²C	2	2	2	2	2
	SPI	1	1	1	1	1
	Timer / Counter	1	1	1	1	1
On-chip oscillator		1	1	1	1	1
Whether to support MIPI D-PHY		Yes	Yes	Yes	Yes	Yes

Note: 1. Each DRM The capacity is 9 Kbits

2. User-available embedded Flash The maximum capacity refers to the size of the ordinary memory space remaining after a set of ordinary bit streams that do not contain initialization data
3. PGC1KL of user-available embedded Flash Maximum capacity is 310Kbits , PGC1KG of user-available embedded Flash Maximum capacity is 80Kbits
4. Embedded Flash The maximum capacity refers to the space size of ordinary memory, which can be used by users to store bit streams or other user data, etc.

CPLD The package information of the device is shown in Table 1-2 shown.

Table 1-2 CPLD Packaging and I/O quantity

Device / Package information	PGC1KL	PGC1KG	PGC2KL	PGC2KG	PGC4KL	PGC4KD	PGC7KD	PGC10KD
UWG36 (2.5mm*2.5mm， 0.4mm)	29/3 [1]							
UWG49 (3.2mm*3.2mm， 0.4mm)			39/5 [1]					
UWG81 (3.8mm*3.8mm， 0.4mm)					64/10 [1]			
LPG100 (14mm*14mm， 0.5mm)		80/4 [1]		80/4 [1]				
LPG144 (20mm*20mm， 0.5mm)		112/4 [1]		112/4 [1]		115/9 [1]	115/9 [1]	
SSBG256 (9mm*9mm， 0.5mm)			207/14 [1,2]		207/14 [1,2]			
MBG256 (14mm*14mm， 0.8mm)		207/14 [1,2]		207/14 [1,2]		207/18 [1,2]	207/19 [1]	
MBG324 (15mm*15mm， 0.8mm)						280/18 [1,2]		

MBG332 （17mm*17mm， 0.8mm）						275/18 [1,2]	279/21 [1]	
MBG400 （17mm*17mm， 0.8mm）							336/21 [1,2]	
MBG484 （19mm*19mm， 0.8mm）								384/24 [1,2]
FBG256 （17mm*17mm， 1.0mm）		207/14 [1,2]		207/14 [1,2]		207/18 [1,2]		
FBG484 （23mm*23mm， 1.0mm）							335/21 [1,2]	

Note: 1.X/Y Indicates X user I/Os , Y True differential output pin

2. These devices support slave and configure mode

1.3 Part Number Content and Meaning

Compact Series CPLDs part number content and meaning are shown in Figure 1-1 shown.

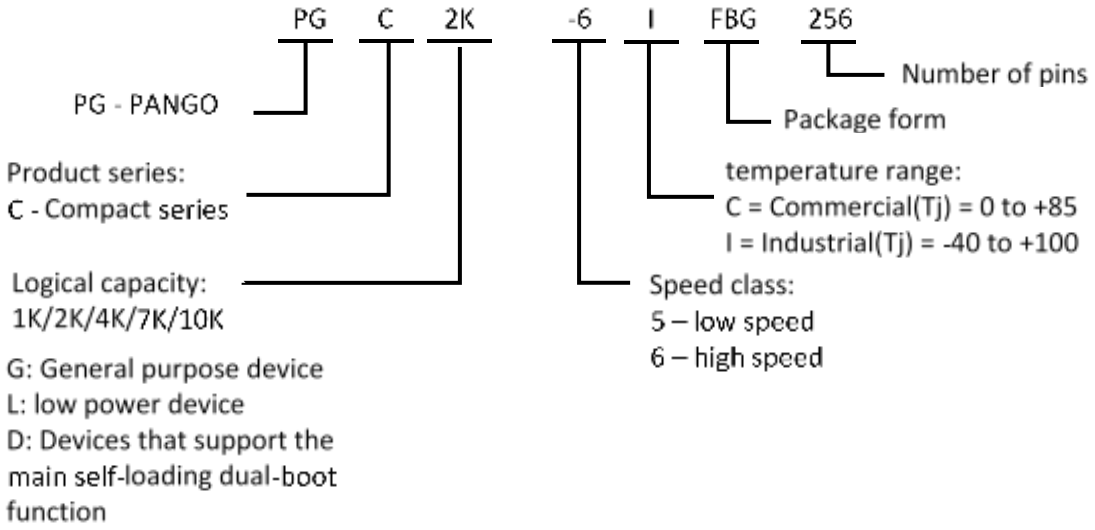

Figure 1- 1 Compact Series CPLDs Device naming

1.4 Reference documentation

Table 1-3 Compact Series CPLDs Document list

document number	File name
UG030001	" Compact Series CPLD Configurable Logic Module (CLM) User's Guide "
UG030002	" Compact Series CPLD Dedicated RAM Module (DRM) User's Guide "
UG030003	" Compact Series CPLD Clock Resources (Clock&PLL) User's Guide "
UG030004	" Compact Series CPLD Configuration (Configuration) User's Guide "
UG030005	" Compact Series CPLD Input and Output Interface (IO) User's Guide "
UG030006	" Compact Series CPLD Embedded Flash (EFlash) User's Guide "
UG030007	" Compact Series CPLD Embedded Hard Core User's Guide "
UG030008	" Compact Series GTP User Guide "
UG030009	" Compact Series Single Board Hardware Design User Guide"

2. Compact series CPLD function description

2.1 Configurable Logic Module（CLM）

CLM (Configurable Logic Module, Configurable Logic Module) is the basic logic unit of Compact series CPLD devices, each CLM contains 4 LUT5, 6 registers, bit extended function selector, fast carry logic and 4 independent cascades The cascade chain includes a fast carry chain (Carry Chain), a reset set control cascade chain (RS Chain), a clock enable control cascade chain (CE and a shift register data cascade chain (SR Chain).

2 LUT5 in each CLM can implement 1 LUT6, 2 LUT6 can implement 1 LUT 7. Two adjacent CLMs can implement 1 LUT8 logic.

There are two types of CLMs for CPLDs:

- CLMA , which implements logic, arithmetic, shift registers, and ROM Function
- CLMS , adding distributed RAM function based on the CLMA implementation function

CLM can be configured into different functional modes:

- Logical function mode
- Arithmetic function mode
- ROM memory mode
- Distributed RAM memory mode
- Multiplexer
- Output register

For details, please see " UG030001_Compact Series CPLDs Configurable Logic Module (CLM) User Guide.

2.2 Dedicated Memory Module（DRM）

The Compact family of CPLD devices contains up to 45 DRMs, each with a 9Kbits memory location, as well as input registers and output registers..

➢ Multiple working modes

DRM support a variety of working modes, including dual-port RAM , simple dual-port RAM , single-port RAM or ROM mode, and FIFO mode. Table 21 shows the configuration modes supported by the CPLD's DRM.

Table 2-1 DRM Configuration list

DRM mode	Single port RAM	Dual port RAM	Simple dual-port RAM	FIFO
storage mode	8K*1	8K*1	8K*1	8K*1
	4K*2	4K*2	4K*2	4K*2
	2K*4	2K*4	2K*4	2K*4
	1K*9(8)	1K*9(8)	1K*9(8)	1K*9(8)
	512*18(16)	N/A	512*18(16)	512*18(16)

➢ Support mixed data width

The DRM supports dual-port mixed data widths in dual-port RAM and simple dual-port RAM modes.

Table 2-2 Dual port RAM Mode Mixed Data Bit Width List

A port	B port				
	8K x 1	4K x 2	2Kx4	1Kx8	1Kx9
8Kx1	√	√	√	√	
4Kx2	√	√	√	√	
2Kx4	√	√	√	√	
1Kx8	√	√	√	√	
1Kx9					√

Table 2-3 Simple dual-port RAM Mode Mixed Data Bit Width List

Read port	Write port						
	8Kx1	4Kx2	2Kx4	1Kx8	512x16	1Kx9	512x18
8Kx1	√	√	√	√	√		
4Kx2	√	√	√	√	√		
2Kx4	√	√	√	√	√		
1Kx8	√	√	√	√	√		
512x16	√	√	√	√	√		
1Kx9						√	√
512x18						√	√

➢ Support byte enable

DRM Supports the byte enable function of the write operation, that is, the writing of the selected data byte is realized through the enable signal, and the writing of other bytes of the same address index is masked at the same time.

➢ Optional output register

For the data output port, DRM provides optional output registers for better timing performance.

➢ DRM cascading extension

Multiple DRMs can be combined into larger dual-port RAM, simple dual-port RAM, single-port RAM or ROM and FIFO by cascading expansion. For this, DRM provides an additional 3 bit s address extension

for deep extension applications.

For details, please see " UG030002_Compact Series CPLDs Dedicated RAM Module (DRM) User Guide.

2.3 Clock

Compact series CPLD devices have up to 8 pairs of dedicated clock differential input pins, which can accept differential or single-ended input signals. When a single-ended clock signal is connected, use the P side of the differential signal. As clock inputs, these pins are used to drive the clock line. When these pins do not need to drive the clock line, they can also be used as general purpose I/O.

- **Global clock network**

Global clock network supports 8 global clocks and 8 global signals 8 global signals can also be used as global clocks.

The global clock can clock various resources within the device, such as CLM DRM and IO Logic. The global clock supports a clock frequency of 400MHz. The global clock supports clock dynamic enable and dynamic switching functions.

Global signals are used as global control signals, such as clock enable signals, synchronous and asynchronous clear, reset or output enable signals.

- **I/O clock network**

There are 4 I/O clock networks, 2 each near BANK0 and BANK2. The clock signal can reach the IO Logic through the I/O clock as the high-speed sampling clock of the signal.

The I/O clock has the characteristics of high frequency (600MHz) and small frequency offset. The I/O clock supports the dynamic enable function.

- **PLL**

The Compact family CPLD devices have up to 2 PLLs. PLL is the core subsystem that CPLD provides clock resources.

The main functions are clock frequency synthesis, reducing clock skew, adjusting clock phase and low power management.

The input clock of the PLL supports input clock from external I/O and internal interconnect. Two input clocks are supported for dynamic switching. The PLL's feedback clock supports input from external I/O and internal interconnect.

PLL supports multiple clock outputs, each clock output has an independent frequency divider, supports 1-128 frequency division; each clock output can be cascaded, and PLLs can also be cascaded; each

clock output has optional dynamic Clock enable control; PLL also supports 16-bit precision fractional clock output, allowing users to generate non-integer output clocks. For details of the fractional frequency division calculation method and usage restrictions, please refer to "UG03000 3_ Compact Series CPLD Clock Resources Clock&PLL User Guide".

The PLL supports both static configuration and dynamic control of the clock phase. Among them, when dynamically adjusting the phase of the PLL, it can be rewritten with the APB interface, or controlled through the port. The PLL can dynamically and continuously realize the gradual increase or decrease of the phase, and during the phase adjustment process, the adjusted clock output has no glitches.

The PLL supports standby mode (standby mode, that is, when the PLL is not needed in the design, the PLL can be powered down to save power consumption.

The PLL supports the user to dynamically change the PLL operating parameters through the APB interface, providing another way for the user to dynamically configure the PLL. Details can be found in the UG030003 Compact Series CPLD Clock Resources Clock&PLL User Guide.

2.4 I/O unit

2.4.1 IO Buffer（IOB）

IO Buffer has different numbers of I/O Banks according to different device sizes (see Table 2-4 for details). The bank distribution of each device is as follows

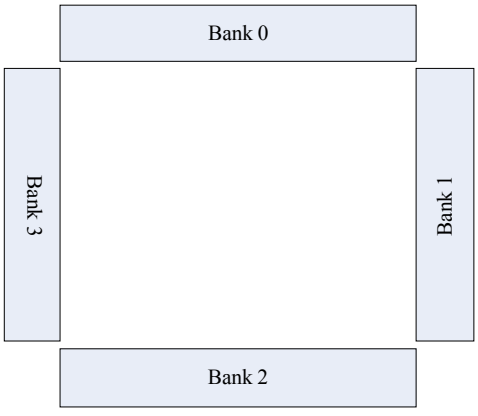

Figure 2-1 PGC1KL bank Distribution top view

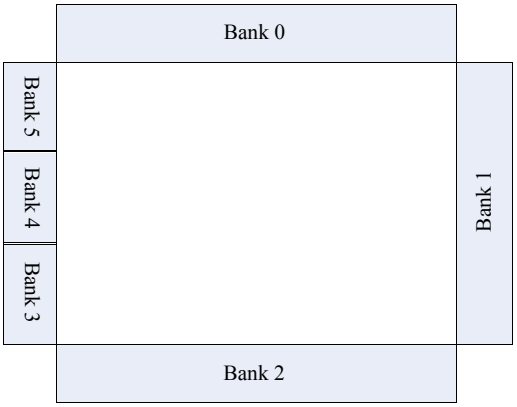

Figure 2-2 PGC1KG/2K/4K/7K/10K bank CPLD

Table 2-4 Bank resource distribution of Compact series CPLD devices

I/O Bank resource	PGC1KL[1]	PGC1KG	PGC2K[1]	PGC4K[1]	PGC7K	PGC10K
I/O Banks left	1	3	3	3	3	3
I/O Banks right	1	1	1	1	1	1
I/O Banks up	1	1	1	1	1	1
I/O Banks down	1	1	1	1	1	1
I/O Banks total	4	6	6	6	6	6

Note: 1. Devices in UWG package only lead out 3 banks of I/O, please refer to the package manual for details

Each bank independently supports 1.2V-3.3V bank voltage. When the IO in the whole bank is not in use, the bank power supply can be left floating or connected to the normal working voltage. It is recommended to connect to VCC. Each bank supports a variety of single-ended and differential interface standards to suit different application scenarios. IO Buffer is powerful and can flexibly configure I/O standards, output drive capability, slew rate, input hysteresis, and bus hold status. In addition, IO Buffer also supports hot-plug properties to prevent chip damage due to excessive leakage current;

Support internal differential input terminal matching resistance 100Ω, support LVDS and MIPI level standards.

All I/Os of the Compact series CPLD devices support differential inputs, but only the I/Os on the lower side of the device (Bank2) support internal differential input termination resistors. Some I/Os on the upper side (Bank0) support true differential output (pins defined as DIFFIO support true differential output, please refer to the PK series package manual for specific pin definitions. The I/O standards supported by CPLD are shown in Table 2-5.

Table 2-5 Compact Series CPLDs Supported I/O standard

I/O standard	I/O Typical Operating Voltage	Location	Remark
Input single-ended standard			
LVTTL33	3.3V	top bottom left right	
LVCMOS	3.3/2.5/1.8/1.5/1.2 V	top bottom left right	
PCI33	3.3V	Bottom	
Input differential standard			
LVDS	3.3/2.5 V	top bottom left right	Only the differential pairs below (BANK2) support internal termination resistors
BLVDS	3.3/2.5 V	top bottom left right	
MLVDS	3.3/2.5 V	top bottom left right	
RSDS	3.3/2.5 V	top bottom left right	
LVPECL33	3.3/2.5 V	top bottom left right	
MIPI (D- PHY)	1.2V	top bottom left right	Only the differential pairs below (BANK2) support internal termination resistors
Output single-ended standard			
LVTTL33	3.3V	top bottom left right	
LVCMOS	3.3/2.5/1.8/1.5/1.2 V	top bottom left right	
PCI33	3.3V	Bottom	
Output differential standard			
LVDS	3.3/2.5 V	top	True differential, only supported by pins with function name DIFFIO, see package manual for details
BLVDS	2.5V	top bottom left right	LVCMOS analog
MLVDS	2.5V	top bottom left right	LVCMOS analog
RSDS	2.5V	top bottom left right	LVCMOS analog
LVPECL33	3.3V	top bottom left right	LVCMOS analog
MIPI (D- PHY)	2.5V	top	
Bidirectional level standard			
LVTTL33	3.3V	top bottom left right	
LVCMOS	3.3/2.5/1.8/1.5/1.2 V	top bottom left right	

2.4.2 IO Logic（IOL）

IO Logic mainly include the following functions:

- Input, output, three-state combinational logic

- Input registers (flip-flops / latches), output registers (flip-flops) & tri-state registers (flip-flops)
- IDDR (1:2) and ODDR (2:1) , where ODDR includes output and tri-state ODDR

2.4.3 I/O input and output delay unit

The I/O input delay function and output delay function of CPLD are implemented separately by the same delay unit. All I/Os support static configuration of input and output delays, but only the I/Os on the lower side of the device support dynamically adjustable input delays, all I/Os do not support dynamically adjustable output delays.

Table 2 6 Step delay of I/O delay unit

Symbol	Description	minimum	Typical value	maximum value
$T_{IODELAY}$	per input / output delay step	55ps	79ps	125 ps

2.4.4 High-speed data transfer

The I/O unit can realize high-speed data transmission and reception by working with the I SERDES and OSERDES modules.

- ISERDES : For high-speed interface, support 1:4 , 1:7 , 1:8
- OSERDES : For high-speed interface, support 4:1 , 7:1 , 8:1

All banks support I DDR /ODDR and I/O tri-state registers. For high-speed interface applications, the Bank on the lower side supports ISERDES and the Bank on the upper side supports OSERDES.

2.4.5 Hot swap

The Compact family of CPLD devices supports Level 2 hot-swap capability. Each IO Buffer supports the hot-swap function to prevent the current from the signal pins flowing into the device substrate when the device supply voltage is lower than the external input signal voltage, resulting in latch up.

For details, please refer to "UG03000 5_ Compact Series CPLD Input and Output Interface (IO) User Guide".

2.5 On-chip oscillator

Each Compact family CPLD device has an on-chip oscillator (OSC). The output of the OSC can be programmed to be interconnected to the global clock network or to the PLL as a reference clock for the PLL. The output of the OSC can also provide a programmable configuration clock for the configuration system, Used as the main configuration clock. The output of OSC can also provide fixed frequency clock for embedded Flash.

Users can divide the clock frequency of OSC by instantiating GTP_OSC_E2. The eigenfrequency

of OSC is 266MHz, and the integer frequency division coefficient range is 2 128 OSC output frequency range is 2.08MHz 133MHz These frequency points are discontinuous, and the default value is 2.08MHz. When the clock output by the OSC is used as the user clock, the output frequencies are shown in Table 2-7.

Table 2-7 OSC Output frequency

OSC Output frequency (frequency division factor), in MHz							
2.08(128)	2.09(127)	2.11(126)	2.13(125)	2.15(124)	2.16(123)	2.18(122)	2.20(121)
2.22(120)	2.24(119)	2.25(118)	2.27(117)	2.29(116)	2.31(115)	2.33(114)	2.35(113)
2.38(112)	2.40(111)	2.42(110)	2.44(109)	2.46(108)	2.49(107)	2.51(106)	2.53(105)
2.56(104)	2.58(103)	2.61(102)	2.63(101)	2.66(100)	2.69(99)	2.71(98)	2.74(97)
2.77(96)	2.80(95)	2.83(94)	2.86(93)	2.89(92)	2.92(91)	2.96(90)	2.99(89)
3.02(88)	3.06(87)	3.09(86)	3.13(85)	3.17(84)	3.20(83)	3.24(82)	3.28(81)
3.33(80)	3.37(79)	3.41(78)	3.45(77)	3.50(76)	3.55(75)	3.59(74)	3.64(73)
3.69(72)	3.75(71)	3.80(70)	3.86(69)	3.91(68)	3.97(67)	4.03(66)	4.09(65)
4.16(64)	4.22(63)	4.29(62)	4.36(61)	4.43(60)	4.51(59)	4.59(58)	4.67(57)
4.75(56)	4.84(55)	4.93(54)	5.02(53)	5.12(52)	5.22(51)	5.32(50)	5.43(49)
5.54(48)	5.66(47)	5.78(46)	5.91(45)	6.05(44)	6.19(43)	6.33(42)	6.49(41)
6.65(40)	6.82(39)	7.00(38)	7.19(37)	7.39(36)	7.60(35)	7.82(34)	8.06(33)
8.31(32)	8.58(31)	8.87(30)	9.17(29)	9.50(28)	9.85(27)	10.23(26)	10.64(25)
11.08(24)	11.57(23)	12.09(22)	12.67(21)	13.30(20)	14.00(19)	14.78(18)	15.65(17)
16.63(16)	17.73(15)	19.00(14)	20.46(13)	22.17(12)	24.18(11)	26.60(10)	29.56(9)
33.25(8)	38.00(7)	44.33(6)	53.20(5)	66.50(4)	88.67(3)	133.00(2)	

The OSC accuracy of each device of the Compact series CPLD is shown in Table 2-8.

Table 2-8 CPLD Device OSC Precision list

device / temperature class	PGC1KL	PGC1KG	PGC2KL	PGC2KG	PGC4KL	PGC4KD	PGC7KD	PGC10KD
Commercial Grade (C)	**± 5.5%**	± 10%	**± 5.5%**	± 10%	**± 5.5%**	± 10%	± 10%	± 10%
Industrial grade (I)	± 10%	± 10%	± 10%	± 10%	± 10%	± 10%	± 10%	± 10%

Details can be found in " UG030003_Compact Series CPLDs Clock Resources (Clock&PLL) User Guide.

2.6 Embedded hard core

The Compact family of CPLD devices embeds several hard cores such as I²C, SPI and timer counters. Users can access these hard cores through the APB interface.

2.6.1 I²C hard core

Each CPLD device contains 2 I²C hard cores, and each I²C hard core can be configured as a master and a slave. When the I²C hard core is configured as a master device, it can control other devices through the I²C bus

interface; when it is a slave device, it can provide expansion I/O for the I^2C master device.

The I^2C hard core mainly supports the following functions:

- Can be configured as master or slave, support master-slave operation
- 7-bit and 10-bit addressing
- Multiple Master Arbitration
- Supports fast mode standard mode I^2C bus protocol, data transfer speed up to 400 KHz
- 8-bit APB bus user interface
- Support soft reset
- Interrupt support
- Support all-call address

2.6.2 SPI hard core

Each CPLD devices all contain a hard SPI core, which can be configured as a master or a slave. When it is a master device, it can control other chips with SPI interface through the SPI bus; when it is a slave device, it can be used as an interface for an external SPI master device. The SPI hard core supports the following functions:

- Can be configured as master or slave, support master-slave operation
- Interrupt support
- Double-buffered data register
- Polarity and Phase Programmable Serial Clock
- Data transmission supports LSB or MSB first
- 8-bit APB bus user interface
- Control up to 8 slave devices

2.6.3 Timer / Counter hard core

Each CPLD device provides a general-purpose, bidirectional 16-bit timer counter hard core. It has independent output compare unit and supports pulse width modulation. The hard core supports the following functions:

- Support the following working modes
  - Watchdog
  - Auto-clear timer
  - Fast PWM
  - Phase and Frequency Corrected Pulse Width Modulation

- Programmable clock input
- Support interrupt request
- Auto reload
- Timestamp supported
- 8-bit APB bus user interface

For details, see " UG030007_Compact Series CPLDs Embedded Hardcore User Guide.

2.7 Embedded Flash

Compact series CPLD devices contain an embedded Flash, which can be used to store configuration information, or provide users with general-purpose Flash storage space. Embedded Flash has the following characteristics:

- Power supply voltage 1.2V, provided by VCC CORE
- Storage space up to 5120 Kbits
- At least 100,000 erase and write operations
- Self-Adding Addressing
- Supports JTAG, I 2 CC, SPI and APB interfaces

For details, see " UG030006_Compact Series CPLDs Embedded Flash (EFlash) User Guide.

2.8 Power-On Reset Circuit（POR）

Compact Series CPLD devices feature a power-on-reset circuit (POR) which monitors the device at power-up and during operation VCC CORE and VCCIO0 of the device. After power-up begins, when the POR circuit detects that VCC CORE and VCCIO0 reach VPUP as shown in Table 36), the device begins to initialize.

Multiplexed I/O can be configured as configuration I/O or user I/O by setting the characteristic control bits. All I/Os are low during power up; before and during configuration, user I/Os are weakly pulled down, configuration I/Os are weakly pulled up or their inherent state After configuration is complete and enters user mode, user I/Os are weakly pulled down /O is released to the user. See the status of all I/Os at different stages "UG03000 44_Compact Series CPLD Configuration (Configuration) User Guide".

After entering user mode, the POR circuit continues to monitor VCC CORE. Correct operation of

the chip is not guaranteed if VCC CORE falls to the voltage specified by VPDN; once this happens, the POR circuit resets the entire chip and monitors VCC CORE and VCCIO0 again.

2.9 Configure and test

➢ Configuration

Compact family of CPLD devices includes a variety of configuration interfaces, JTAG, SPI, and I^2C. Among them, JTAG supports IEEE1149.1 Boundary Scan Specification and IEEE 1532 In-System Configuration Specification. With the support of these configuration interfaces, Compact devices can be configured in various modes.

- Autonomous loading
- JTAG mode
- Master SPI mode
- Slave SPI mode
- Slave I2C mode
- Slave parallel mode (not supported by all devices, see Table 1-2 CPLD package and I/O number for supported devices)

Power on the device, after completion, start the initialization operation of the device, and then select the configuration mode; different configuration modes have different configuration interfaces, after the configuration mode is determined, the corresponding pins are set as configuration pins, and then the bit stream is loaded; complete; After the bit stream is loaded, the CRC check is performed; after the CRC check is successful, the user mode is entered.

All configuration pins are multiplexed,

When some configuration pins are not used for configuration functions after entering user mode, they can be used for general purpose I/O

CPLD The device supports compressed bitstreams.

CPLD devices support a readback function for reading configuration data from CRAM. In the process of reading back, it does not affect the normal work of the system. At the same time, it also supports the prohibition of CRAM readback to protect the security of user information.

CPLD devices support dual-boot functionality.

CPLD device supports remote upgrade function.

➢ Boundary Scan Test

The Compact family of CPLD devices integrates a boundary scan unit, which supports IEEE

- Programmable clock input
- Support interrupt request
- Auto reload
- Timestamp supported
- 8-bit APB bus user interface

For details, see " UG030007_Compact Series CPLDs Embedded Hardcore User Guide.

2.7 Embedded Flash

Compact series CPLD devices contain an embedded Flash, which can be used to store configuration information, or provide users with general-purpose Flash storage space. Embedded Flash has the following characteristics:

- Power supply voltage 1.2V, provided by VCC CORE
- Storage space up to 5120 Kbits
- At least 100,000 erase and write operations
- Self-Adding Addressing
- Supports JTAG, I 2 CC, SPI and APB interfaces

For details, see " UG030006_Compact Series CPLDs Embedded Flash (EFlash) User Guide.

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Compact Series CPLD devices feature a power-on-reset circuit (POR) which monitors the device at power-up and during operation VCC CORE and VCCIO0 of the device. After power-up begins, when the POR circuit detects that VCC CORE and VCCIO0 reach VPUP as shown in Table 36), the device begins to initialize.

Multiplexed I/O can be configured as configuration I/O or user I/O by setting the characteristic control bits. All I/Os are low during power up; before and during configuration, user I/Os are weakly pulled down, configuration I/Os are weakly pulled up or their inherent state After configuration is complete and enters user mode, user I/Os are weakly pulled down /O is released to the user. See the status of all I/Os at different stages "UG03000 44_Compact Series CPLD Configuration (Configuration) User Guide".

After entering user mode, the POR circuit continues to monitor VCC CORE. Correct operation of

of the input signal undershoot; Different levels of overshoot requirements under 10-year service life conditions are given in Table 3-2.

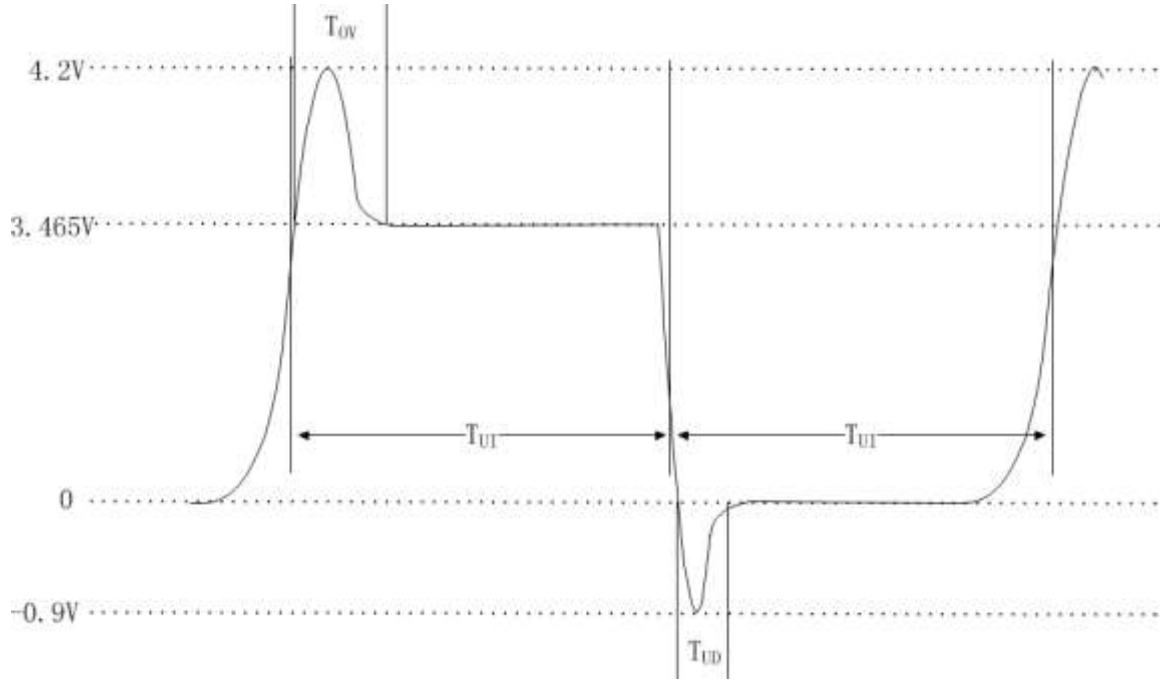

Figure 3-1 Schematic diagram of the overshoot and undershoot of the input signal

Table 3-2 10 Permissible overshoot requirement under annual service life conditions[1]

Input signal overshoot (V)	%UI (-40 ℃~100 ℃)	Input signal undershoot (V)	%UI (-40 ℃~100 ℃)
3.65	100	-0.35	100
3.7	82.6	-0.4	82.6
3.75	65.7	-0.45	65.7
3.8	52.3	-0.5	52.3
3.85	41.6	-0.55	41.6
3.9	30.9	-0.6	30.9
4.0	14.5	-0.7	14.5
4.1	6.9	-0.8	6.9
4.15	4.8	-0.85	4.8
4.2	3.35	-0.9	3.35

Note: 1.When UI< 100μs, the duration of overshoot of different degrees is the corresponding percentage multiplied by UI; when UI≥ 100μs, the duration of different degrees of overshoot is the corresponding percentage multiplied by 100μs

3.2 Recommended working conditions

Table 3-3 Recommended Device Operating Conditions

symbol	illustrate	minimum	Typical value	maximum	unit
V_{cc}[1]	L external supply voltage for type devices	1.14	1.2	1.26	V
	G Type /D external supply voltage for	2.375	2.5V/3.3	3.465	V

	type devices				
VCCIO [1,2]	I/O Bank Voltage	1.14	- -	3.465	V
T_J	Commercial grade operating junction temperature	0	- -	85	° C
	Industrial grade operating junction temperature	- 40	- -	100	° C

Note: 1. The same power supply should be connected together. For example, if VCCIO and V_{CC} are the same voltage value, they must come from the same source

2. When making the board, it is not used I/O Bank of VCCIO The pin can be left floating or powered, it is recommended to connect to V_{CC}; In order to ensure the normal operation of the chip , VCCIO0

Must be powered normally

3.3 ESD and Latch Up indicator

Table 3-4 ESD and Latch Up index

ESD（HBM）	ESD（CDM）	Latch- up
±2000 V	± 500 V	± 100 mA

3.4 Power ramp time

Table 3-5 Power ramp time

Symbol	Description	minimum	Typical value	maximum	unit
T_{VCCR}	V_{CC} rise time	0.20	- -	100.0	ms
T_{CCIOR}	I/O Bank Voltage Rise Time	0.20	- -	100.0	ms
V_{CC} and each bank VCCIO _ No power-up sequence requirement					

3.5 Power-on Reset Voltage Standard

Table 3-6 Power-on reset voltage standard[1,2]

Symbol	Description	Minimum	Typical value	Maximum value	unit
V_{PUP}	Power-on reset trigger level (monitoring VCC_{CORE} and VCCIO0)	0.9	- -	1.06	V
V_{PUPEXT}	Power-on reset trigger level (monitors V_{CC})	1.5	- -	2.1	V
V_{PDN}	Power-down reset trigger level (monitoring VCC_{CORE})	0.75	- -	0.93	V
V_{PDNEXT}	Power-down reset trigger level (monitors V_{CC})	1.6	- -	1.85	V

Note: 1.L version has no LDO inside the device, VCC_{CORE} and V_{CC} same; G/D version device VCC_{CORE} by V_{CC} by LDO produce V_{PUPEXT} and V_{PDNEXT} Only for G/D version device

3.6 Hot Swap Electrical Parameters

Table 3-7 Hot Swap Electrical Parameters

Symbol	Description	Condition	Minimum	Maximum value	unit
$IDK_{\_}$	Input or output leakage current during hot plugging	$0<V_{IN}<V_{IH}$ (Max)	- 1000	+1000	μA

3.7 Single-ended I/O DC Characteristics

Table 3-8 Single-ended I/O DC characteristics

Level standard	V_{IL} (V)		V_{IH} (V)		V_{OL} max (V)	V_{OH} Min (V)	IOL (mA)	I_{OH} (mA)
	min	max	min	max				
PCI33	- 0.3	0.3VCCIO	0.5VCCIO	3.465	0.1VCCIO	0.9VCCIO	1.5	- 0.5
LVCMOS33 LVCMOS33D LVTTL33	- 0.3	0.8	2.0	3.465	0.4	VCCIO- 0.4	4	- 4
							8	- 8
							12	- 12
							16	- 16
LVCMOS25 LVCMOS25D	- 0.3	0.7	1.7	3.465	0.4	VCCIO- 0.4	4	- 4
							8	- 8
							12	- 12
							16	- 16
LVCMOS18	- 0.3	0.35VCCIO	0.65VCCIO	3.465	0.4	VCCIO- 0.4	4	- 4
							8	- 8
							12	- 12
LVCMOS15	- 0.3	0.35VCCIO	0.65VCCIO	3.465	0.4	VCCIO- 0.4	4	- 4
							8	- 8
LVCMOS12	- 0.3	0.35VCCIO	0.65VCCIO	3.465	0.4	VCCIO- 0.4	2	- 2
							6	- 6

3.8 Differential I/O Electrical Characteristics

LVDS , BLVDS and LVPECL33 The main electrical parameters are defined as shown in Figure 3-2 shown.

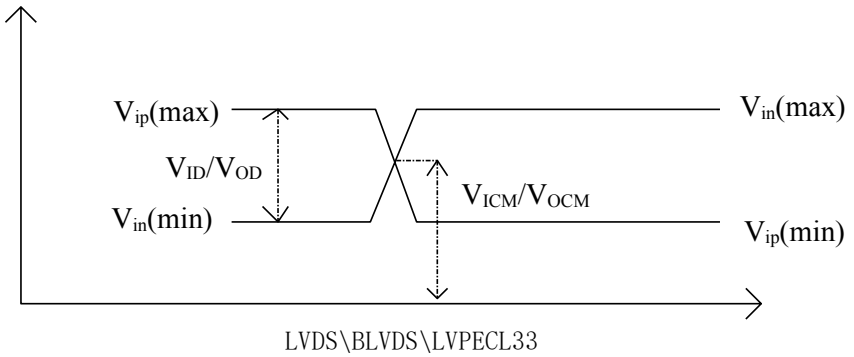

Figure 3-2 LVDS\BLVDS\LVPECL33 Voltage waveform

3.8.1 LVDS DC Characteristics

Table 3-9 LVDS DC characteristics

Symbol	Symbol description	Test Conditions	Minimum	Typical value	Maximum value	unit
V_{IP}, V_{IN}	Input voltage	VCCIO =3.3V	0	--	2.605	V
		VCCIO =2.5V	0	--	2.05	V
V_{ID}	Input differential mode voltage		0.1	--	--	V
V_{ICM}	Input common mode voltage	VCCIO=3.3V	0.4	--	2.4	V
		VCCIO=2.5V	0.4	--	1.9	V
V_{OD}	Output differential mode voltage	(Vop-Von), Rt=100 Ω	0.245	0.350	0.455	V
△ V_{OD}	$VOD_{Variation}$ Range		--	--	0.050	V
V_{OCM}	Output common mode voltage	(Vop+Von) /2 , Rt=100 Ω	1.0	1.2	1.4	V
△ V_{OCM}	V_{OCM} Variation Range		--	--	0.050	V

3.8.2 BLVDS DC Characteristics

Table 3-10 BLVDS DC characteristics

Symbol	Symbol description	Minimum	Typical value	Maximum value	unit
V_{ICM}	Input common mode voltage	0.4	--	1.9	V
V_{ID}	Input differential mode voltage	0.1	--	--	V
$V_{OD\_}$	Output differential mode voltage	0.230	--	0.460	V
V_{OCM}	Output common mode voltage	1.1	--	1.4	V
R_{left}	Left terminating resistor	40	--	100	Ω
R_{right}	Right terminating resistor	40	--	100	Ω
R_s	Driver series resistance	--	80	--	Ω

3.8.3 LVPECL33 DC Characteristics

Table 3-11 LVPECL33 DC characteristics

Symbol	Symbol description	Minimum	Typical value	Maximum	unit
V_{ICM}	Input common mode voltage	0.4	--	2.4	V
V_{ID}	Input differential mode voltage	0.1	--	--	V
$V_{OD\_}$	Output differential mode voltage	0.78	--	1.0	V
V_{OCM}	Output common mode voltage	1.3	--	2.1	V
R_S	Driver series resistance	--	100	--	Ω
R_P	Driver parallel resistance	--	200	--	Ω
RT_	Receiver Termination Resistor	--	100	--	Ω

3.8.4 MIPI DC Characteristics

Compact Series CPLDs Device supports MIPI D-PHY unidirectional HS (High Speed) and bidirectional LP (Low Power) input and output. The electrical parameters of the MIPI receiver are defined as shown in Figure 3-3 shown.

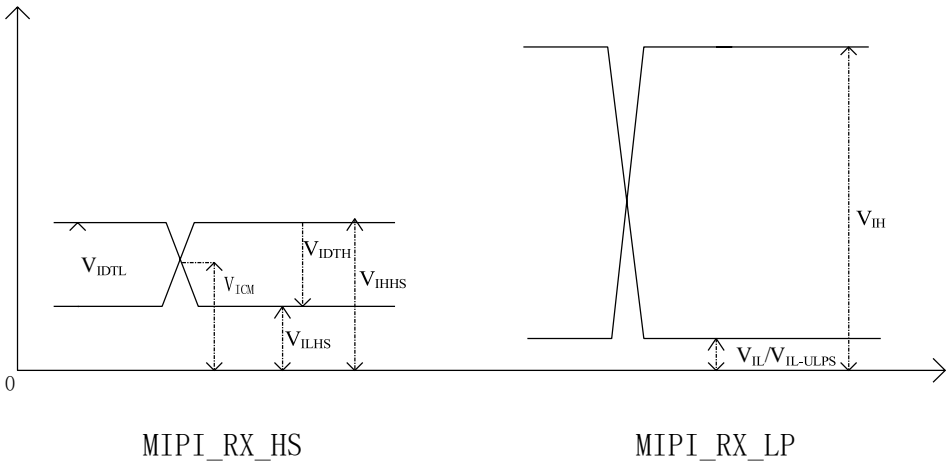

Figure 3-3 MIPI Receiver voltage waveform

Table 3-12 is MIPI DC characteristics of the receiver.

Table 3-12 MIPI Receiver DC Characteristics

Symbol	Symbol description	Minimum	Typical value	Maximum	unit
High Speed RX					
V_{ICM}	HS receive common mode voltage	70	--	330	mV
VCCIO	I/O Bank voltage	--	1.2	--	V
V_{IDTH}	Differential Input High Threshold	--	--	70	mV
V_{IDTL}	Differential Input Low Threshold	-70	--	--	mV
V_{IHHS}	Single-ended input high	--	--	460	mV

V_{ILHS}	Single-ended input low level	-40	--	--	mV
$V_{TERM-EN}$	Single-Ended Voltage Threshold for Termination Matching Enable	--	--	450	mV
Z_{ID}	Differential input impedance	80	100	125	Ω
Low Power RX					
V_{IH}	Input high level voltage value	880	--	--	mV
VCCIO	I/O Bank voltage	--	1.2	--	V
$V_{IL\_}$	Input low level voltage value	--	--	550	mV
VIL_{-ULPS}	Input low level voltage value (ultra low power mode)	--	--	300	mV
V_{HYST}	input hysteresis	25	--	--	mV

Table 3-13 is MIPI DC characteristics of the transmitter. MIPI The electrical parameters of the sender are defined as shown in Figure 3-4 shown .

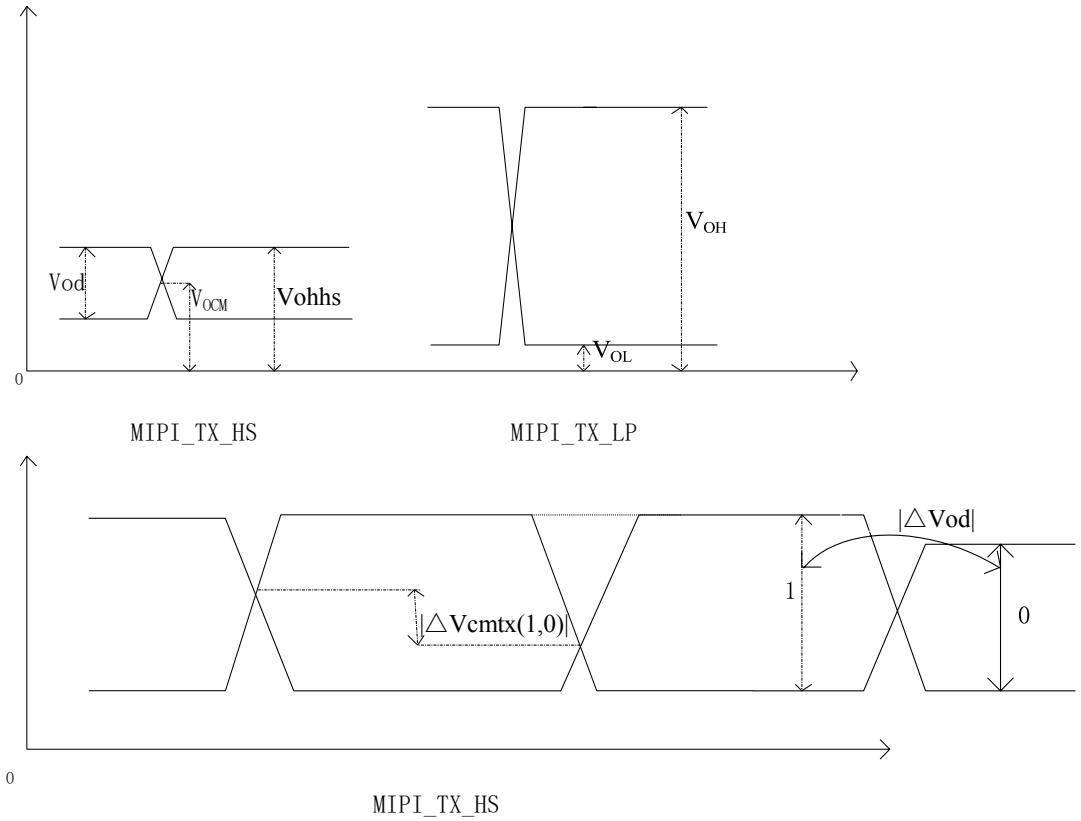

Figure 3-4 MIPI Transmitter Voltage Waveform

Table 3-13 MIPI Transmitter DC Characteristics

Symbol	Symbol description	Minimum	Typical	Maximum	Unit
High Speed TX					
V_{OCM}	HS output common mode voltage	150	200	250	mV
VCCIO	I/O Bank Voltage	--	2.5	--	V
|△Vcmtx(1,0)|	Difference in output common mode voltage for differential 1 and differential 0	--	--	5	mV
|Vod|	Output differential mode voltage	140	200	270	mV
|△Vod|	Difference in output differential mode voltage for differential 1 and differential 0	--	--	10	mV
Vohhs	HS output high level	--	--	360	mV
Z_{OS}	Single-ended output impedance	40	50	62.5	Ω
$\triangle Z_{OS}$	Differences in Single-Ended Output Impedance	--	--	10%	--
Low Power TX					
V_{OH}	Output high level	1.1	1.2	1.3	V
VCCIO	I/O Bank voltage	--	1.2	--	V
V_{OL}	Output low level	-50	--	50	mV
Z_{OLP}	LP mode output impedance	110	--	--	Ω

3.9 Input DC Characteristics

Table 3-14 Input DC Characteristics under Recommended Operating Conditions

Symbol	Symbol description	Condition	Minimum	Typical value	Maximum value	unit
I_{IL}	Leakage current when input is low	$0 \le V_{IN} \le (VCCIO - 0.2V)$	- 10	- -	10	μA
I_{IH}	Leakage current when input is high	$(VCCIO - 0.2V) < V_{IN} \le 3.6V$	- -	- -	175	μA
C_{IN}	pin input capacitance	25 ℃, signal frequency 1MHz	- -	- -	10	pF
$I_{PU\_}$	I/O pull-up current	$0 \le V_{IN} \le 0.7VCCIO$	- 30	- -	- 310	μA
$I_{PD\_}$	I/O pull-down current	$V_{IL}(Max) \le V_{IN} \le VCCIO$	30	- -	310	μA
I_{BKL}	The bus remains low with a holding current	$V_{IN} = V_{IL}(Max)$	30	- -	- -	μA
I_{BKH}	The bus remains high holding current	$V_{IN} = 0.7$ VCCIO	- 30	- -	- -	μA
I_{BKLOD}	Bus stays low with overdrive current	$0 \le V_{IN} \le VCCIO$	- -	- -	310	μA
I_{BKHOD}	Bus remains high overdrive current	$0 \le V_{IN} \le VCCIO$	- -	- -	- 310	μA
V_{BKV}	bus hold threshold		V_{IL} (Max)	- -	V_{IH} (Min)	- -

3.10 Quiescent Current

Under the condition that the ambient temperature is 25 ℃ and the device is not configured, the quiescent current is shown in Table 3-15 shown.

Table 3-15 Quiescent Current

Symbol	Symbol description	Device	Current value	unit
I_{VCC}	External power supply current	PGC1KL	3	mA
		PGC1KG	4.6	mA
		PGC2KL	4	mA
		PGC2KG	4.6	mA
		PGC4KL	4.6	mA
		PGC4KD	7.2	mA
		PGC7KD	9	mA
		PGC10KD	12	mA
$I_{CCIO\_}$	I/O Bank Current, I/O Bank Voltage is 2.5V	All devices	0	mA

4 AC characteristics

4.1 Switching Characteristics of DRM

Table 4-1 AC characteristic parameters of DRM

Symbol	Symbol description	Speed class		unit
		- 5	- 6	
$F_{MAX\_DRM\_}$	Single DRM, NW model	235	280	MHz
	Single DRM, TW model	235	280	MHz
	Single DRM, RBW model	168	200	MHz
	Single DRM, FIFO model	235	280	MHz

4.2 Clock AC Characteristics

Table 4-2 Clock AC Characteristics

Parameter Description	- 5			- 6			unit
	min	Typical value	max	min	Typical value	max	
Global clock frequency	--	--	340	--	--	400	MHz
Global clock pulse width	0.575	--	--	0.5	--	--	ns
Global clock skew	--	--	920	--	--	800	ps
Global clock duty cycle	45%	50%	55%	45%	50%	55%	--
Global clock dynamic switching hold time	$2(T_{CLKIN0}+T_{CLKIN1})$	--	--	$2(T_{CLKIN0}+T_{CLKIN1})$	--	--	--
I/O clock frequency	--	--	510	--	--	600	MHz
I/O clock skew	--	--	40.25	--	--	35	ps

I/O clock duty cycle	43%	50%	57%	43%	50%	57%	--

4.3 PLL AC Characteristics

Table 4-3 PLL AC characteristics

Symbol	Symbol description	Test Conditions	min	Typical value	max	unit
f_{IN}	input clock frequency		10	--	500	MHz
$f_{OUT\_}$	output clock frequency		3.125	--	600	MHz
$f_{OUT-CAS}$ [1]	Cascaded Output Clock Frequency（Class 1）		0.0244	--	600	MHz
f_{VCO}	VCO operating frequency range（G/D）		400	--	1200	MHz
	VCO operating frequency range（L）		400	--	800	MHz
$f_{PFD\_}$	PFD operating frequency range (integer division)		10	--	500	MHz
	PFD operating frequency range (fractional division)		20	--	40	MHz
$f_{DUTY\_}$	Output clock duty cycle		45%	50%	55%	--
$t_{IJITTER}$	Input Clock Cycle-to-Cycle Jitter	$f_{PFD\_} \geqslant$ 20MHz_	--	--	0.01	UIPP
		$f_{PFD\_}$ < 20 MHz	--	--	500	ps p-p
$t_{OJITTER}$	Output Clock Period Jitter (integer division)	$f_{OUT\_} \geqslant$ 100 MHz	--	--	155	ps p-p
		fOUT_ < 100 MHz	--	--	0.008	UIPP
	Output Clock Cycle-to-Cycle Jitter (integer division)	fOUT_ ⩾ 100 MHz	--	--	185	ps p-p
		fOUT_ < 100 MHz	--	--	0.010	UIPP
	Output Clock Period Jitter (fractional division)	fOUT_ ⩾ 100 MHz	--	--	235	ps p-p
		fOUT_ < 100 MHz	--	--	0.13	UIPP
	Output Clock Cycle-to-Cycle Jitter (fractional division)	fOUT_ ⩾ 100 MHz	--	--	235	ps p-p
		fOUT_ < 100 MHz	--	--	0.13	UIPP
	Output Clock Phase Jitter (integer division)	f_{PFD} ⩾ 100 MHz	--	--	165	ps p-p
		fPFD_ < 100 MHz	--	--	0.012	UIPP
$t_{PH\_}$	Phase shift accuracy		-6% Tvco	--	+6% Tvco	--
$t_{LOCK\_}$	PLL lock time		--	--	5	ms
t_{UNLOCK}	PLL loss of lock time		--	--	50	ns
t_{RST}	Reset signal RST pulse width		10	--	--	ns

Note: 1. For each additional stage of cascade, divide the output clock of the previous stage by 128

4.4 Configuration Mode AC Characteristics

Table 4-4 Configuration Mode AC Characteristics

Configuration mode	Description	min	Typical value	max	unit
JTAG	TCK frequency	--	--	50	MHz
	TCK low pulse width	10	--	--	ns
	TCK high pulse width	10	--	--	ns
	TMS/TDI setup time (rising edge of TCK)	3	--	--	ns
	TMS/TDI hold time (TCK rising edge)	2	--	--	ns
	TCK falling edge to TDO output valid	--	--	8	ns
main SPI	SCK initial frequency	--	--	2.08	MHz
	SCK frequency (high speed mode)	--	--	53.2	MHz
	SCK frequency (low speed mode, SPI Flash clock falling edge to data input out effective up to 5ns)	--	--	29.55	MHz
	SCK frequency (low speed mode, SPI Flash clock falling edge to data output effective maximum 6ns)	--	--	26.6	MHz
	SCK frequency (low speed mode, SPI Flash clock falling edge to data input out effective maximum of 7ns)	--	--	26.6	MHz
	SCK frequency (low speed mode, SPI Flash clock falling edge to data input out effective maximum of 8ns)	--	--	24.18	MHz
	SCK duty cycle	45%	50%	55%	--
	SCK frequency deviation	--	--	5%	--
	MISO setup time (SCK rising edge)	10	--	--	ns
	MISO hold time (SCK rising edge)	0	--	--	ns
	MISO setup time (falling edge of SCK)	9	--	--	ns
	MISO hold time (SCK falling edge)	0	--	--	ns
	SCK falling edge to MOSI output valid	--	--	4	ns
	SCK falling edge to CS_N output valid	--	--	4	ns
from SPI	SCK frequency	--	--	100	MHz
	SCK low pulse width	5	--	--	ns
	SCK high pulse width	5	--	--	ns
	MOSI setup time (SCK rising edge)	3	--	--	ns
	MOSI hold time (SCK rising edge)	2	--	--	ns
	SCK falling edge to MISO output valid	--	--	10	ns
Reset pulse width		384	--	--	ns
Delay from completion of device initialization to SCK output		400	--	--	ns
Device power-on initialization time (time from device reset release to initialization completion)	PGC1K	--	--	964	μs
	PGC2K	--	--	964	μs
	PGC4K	--	--	600	μs
	PGC7K	--	--	870	μs
	PGC10K	--	--	1500	μs

4.5 I²C Interface AC Characteristics

Table 4-5 I2C Interface AC Characteristics

Description [1]	standard mode		fast mode		unit
	minimum	maximum value	min	max	
SCL frequency	--	100	--	400	KHz
SCL low pulse width	4.7	--	1.3	--	μs
SCL high pulse width	4	--	0.6	--	μs

Note: 1. Other parameters refer to I²C Agreement shall prevail

4.6 Hard core SPI interface AC characteristics

Table 4-6 Hardcore SPI Interface AC Characteristics

Description	fast mode		unit
	min	max	
SCK frequency [1]	--	45	MHz

Note: 1.For the performance indicators of the configuration mode, see Table 4-4 Configuration Mode AC Characteristics

4.7 IO Buffer performance

Table 4-7 IO Buffer performance

Level standard	Max speed		unit
	-5	-6	
LVDS [1]	1080 (540 MHz)	1200 (600MHz)	Mbps
MIPI [2]	810 (405MHz)	900 (450MHz)	Mbps
BLVDS25	270 (135MHz)	300 (150MHz)	Mbps
MLVDS25	270 (135MHz)	300 (150MHz)	Mbps
LVPECL33	270 (135MHz)	300 (150MHz)	Mbps
LVTTL33	270 (135MHz)	300 (150MHz)	Mbps
LVCMOS33	270 (135MHz)	300 (150MHz)	Mbps
LVCMOS25	270 (135MHz)	300 (150MHz)	Mbps
LVCMOS18	270 (135MHz)	300 (150MHz)	Mbps
LVCMOS15	270 (135MHz)	300 (150MHz)	Mbps
LVCMOS12	180 (90 MHz)	200 (100MHz)	Mbps
PCI33	59	66	MHz

Note: 1.G/D type devices support such performance
2.L type devices support such performance

4.8 High-speed data transfer performance

Table 4-8 High-speed data transfer performance list

High-speed data transfer applications	Transmission rate		unit
	- 5	- 6	
LVDS 2： 1	360	400	Mbps
LVDS 4： 1	630	700	Mbps
LVDS 7： 1	693	770	Mbps
LVDS 8： 1	720	800	Mbps
MIPI D- PHY	810	900	Mbps

4.9 Master self-loading time

Table 4-9 Master self-loading time [1]

Device	Load time [1]	unit
PGC1K	1.3	ms
PGC2K	1.3	ms
PGC4K	2.4	ms
PGC7K	3.8	ms
PGC10K	5.8	ms

Note: 1. Master self-loading time refers to slave CPLD The time from the end of initialization to entering user mode