Logos Series FPGA Device Data Sheet

(DS02001, Version2.6)

(2021.07.12)

Revision history

Date	Revision	Description
2017.12.19	V1.0	initial release
2018.12.18	V1.1	1. The symbols of the unified core voltage and auxiliary power supply voltage are VCC and VCCAUX respectively 2. Modify Table 1 Logos series FPGA user guide document, delete package series document, add "Logos series product HMEMC application example user guide" 3. Modify the power-on sequence diagram in Chapter 3.2
2019.01.23	V1.2	1. Update Table 6 - the minimum value of each parameter of the absolute limit voltage of the device; 2. Update the fields and description of the table
2019.06.03	V1.3	1. Update product feature description; 2. FPGA resource quantity entry; 3. Update the encapsulation information and user IO quantity entries; 4. Delete HSST-related content; 5. Hot-swappable DC characteristics table items; 6. Update IO DC characteristics related items; 7. Update the items related to AC characteristics; 8. Update related table items of performance parameters under typical working conditions 9. Supplementary list of abbreviations
2019.09.25	V1.4	1. Symbol for unified power supply voltage; 2. Updated the fpga product features; 3. Updated resource scale, package information, and user IO quantity table items, and added PGL25G related information; 4. Updated the brief description of ddr, clock and configuration; 5. Added the working conditions of PGL25G device; 6. Added PGL25G input, output, and input and output IO level standard items; 7. Updated lvds performance characteristics and storage interface performance parameters
2019.12.16	V1.5	1. Modify Table 10, delete VCCEFUSE, VCCIOCFG two lines 2. Added the function that PGL12G does not support ROM in the DRM description
2020.01.03	V1.6	1. Modify Table 1 and Table 2
2020.03.03	V1.7	1. Modify Table 7 and add attention information 2. Modify Tables 18 and 19
2020.03.09	V1.8	1. Modify 1.3.2 DRAM description 2. Modify the description of 1.3.5 hard core and soft core 3. Modify the titles of chapters 3, 4, and 5 4. Amendments to Tables 22, 28, 30, 31, 32, 33, and 35 5. Modify Figure 2
2020.03.26	V1.9	1. Increase the input AC overshoot limit
2020.04.23	V2.0	1. Added note (2) to chapter 1.1

2020.08.13	V2.1	1. Added PGL50H data 2. MIPI performance indicators
2020.10.18	V2.2	1. Add PGL50G data
2020.12.10	V2.3	1. Modify Table 47, HSST_FREFCLK indicators
2020.03.01	V2.4	1. Add PGL100H data
2020.04.07	V2.5	1. Update table 51 data
2021.07.12	V2.6	1. Add caption table 8 2. Update the hot-swap feature 3. Modify Table 11 to increase the voltage range of VCCEFUSE 4. Modify Table 35 to increase the minimum value of the setup time and hold time of the falling edge of the slave string 5. Delete the HSST_VOUTCMAC indicator in Table 45 6. Modify Table 45, the maximum value of HSST_VRCLKPP is 1000mv

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List of acronyms

Acronym	Full Spelling
CLM	Configurable logic Module
DRM	Dedicated RAM Module
APM	Arithmetic Process Module
HMEMC	hard Memory Controller
DDRC	Double Data Rate Controller
DDR	Double Data Rate
ADC	Analog to Digital Converter
PLLs	Phase Locked Loop
ESD	Electro Static Discharge

This article mainly includes Shenzhen Ziguang Tongchuang Electronics Co., Ltd. (hereinafter referred to as Ziguang Tongchuang) Logos series FPGA The device feature summary description, product model and resource scale list, AC and DC characteristics, etc., users can use this article to understand the characteristics of Logos series FPGA devices, which is convenient for device selection.

1. LOGOS SERIES FPGA OVERVIEW

Logos series programmable logic device is a new low-power, low-cost FPGA product launched by Shenzhen Ziguang Tongchuang Electronics Co., Ltd. It adopts a completely independent property right architecture and mainstream 40nm process. Logos series FPGA includes innovative configurable logic module (CLM), dedicated 18Kb storage unit (DRM), arithmetic processing unit (APM), multi-functional high-performance IO and rich on-chip clock resources and other modules, and integrates a memory controller (HMEMC), analog-to-digital conversion module (ADC) and other hard core resources, support multiple configuration modes, and provide bit stream encryption, device ID (UID) and other functions to protect user design security. Based on the above characteristics, Logos series FPGA can be widely used in many application fields such as video, industrial control, automotive electronics and consumer electronics.

1.1 Logos series FPGA product features

- **Low cost, low power consumption**
  - Low power consumption, mature 40nm CMOS technology
  - As low as 1.1V core voltage
- **Support multiple standard IO**
  - Up to 308 user IO, support 1.2V, 1.5V, 1.8V, 2.5V, 3.3V IO standard
  - Support HSTL, SSTL storage interface standard
  - Support MIPI D-PHY interface standard
  - Support LVDS、 MINI-LVDS, SUB-LVDS, SLVS (MIPI Two-wire level standard), TMDS (applied to HDMI, DVI interface) and other differential standards
  - Programmable I/O BUFFER, high-performance IO LOGIC
- **Flexible Programmable Logic Module CLM**
  - LUT5 logical structure
  - Each CLM contains 4 multi-function LUT5, 6 registers
  - Supports fast arithmetic carry logic
  - Support distributed RAM model
  - Support for cascading chains
- **DRM that supports multiple read and write modes**
  - Single DRM Provides 18Kb Storage space, configurable as 2 independent 9Kb storage blocks
  - Support multiple working modes, including single-port (SP) RAM, dual-port (DP) RAM, simple dual- port (SDP) RAM, ROM and FIFO mode
  - Dual-port RAM and simple dual-port RAM Support dual port mixed data bit width
  - Support Normal-Write, Transparent-Write and Read-before-Write (1) write mode
  - Support Byte-Write Function

- **Efficient Arithmetic Processing Unit APM**
  - Each APM supports one 18*18 operation or two 9*9 operations
  - Support input and output registers
  - Support 48bit accumulator
  - Support "Signed" and "Unsigned" data operation
- **Integrated memory controller hard core HMEMC**
  - Support DDR2, DDR3, LPDDR
  - Single HMEMC Support x8, x16 data bit width
  - Support standard AXI4 bus protocol
  - Support DDR3 write leveling and DQS gate training
  - DDR3 Maximum rate up to 800Mbps
- **Integrated ADC hard core**
  - 10bit Resolution, 1MSPS (independent ADC operation) sampling rate
  - Up to 12 input channels
  - Integrated temperature sensor
- **Rich clock resources**
  - Support 3 types of clock network, flexible configuration
  - Region-based global clock network
  - Each area has 4 regional clocks, supporting vertical cascading
  - High-speed I/O Clock, support IO clock frequency division
  - Optional Data Address Latch, Output Register
  - Integrated multiple PLLs, each PLL supports up to 5 clock outputs
- **Flexible configuration**
  - Supports multiple programming modes
  - JTAG mode conforms to IEEE 1149 and IEEE
  - 1532 standard
  - Master SPI Optional up to 8bit Data bit width, effectively improve programming speed
  - Support BPI x8/x16, Serial slave, Parallel slave mode
  - Support AES-256bit stream encryption [(2)], support 64bit UID protection
  - Support SEUs Error detection and correction
  - Support multi-version bitstream fallback function
  - Support watchdog timeout detection
  - Support programming download
  - Support online debugging

Note (1): It is not supported to configure two ports as Read-before-Write at the same time

pattern

Note (2): PGL25G Does not support AES-256 bit stream encryption

1.2 Logos series FPGA resource size and package information

Table 1 and Table 2 show the resource scale and package information of Logos series FPGAs.

Table 1 Logos Number of FPGA resources

Device	CLM [1,2]				18Kb DRM	APM	PLLs	ADC	HME MC	MAX USER IO	HSST LANE	SD RAM
	LUT5	Eq LUT4	FF	Distributed RAM (bits)								
PGL12G	10400	12480	15600	84480	30	20	4	1	0	160	0	0
PGL22G	17536	21043	26304	71040	48	30	6	1	2	240	0	0
PGL22GS [3]	17536	21043	26304	71040	48	30	6	0	0	140	0	0
PGL25G	22560	27072	33840	242176	60	40	4	0	0	308	0	0
PGL50G	42800	51360	64200	544000	134	84	5	0	0	341	0	0
PGL50H	42800	51360	64200	544000	134	84	5	0	0	304	4	0
PGL100H	85392	102470	128088	1013504	286	188	8	0	0	498	8	0

Note 1: Each CLM contains 4 multi-function LUT5 and 6 registers; each multi-function LUT5 is equivalent to 1.2 LUT4

Note 2: The CLM in the chip includes CLMA and CLMS, and only CLMS can be configured as Distributed RAM.

Note 3: PGL22GS-176 contains a maximum of 140 IOs, including 68 pairs of differential pairs and 4 single-ended IOs; MAX USER IO 140 means off-chip.

Table 2 Logos FPGA package information and user IO quantity

Package	FBG256	FBG484	FBG900	MBG484	MBG324	LPG176	LPG144
Dimensions (mm)	17×17	23×23	31×31	19×19	15×15	22x22	22x22
Pitch (mm)	1.0	1.0	1.0	0.8	0.8	0.4	0.5
device	User IO	User IO	User IO	User IO	User IO	User IO	User IO
PGL12G	160	-	-	-	-	-	103
PGL22G	186	-	-	-	240	-	-
PGL22GS	-	-	-	-	-	140	-
PGL25G	186	308	-	-	226	-	-
PGL50G	-	332	-	341	218	-	-
PGL50H	-	296	-	304	190	-	-
PGL100H	-	-	498	-	-	-	-

1.3 Brief description of Logos series FPGA

1.3.1 CLM

CLM (Configurable Logic Module) is the basic logic unit of Logos series products. It is mainly composed of multi-function LUT5, registers and extended function selectors. CLM is distributed in columns in the Logos series products, and has two forms: CLMA and CLMS. Both CLMA and CLMS

support logic functions, arithmetic functions, and register functions, and only CLMS supports distributed RAM functions. Between CLM and CLM, and between CLM and other on-chip resources are connected through signal interconnection modules.

Each CLMA includes 4 LUT5s, 6 registers, multiple extended function selectors, and 4 independent cascade chains, etc.

CLMS is an extension of CLMA, which adds support for distributed RAM on the basis of supporting all functions of CLMA. CLMS can be configured as single-port RAM or simple dual-port RAM.

1.3.2 DRM

A single DRM has 18K bits storage unit, which can be independently configured with two 9K bits or one 18K bit It supports multiple working modes, including dual-port RAM, simple dual-port RAM, single-port RAM or ROM mode, and FIFO mode. DRM supports configurable data bit width, and supports dual-port mixed data bit width in DP RAM and SDP RAM modes. For PGL12G, ROM is not supported For detailed DRM usage, please refer to " Logos Series FPGA Dedicated RAM Module (DRM) User Guide".

1.3.3 APM

Each APM is composed of I/O Unit, Preadder, Mult and Postadder functional units, and supports each level of register pipeline. Each APM can realize one 18*18 multiplier or two 9*9 multipliers, and supports pre-add function; it can realize one 48bit accumulator or two 24bit accumulators. The APMs of Logos FPGAs support cascading for filter and high bit-width multiplier applications.

1.3.4 Input/Output

IOBs

The IO of Logos FPGA is distributed according to Bank, and each Bank is powered by an independent IO power supply. The IO is flexible and configurable, supporting 1.2V~3.3V power supply voltage and different single-ended and differential interface standards to suit different application scenarios. All user IOs are bidirectional, including IBUF, OBUF and tri-state control TBUF. The IOB function of Logos FPGA is powerful, and it can flexibly configure interface standards, output drivers, Slew Rate, input hysteresis, etc. For detailed IO characteristics and usage methods, please refer to "Logos Series FPGA Input and Output Interface (IO) User Guide".

IOL

The IOL module is located between the IOB and the core, and manages the signals to be input and output to the FPGA Core.

IOL supports various high-speed interfaces. In addition to supporting direct data input and output and IO register input and output modes, it also supports the following functions:

- ISERDES : For high-speed interfaces, it supports 1:2 ; 1:4 ; 1:7 ; 1:8 input serial-to-parallel converters.
- OSERDES : For high-speed interfaces, it supports 2:1 ; 4:1 ; 7:1 ; 8:1 output parallel-serial

converters.

- The built-in IO delay function can adjust the input / output delay dynamically or statically.
- The built-in input FIFO is mainly used to complete the clock domain conversion from the external discontinuous DQS (for DDR memory interface) to the internal continuous clock and the phase difference compensation between the sampling clock and the internal clock in some special Generic DDR applications.

1.3.5 Memory Controller System

PGL DDR Memory Controller System provides users with a complete DDR memory controller solution with flexible configuration.

PGL22G integrates HMEMC and has the following features:

- Support LPDDR, DDR2, DDR3
- Support x8, x16 Memory Device
- Support standard AXI4 bus protocol (burst type does not support fixed)
- A total of three AXI4 Host port, 1 128bit, 2 64bit
- Support AXI4 Read Reordering
- Support BANK Management
- Support Low power Mode, Self_refresh, Power down, Deep power down
- Support Bypass DDRC, support Bypass HMEMC
- Support DDR3 Write Leveling and DQS Gate Training
- DDR3 up to 800 Mbps

PGL12G, PGL25G, PGL50G, PGL50H, PGL100H can only use soft core to realize DDR Memory control has the following characteristics:

- Support DDR3
- Support x8, x16 Memory Device
- The maximum bit width supports 16 bit
- AXI4 bus protocol that supports tailoring
- AXI4 128bit Host port
- Support Self_refresh, Power down
- Support Bypass DDRC
- Support DDR3 Write Leveling and DQS Gate Training
- DDR3 up to 800 Mbps

1.3.6 ADC

The resolution of each ADC is 10bit, the sampling rate is 1MSPS, and there are 12 Channels, of which 10 Analog Inputs are multiplexed with GPIO, and the other 2 use dedicated analog input pins. The scanning mode of the 12 Channels is completely controlled flexibly by the FPGA, and the user can decide through User Logic that finally several Channels will share the ADC sampling rate of 1MSPS.

The ADC provides on-chip voltage and temperature monitoring. Can detect VCC, VCCAUX, VDDM (internal LDO output voltage); see Table 40 for detailed characteristic parameters.

1.3.7 Clock resource

Logos series products are divided into different number of regions, providing rich on-chip clock resources, including PLL and three types of clock networks: global clock, regional clock, I/O clock. Compared with other clocks, the IO clock has the characteristics of high frequency, small clock skew, and small delay time. See Table 3 for clock resources

Table 3 Clock Resources for Logos Series Products

PARAMETER	PGL12G	PGL22G	PGL25G	PGL50H PGL50G	PGL100H
Number of regions	4	6	4	6	10
Number of global clocks	20	20	20	30	30
Number of global clocks supported per region	16	12	16	16	16
Number of local clocks supported per region	4	4	4	4	4
Number of IO BANKs	4	6	4	4	6
Each IO BANK supports the number of IO clocks	2	2	4	BANK0/2 : 4 BANK1/3 : 6	BANK0/2 : 4 BANK1/3 : 10
Total IO clocks	8	12	16	20	28
Number of PLLs	4	6	4	5	8

Logos FPGA embeds multiple PLLs, each PLL has up to 5 clock outputs, supports frequency synthesis, phase adjustment, dynamic configuration, source synchronization, zero-delay buffering and other modes, in addition, PLL supports Power Down, if in a certain period If the PLL is not used for a certain period of time, the user can turn off the PLL to reduce power consumption.

In order to improve clock performance, Logos FPGA also provides CLK- related special IOs, including four types: clock input pins, PLL reference clock input pins, PLL feedback input clock pins, and PLL clock output pins. Compared with ordinary IOs, using these clock input / output pins can avoid the interference caused by ordinary routing resources, thereby obtaining better clock performance. When not used as clock input / output, these clock pins can be used as ordinary IO For details about the specific use of the clock, see " Logos Series FPGA Clock Resource (Clock) User Guide".

1.3.8 Configuration

Configuration is the process of programming the FPGA. Logos FPGA uses SRAM unit to store

configuration data, which needs to be reconfigured every time it is powered on; configuration data can be actively obtained by the chip from an external flash, or downloaded to the chip through an external processor or controller.

Logos FPGA supports multiple configuration modes, including JTAG mode, SPI Master mode, SPI Slave mode, Parallel Slave mode, Serial Slave mode and Master BPI mode. The configuration modes supported by each device are listed in Table 4 below.

Table 4 Configuration mode

Model	Data width	PGL12G		PGL22G		PGL22GS	PGL25G	PGL50H PGL50G	PGL 100H
		LPG144	FBG 256	FBG 256	MBG 324	LPG176	FBG256 MBG324 FBG484	FBG484 MBG484 MBG324	FBG900
JTAG	1	support	support	support	support	support	support	support	support
SPI Master	1	not support	support	support	support	support	support	support	support
	2	not support	support	support	support	support	support	support	support
	4	not support	support	support	support	support	support	support	support
	8	not support	support	support	support	support	not support	not support	not support
SPI Slave	1	support	support	support	support	not support	not support	not support	not support
Parallel Slave	8	support	support	support	support	not support	support	support	support
	16	support	support	support	support	not support	support	support	support
	32	support	support	not support	support	not support	not support	not support	not support
Serial Slave	1	support	support	support	support	not support	support	support	support
BPI Master	8 (async)	not support	not support	not support	support	not support	support	support	support
	16 (async)	not support	not support	not support	support	not support	support	support	support
	16 (sync)	not support	not support	not support	support	not support	not support	not support	not support

The configuration related functions of Logos FPGA are as follows:

- Support configuration data stream compression, which can effectively reduce bit stream size, saving storage space and programming time
- Support via JTAG interface, SEU from parallel interface 1 bit Error correction and 2bit error detection
- Support watchdog timeout detection function
- In main BPI/ master SPI In mode, support configuration bit stream version rollback function

To protect user designs, Logos FPGAs also provide UID functionality. Each FPGA device has a corresponding unique number, which has been uniquely determined when the device leaves the factory. Users can read through the UID interface and JTAG interface, and after processing with their own unique encryption algorithm, the result will be incorporated into the programming data stream. After reloading the data flow every time, the FPGA enters the user mode, and the user logic will first read the UID and process it with the user's unique encryption algorithm, and then compare it with the result in the previous programming data flow. If there is a difference, the FPGA cannot work normally.

Logos Series FPGA Reference Materials

Section 1.3 briefly describes each module of Logos FPGA, as well as the clock and configuration system. For detailed information about the corresponding modules, please refer to the user guide documents related to Logos FPGA, as shown in Table 5 below.

Table 5 Logos Series FPGA User Guide Documentation

Document number	File name	Document content
UG020001	"Logos Series FPGA Configurable Logic Module (CLM) User Guide"	Logos series FPGA configurable logic module function description
UG020002	"Logos Series FPGA Dedicated RAM Module (DRM) User Guide"	Logos series FPGA dedicated RAM module
UG020003	"Logos Series FPGA Arithmetic Processing Module (APM) User Guide"	Logos series FPGA arithmetic processing module function description
UG020004	"Logos Series FPGA Clock Resource (Clock) User Guide"	Logos series FPGA clock resources, including PLL function and usage description
UG020005	"Logos Series FPGA Configuration (configuration) User Guide"	Logos series FPGA configuration interface, configuration mode, configuration process, etc.
UG020006	"Logos Series FPGA Input and Output Interface (IO) User Guide"	Logos series FPGA input and output interface function description
UG020009	"Logos Series FPGA Analog-to-Digital Conversion Module (ADC) User Guide"	Logos series FPGA analog-to-digital converter function description
UG020011	"Logos Series Products HMEMC Application Example User Guide"	Logos series FPGA storage control system
UG020013	“Logos Family FPGA High- Speed Serial Transceiver (HSST) User Guide	Logos Series FPGA High Speed Serial Transceiver Application Description

1.4 Logos Series FPGA Ordering Information

Figure 1 shows the numbering content and meaning of Logos series FPGA product models.

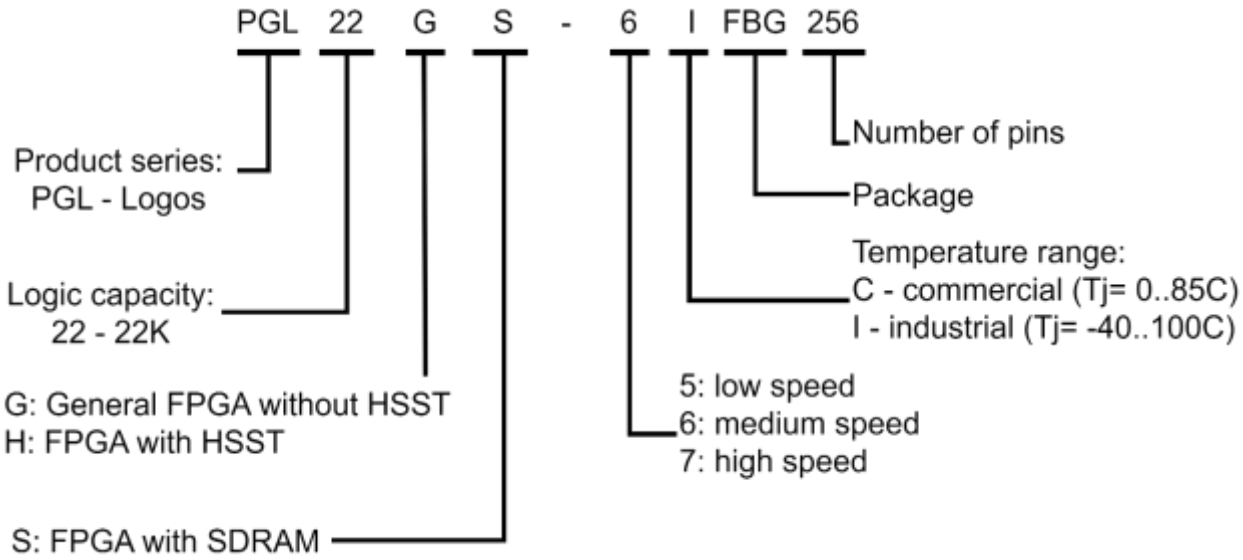


Figure 1 The numbering content and meaning of the Logos series FPGA product model

The description of product quality grades is shown in Table 6 below.

Table 6 Description of product quality grades

Product Series	Device	Speed Grades and Temperature Ranges	
		Commercial (C) 0°C to 85°C	Industrial (I) -40°C to 100°C
Logos	PGL12G	- 6C	- 6I
	PGL22G	- 6C	- 6I
	PGL25G	- 6C	- 6I
	PGL50G	- 6C	- 6I
	PGL50H	- 6C	- 6I
	PGL100H	- 6C	- 6I

2. WORKING CONDITIONS

2.1 Absolute Maximum Ratings

Table 7 Absolute Maximum Ratings

SYMBOL	DESCRIPTION	MINIMUM	MAXIMUM	UNITS
VCC	Core supply voltage	- 0.16	1.32	V
VCCAUX	Auxiliary power supply voltage (for IOB, LDO, etc.)	- 0.16	3.63	V
VCCAUX_A	Auxiliary supply voltage (for ADC, POR, Bandgap, etc.)	- 0.16	3.63	V
VCCIO	BANK IO supply voltage	- 0.16	3.63	V
VCCEFUSE	Efuse programming voltage	- 0.16	3.63	V
VCCIOCFG	BANKCFG supply voltage	- 0.16	3.63	V
V_I	DC input voltage	- 0.16	3.63	V

Note: Stresses above extreme ratings may cause permanent damage to the device. Operation at the rated values will not damage the device, but does not imply that the device will function properly at these limits. Devices work under extreme conditions for a long time, which will seriously affect the reliability of the device.

2.2 Input AC overshoot limit value

Table 8 IO input AC overshoot voltage limit

INPUT PIN	OVERSHOOT VOLTAGE	SPECIFICATION	TEMPERATURE	CONDITION	LIMIT VALUE	UNIT
I/O input voltage, with respect to ground	OVERSHOOT	industry	100 °C	DC	4.02	V
				55%	4.07	V
				30%	4.12	V
				17%	4.17	V
				9.5%	4.22	V
				5.5%	4.27	V
				3.1%	4.32	V
				1.7%	4.37	V
				1.0%	4.42	V
				0.5%	4.47	V
				0.3%	4.52	V
				0.2%	4.57	V
				0.1%	4.62	V
	UNDERSHOOT	industry	100 °C	DC	- 0.16	V
				72%	- 0.21	V
				55%	- 0.26	V
				40%	-0.31	V
				30%	- 0.36	V
				22%	- 0.41	V
				17%	- 0.46	V
				12%	- 0.51	V
				10%	- 0.56	V
				8%	- 0.61	V
				6%	- 0.66	V
				4%	- 0.71	V
				3%	- 0.76	V

2.3 Recommended Operating Conditions

Table 9 Recommended operating conditions for PGL12G and PGL22G

Symbol	Description	Minimum	Typical	Maximum	Units
VCC	Core supply voltage	1.045	1.1	1.155	V
VCCAUX	Auxiliary power supply voltage (for IOB, LDO, etc.)	3.135	3.3	3.465	V
VCCAUX_A	Auxiliary supply voltage (for ADC, POR, Bandgap, etc.)	3.135	3.3	3.465	V
VCCIO	BANK IO supply voltage	1.14	- -	3.465	V
VCCEFUSE	Efuse programming voltage	3.135	3.3	3.465	V
VCCIOCFG	BANKCFG supply voltage	1.425	- -	3.465	V
T_J (commercial grade)	Commercial Grade Chip Operating Temperature	0	- -	85	℃
T_J (industrial grade)	Industrial grade chip operating temperature	- 40	- -	100	℃

Note: The recommended operating voltage is within ± 5 % of the typical operating voltage

Table 10 PGL25G recommended working conditions

Symbol	Description	Minimum	Typical	Maximum	Units
VCC	Core supply voltage	1.14	1.2	1.26	V
VCCAUX	Auxiliary power supply voltage, including BANK configuration voltage, Efuse programming voltage, etc.	3.135	3.3	3.465	V
VCCIO	BANK IO supply voltage	1.14	- -	3.465	V
T_J (commercial grade)	Commercial Grade Chip Operating Temperature	0	- -	85	℃
T_J (industrial grade)	Industrial grade chip operating temperature	- 40	- -	100	℃

Note: The recommended operating voltage is within ± 5 % of the typical operating voltage

Table 11 PGL50G, PGL50H, PGL100H recommended working conditions

Symbol	Description		Minimum	Typical	Maximum	Units
VCC	Core supply voltage		1.14	1.2	1.26	V
VCCAUX	auxiliary supply voltage, Contains BANK configuration voltage, etc.	VCCAUX=3.3V	3.135	3.3	3.465	V
		VCCAUX=2.5V	2.375	2.5	2.625	V
VCCIO	BANK IO supply voltage		1.14	- -	3.465	V
VCCEFUSE	Efuse programming voltage		3.135	3.3	3.465	V
T_J (commercial grade)	Commercial Grade Chip Operating Temperature		0	- -	85	℃
T_J (industrial grade)	Industrial grade chip operating temperature		- 40	- -	100	℃

Note: The recommended operating voltage is within ± 5 % of the typical operating voltage

2.4 ESD (HBM, CDM), Latch Up indicator

Table 12 ESD, Latch-Up indicators

Human Body Model (HBM)	Charge Device Model (CDM)	Latch- up
±2000V	± 500V	± 100mA

3. DC CHARACTERISTICS

3.1 Hot-Socketing DC characteristics

Table 13 Hot-swap DC characteristics

Symbol	Description	Condition (clamp function off)	Min	Typ	Max	note
I_{DK}	Maximum Leakage Current	–0.5V < V IN < VCCIO MAX 0V < VCC < VCC (max), 0V < VCCIO < VCCIO (max), 0V < VCCAUX < VCCAUX (max)	-	-	+/- 1mA	each pad

Note 1: Vtp is the absolute value of the threshold voltage of the PMOS

3.2 IO input and output DC characteristics

The standard input and output voltage ranges of each single-ended IO level are shown in Table 14.

Table 14 single-ended IO level standard input and output voltage range

Single-ended IO	V_{IL}(V)		V_{IH}(V)		V_{OL} (V)	V_{OH}(V)
	min	max	min	max	max	min
LVTLL33 LVCMOS33	- 0.3	0.8	2	3.465	0.4	VCCIO -0.4
LVCMOS25	- 0.3	0.7	1.7	3.465	0.4	VCCIO -0.4
LVCMOS18	- 0.3	0.35VCCIO	0.65VCCIO	3.465	0.4	VCCIO -0.4
LVCMOS15	- 0.3	0.35VCCIO	0.65VCCIO	3.465	0.4	VCCIO_0.4
LVCMOS12	- 0.3	0.35VCCIO	0.65VCCIO	3.465	0.4	VCCIO -0.4
SSTL25_I	- 0.3	VREF - 0.18	VREF +0.18	3.465	0.54	VCCIO - 0.62
SSTL25_II	- 0.3	VREF - 0.18	VREF +0.18	3.465	0.35	VCCIO - 0.43
SSTL18_I	- 0.3	VREF - 0.125	VREF +0.125	3.465	0. 4	VCCIO -0.4
SSTL18_II	- 0.3	VREF - 0.125	VREF +0.125	3.465	0.28	VCCIO - 0.28
SSTL15_I SSTL15_I _DCI	- 0.3	VREF - 0.1	VREF+0.1	3.465	0.31	VCCIO - 0.31
SSTL15_II SSTL15_II_DCI	- 0.3	VREF - 0.1	VREF+0.1	3.465	0.31	VCCIO - 0.31
HSTL18_I	- 0.3	VREF - 0.1	VREF+0.1	3.465	0. 4	VCCIO -0.4

HSTL18_II	- 0.3	VREF - 0.1	VREF+0.1	3.465	0. 4	VCCIO -0.4
HSTL15_I **HSTL15_I_DCI**	- 0.3	VREF - 0.1	VREF+0.1	3.465	0. 4	VCCIO -0.4

Note: Only PGL22G supports DCI

The standard output current of each single-ended IO level is shown in the table below.

Table 15 Single-ended IO level standard output current

Single-ended IO	I_{OL}(mA)	I_{OH}(mA)	V_{REF}(V)	V_{TT}(V)
LVTTL **LVCMOS33**	4	- 4	-	-
	8	- 8	-	-
	12	-12	-	-
	16	-16	-	-
	24	-24	-	-
LVCMOS25	4	- 4	-	-
	8	- 8	-	-
	12	-12	-	-
	16	-16	-	-
LVCMOS18	4	- 4	-	-
	8	- 8	-	-
	12	-12	-	-
LVCMOS15	4	- 4	-	-
	8	- 8	-	-
LVCMOS12	2	- 2	-	-
	6	- 6	-	-
SSTL25_I	8.1	-8.1	0.45VCCIO 0.5VCCIO 0.55VCCIO	0.5VCCIO
SSTL25_II	16.2	- 16.2	0.45VCCIO 0.5VCCIO 0.55VCCIO	0.5VCCIO
SSTL18_I	6.7	-6.7	0.45VCCIO 0.5VCCIO 0.55VCCIO	0.5VCCIO
SSTL18_II	13.4	- 13.4	0.45VCCIO 0.5VCCIO 0.55VCCIO	0.5VCCIO
SSTL15_I **SSTL15_I_DCI**	7.5	-7.5	0.45VCCIO 0.5VCCIO 0.55VCCIO	0.5VCCIO
SSTL15_II **SSTL15_II_DCI**	8.8	-8.8	0.45VCCIO 0.5VCCIO 0.55VCCIO	0.5VCCIO
HSTL18_I	8	- 8	0.45VCCIO 0.5VCCIO 0.55VCCIO	0.5VCCIO
HSTL18_II	16	-16	0.45VCCIO 0.5VCCIO 0.55VCCIO	0.5VCCIO
HSTL15_I **HSTL15_I_DCI**	8	- 8	0.45VCCIO 0.5VCCIO 0.55VCCIO	0.5VCCIO

Note: Only PGL22G supports DCI, PGL22GS_LPG176 L0 BANK does not support all level standards using VREF

Table 16 BANK support description of input IO level standard

	model	IO standard	Device							
			PGL22G		PGL12G		PGL25G/PGL50G /PGL50H		PGL100H	
			BANKL0, BANKL1, BANKL2	BANKR0, BANKR1, BANKR2	BANKL0, BANKL1	BANKR0, BANKR1	BANK0, BANK2	BANK1, BANK3	BANK0, BANK2	BANK1 BANK3 BANK4 BANK5
enter	single ended	LVCMOS12 LVCMOS15 LVCMOS18 LVCMOS25 LVCMOS33 SSTL15_I SSTL15_II SSLT18_I SSTL18_II SSTL25_I SSTL25_II	support	support	support	support	support	support	support	support
		SSTL15_I_DCI SSTL15_II_DCI HSTL15_I_DCI	support	support	not support	not support	not support	not support	not support	not support
	differential	LVPECL33 LVDS25 SLVS MINI-LVDS SUB-LVDS TMDS RSDS PPDS TMDS SSTL15D_I SSTL15D_II HSTL15D_I MIPI	support	support	support	support	support	support	support	support
		SSTL15D_I_DCI SSTL15D_II_DCI HSTL15D_I_DCI	support	support	not support	not support	not support	not support	not support	not support

Table 17 Output IO level standard BANK support instructions

	model	IO standard	Device							
			PGL22G		PGL12G		PGL25G/PGL50G / PGL50H		PGL100H	
			BANKL0, BANKL1, BANKL2	BANKR0, BANKR1, BANKR2	BANKL0, BANKL1	BANKR0, BANKR1	BANK0, BANK2	BANK1, BANK3	BANK0, BANK2	BANK1 BANK3 BANK4 BANK5
output										

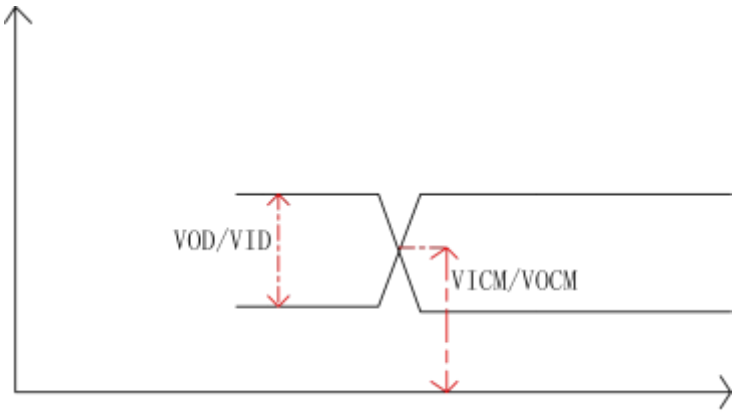
	single ended	LVCMOS12 LVCMOS15 LVCMOS18 LVCMOS25 LVCMOS33 SSTL15_I SSTL15_II SSLT18_I SSTL18_II SSTL25_I SSTL25_II	support	support	support	support	support	support	support	support
		SSTL15_I_DCI SSTL15_II_DCI HSTL15_I_DCI	support	support	not support	not support	not support	not support	not support	not support
	Differential	LVDS25 SLVS MINI- LVDS SUB-LVDS TMDS	support	support	not support	support	support	not support	support	not support
	class difference	PPDS RSDS LVPECL33	support	support	support	support	support	support	support	support

Table 18 BANK support instructions for bidirectional IO level standards

	MODEL	IO standard	Device							
			PGL22G		PGL12G		PGL25G/PGL50G / PGL50H		PGL 100H	
			BANKL0, BANKL1, BANKL2	BANKR0, BANKR1, BANKR2	BANKL0, BANKL1	BANKR0, BANKR1	BANK0, BANK2	BANK1, BANK3	BANK0, BANK2	BANK1 BANK3 BANK4 BANK5
TWO-WAY	SINGLE ENDED	LVCMOS12 LVCMOS15 LVCMOS18 LVCMOS25 LVCMOS33 SSTL15_I SSTL15_II SSTL18_I SSTL18_II SSTL25_I SSTL25_II	support	support	support	support	support	support	support	support
		SSTL15_I_DCI SSTL15_II_DCI HSTL15_I_DCI	support	support	not support	not support	not support	not support	not support	not support
	DIFFEREN	LVDS25 MINI-LVDS SUB-LVDS SLVS TMDS	not support	not support	not support	not support	not support	not support	not support	not support

	CLASS DIFFERENCE	SSTL15D_I SSTL15D_II HSTL15D_I SSTL18D_I SSTL18D_II SSTL25D_I SSTL25D_II LVPECL33 PPDS RSDS	support	support	support	support	support	support	support	support
		SSTL15D_I_DCI SSTL15D_II_DCI HSTL15D_I_DCI	support	support	not support	not support	not support	not support	not support	not support

The main electrical characteristic parameters of the differential IO level standard are defined as shown in the figure below, and the input and output voltage ranges are shown in Table 19 and Table 20.



Differential electric characteristic parameters

Table 19 Parameter requirements for differential input standards

STANDARD	V_{ICM} INPUT COMMON MODE LEVEL (V)			V_{ID} INPUT DIFFERENTIAL MODE LEVEL (V)		
	MIN	TYPE	MAX	MIN	TYPE	MAX
LVDS25	0.5	1.2	1.9	0.1	0.35	0.5
MINI- LVDS	0.4	--	1.9	0.2	0.4	0.6
SUB- LVDS	0.6	0.9	1.2	0.08	0.1	0.2
SLVS	0.07	--	0.3	0.08	--	0.46
LVPECL33	0.5	--	1.9	0.3	--	1.1

Table 20 Parameter requirements for differential output standards

STANDARD	V_{OCM} OUTPUT COMMON MODE LEVEL (V)			V_{OD} OUTPUT DIFFERENTIAL MODE LEVEL (V)		
	MIN	TYPE	MAX	MIN	TYPE	MAX
LVDS25	1	1.25	1.4	0.25	0.35	0.45
MINI- LVDS	1	1.2	1.4	0.3	--	0.6
SUB-LVDS	0.8	0.9	1	0.1	0.15	0.2
SLVS	0.15	0.2	0.25	0.14	0.2	0.27

4. AC CHARACTERISTICS

This chapter mainly lists the AC characteristics of each logic unit of Logos series FPGA under typical working conditions.

4.1 IO AC characteristic parameters

The switching characteristics of the IOB are shown in Table 21.

Table 21 IOB input and output delay

I/O STANDARD	T_{IOPI}	T_{IOOP}	T_{IOTP}	UNIT
	- 6	- 6	- 6	
LVTTL, 4mA, Slow	1.50	2.86	2.86	ns
LVTTL, 8mA, Slow	1.50	2.76	2.76	ns
LVTTL, 12mA, Slow	1.50	2.66	2.66	ns
LVTTL, 16mA, Slow	1.50	2.56	2.56	ns
LVTTL, 24mA, Slow	1.50	2.46	2.46	ns
LVTTL, 4mA, Fast	1.50	2.80	2.80	ns
LVTTL, 8mA, Fast	1.50	2.70	2.70	ns
LVTTL, 12mA, Fast	1.50	2.60	2.60	ns
LVTTL, 16mA, Fast	1.50	2.50	2.50	ns
LVTTL, 24mA, Fast	1.50	2.40	2.40	ns
LVCMOS33, 4mA, Slow	1.50	2.86	2.86	ns
LVCMOS33, 8mA, Slow	1.50	2.76	2.76	ns
LVCMOS33, 12mA, Slow	1.50	2.66	2.66	ns
LVCMOS33, 16mA, Slow	1.50	2.56	2.56	ns
LVCMOS33, 24mA, Slow	1.50	2.46	2.46	ns
LVCMOS33, 4mA, Fast	1.50	2.80	2.80	ns
LVCMOS33, 8mA, Fast	1.50	2.70	2.70	ns
LVCMOS33, 12mA, Fast	1.50	2.60	2.60	ns
LVCMOS33, 16mA, Fast	1.50	2.50	2.50	ns
LVCMOS33, 24mA, Fast	1.50	2.40	2.40	ns
LVCMOS25, 4mA, Slow	1.80	2.96	2.96	ns
LVCMOS25, 8mA, Slow	1.80	2.86	2.86	ns
LVCMOS25, 12mA, Slow	1.80	2.76	2.76	ns
LVCMOS25, 16mA, Slow	1.80	2.66	2.66	ns
LVCMOS25, 4mA, Fast	1.80	2.90	2.90	ns
LVCMOS25, 8mA, Fast	1.80	2.80	2.80	ns
LVCMOS25, 12mA, Fast	1.80	2.70	2.70	ns
LVCMOS25, 16mA, Fast	1.80	2.60	2.60	ns
LVCMOS18, 4mA, Slow	2.90	3.26	3.26	ns
LVCMOS18, 8mA, Slow	2.90	3.06	3.06	ns
LVCMOS18, 12mA, Slow	2.90	2.86	2.86	ns
LVCMOS18, 4mA, Fast	2.90	3.20	3.20	ns
LVCMOS18, 8mA, Fast	2.90	3.00	3.00	ns
LVCMOS18, 12mA, Fast	2.90	2.80	2.80	ns
LVCMOS15, 4mA, Slow	3.60	3.36	3.36	ns
LVCMOS15, 8mA, Slow	3.60	3.16	3.16	ns
LVCMOS15, 4mA, Fast	3.60	3.30	3.30	ns
LVCMOS15, 8mA, Fast	3.60	3.10	3.10	ns

LVCMOS12, 2mA, Slow	6.40	4.46	4.46	ns
LVCMOS12, 6mA, Slow	6.40	3.66	3.66	ns
LVCMOS12, 2mA, Fast	6.40	4.40	4.40	ns
LVCMOS12, 6mA, Fast	6.40	3.60	3.60	ns
SSTL25_I	1.20	2.80	2.80	ns
SSTL25_II	1.20	2.80	2.80	ns
SSTL18_I	1.30	3.00	3.00	ns
SSTL18_II	1.30	3.00	3.00	ns
SSTL15_I	1.60	3.00	3.00	ns
SSTL15_II	1.60	3.00	3.00	ns
SSTL135	1.80	3.30	3.30	ns
HSTL18_I	1.30	3.00	3.00	ns
HSTL18_II	1.30	3.00	3.00	ns
HSTL15_I	1.60	3.00	3.00	ns
LVDS25	1.20	2.40	2.40	ns
MINI_LVDS	1.20	2.40	2.40	ns
SUB_LVDS	1.20	2.40	2.40	ns
SLVS	1.20	2.40	2.40	ns
TMDS	1.20	2.40	2.40	ns
PPDS	1.20	2.40	2.40	ns
LVPECL	1.20	2.40	2.40	ns
RSDS	1.20	2.40	2.40	ns
BLVDS	1.20	2.40	2.40	ns
SSTL25D_I	1.20	2.80	2.80	ns
SSTL25D_II	1.20	2.80	2.80	ns
SSTL18D_I	1.30	3.00	3.00	ns
SSTL18D_II	1.30	3.00	3.00	ns
SSTL15D_I	1.60	3.00	3.00	ns
SSTL15D_II	1.60	3.00	3.00	ns
SSTL135D	2.00	3.30	3.30	ns
HSTL18D_I	1.30	3.00	3.00	ns
HSTL18D_II	1.30	3.00	3.00	ns
HSTL15D_I	1.60	3.00	3.00	ns

T_{IOPI}: The delay from IOB Pad to DIN of IOBUFFER through IBUF

T_{IOOP}: From DO of IOBUFFER to IOB through OBUF Pad delay.

T_{IOTP}: From TO of IOBUFFER to IOB through OBUF Pad delay.

Table 22 Output switching characteristics when IOB tri-state is enabled

category	Characteristic parameter description	Speed class	unit
		- 6	
T_{IOTPHZ}	T input to pad high-impedance	2.7	ns

Note: When the T_{IOTPHZ} parameter is tri-state enabled, from TO of IOBUFFER to IOB through OBUF Pad delay

The AC characteristics of the IOL are shown in Table 23 to Table 25

Table 23 IOL Register AC Parameters

category	AC characteristic parameter description		value	unit	Remark
			-6		
IFF	Setup/Hold time				
	CE -> CLK setup/hold	rising edge	0.131/-0.044	ns	
		falling edge	0.064/-0.031	ns	
	LRS -> CLK setup/hold	rising edge	0.277/-0.099	ns	
		falling edge	0.218/-0.089	ns	
	DIN -> CLK setup/hold	rising edge	0.053/-0.012	ns	
		falling edge	-0.004/-0.003	ns	
	combinatorial logic delay				
	DIN -> RX_DATA_DD	0 -> 1	0.150	ns	bypass model
		1 -> 0	0.150	ns	
	Sequential Delays timing delay				
	DIN -> RX_DATA	0 -> 1	0.237	ns	Latch model
		1 -> 0	0.233	ns	
	CLK -> Q output	0 -> 1	0.359	ns	
		1 -> 0	0.377	ns	
	LRS -> Q output	0 -> 1	0.539	ns	
		1 -> 0	0.539	ns	
OFF/TSFF	Setup/Hold time				
	TX_DATA -> CLK setup/hold	rising edge	0.143/-0.046	ns	
		falling edge	0.074/-0.032	ns	
	CE -> CLK setup/hold	rising edge	0.169/-0.058	ns	
		falling edge	0.123/-0.052	ns	
	TS_CTRL -> CLK setup/hold	rising edge	0.122/-0.058	ns	
		falling edge	0.074/-0.053	ns	
	Sequential Delays timing delay				
	TX_DATA -> do	0 -> 1	0.362	ns	Latch model
		1 -> 0	0.369	ns	
	CLK -> Q of OFF /Q of TSFF	0 -> 1	0.361	ns	
		1 -> 0	0.370	ns	
	Q output of LRS -> OFF / Q output of TSFF	0 -> 1	0.557	ns	
		1 -> 0	0.557	ns	

Note: The data in the above table is subject to the timing report of PDS

Table 24 Input Deserializer switch parameters

category	Characteristic parameter description		speed class	unit
			-6	
IGDDR	Signal Setup/Hold Time			
	PADI -> RCLK	rising edge	-0.001/0.022	ns
		falling edge	0.010/0.014	ns
	Sequential Delays timing delay			
	RCLK -> Q terminal	rising edge	0.259	ns
		falling edge	0.263	ns
	RCLK maximum frequency		266	MHz

Note: The data in the above table is subject to the timing report of PDS

Table 25 Output Serializer switch parameters

CATEGORY	CHARACTERISTIC PARAMETER DESCRIPTION		SPEED CLASS - 6	UNIT
OGDDR	Signal Setup/Hold Time			
	D -> RCLK	rising edge	0.209/-0.095	ns
		falling edge	0.181/-0.036	ns
	T -> RCLK	rising edge	0.221/-0.097	ns
		falling edge	0.183/-0.036	ns
	Sequential Delays timing delay			
	RCLK - > PADO / PADT	rising edge	0.633	ns
		falling edge	0.682	ns
	RCLK maximum frequency		266	MHz

Note: The data in the above table is subject to the timing report of PDS

4.2 CLM AC characteristic parameters

Table 26 CLM module AC characteristics

NO.	PARAMETER DESCRIPTION	VALUE	ATTRIBUTES	UNIT
		-6		
	Logic delay			
1	LUT5 Enter Ax/Bx/Cx/Dx to Y0/Y1/Y2/Y3 delay	0.513	MAX	ns
2	LUT5 Enter Ax/Bx/Cx/Dx and M0/M1 to Y6AB/Y6CD the delay	0.39	MAX	ns
3	LUT5 Enter Ax/Bx/Cx/Dx and M0/M1/M2 Delay to Y1 (LUT7)	0.54	MAX	ns
4	LUT5 Enter Ax/Bx/Cx/Dx and M0/M1/M2/M3 Delay to Y3 (LUT8)	0.585	MAX	ns
5	LUTs input Ax to cout the delay	0.37	MAX	ns
6	LUTs input Bx to cout the delay	0.387	MAX	ns
7	LUTs input Cx to cout the delay	0.436	MAX	ns
8	LUTs input Dx to cout the delay	0.431	MAX	ns
9	CIN input to cout the delay	0.201	MAX	ns
10	CIN Input to Y0/Y1/Y2/Y3 the delay	0.277	MAX	ns
	Timing parameters			
11	CLK Input relative to Q0/Q1/Q2/Q3 TCO	0.261	MAX	ns
12	CLK Enter TCO relative to Y0 (QP0)/Y2(QP1)	0.325	MAX	ns
13	Ax/Bx/Cx/Dx relative to DFF setup /hold	0.049/-0.026	MIN	ns
14	m relative to DFF setup /hold	0.025/-0.003	MIN	ns
15	CE relative to DFF setup /hold	0.185/-0.162	MIN	ns
16	RS relative to DFF setup /hold	0.185/-0.162	MIN	ns
17	CIN relative to DFF setup /hold	0.0263/-0.004	MIN	ns
18	SHIFTIN relative to DFF setup /hold	0.185/-0.162	MIN	ns
19	RS The minimum pulse width of	0.9	MIN	ns
	Distributed RAM timing parameters			
20	CLK -> Y0/Y1/Y2/Y3 meme read delay	0.72	MAX	ns
21	CLK -> RS (as WE) timing check, setup/hold	0.185/-0.162	MIN	ns
22	CLK -> M0/M1/M2/M3 address timing check, setup/hold	- 0.208/0.232	MIN	ns
23	CLK -> AD/BD/CD/DD data timing check, setup/hold	- 0.208/0.232	MIN	ns

4.3 DRM AC characteristic parameters

Table 27 DRM Module AC Characteristics

CATEGORY	AC CHARACTERISTIC PARAMETER DESCRIPTION	VALUE - 6	ATTRIBUTES	UNIT
Tco_9k	CLKA/CLKB->QA/QB (Output register not enabled, 9K mode)	3.550	MAX	ns
Tco_9k_reg	CLKA/CLKB->QA/QB (output register enabled, 9K mode)	0.957	MAX	ns
Tco_18k	CLKA/CLKB->QA/QB (output register disabled, 18K mode & FIFO mode)	3.580	MAX	ns
Tco_18k_reg	CLKA/CLKB->QA/QB (output register enable, 18K mode & FIFO mode)	0.990	MAX	ns
Tco_flag_full	CLKA->FULL(ALMOST_FULL) Flag	1.260	MAX	ns
Tco_flag_empty	CLKB->EMPTY(ALMOST_EMPTY) Flag	1.170	MAX	ns
Tsu_9k_ad/ Thd_9k_ad	Address input Setup/Hold time (9K mode)	- 0.130/0.184	MIN	ns
Tsu_9k_d/ Thd_9k_d	Data Entry Setup/Hold time (9K mode)	- 0.096/0.149	MIN	ns
Tsu_9k_ce/ Thd_9k_ce	CE input Setup/Hold time (9K mode)	0.070/-0.018	MIN	ns
Tsu_9k_we/ Thd_9k_we	WE input Setup/Hold time (9K mode)	0.028/-0.026	MIN	ns
Tsu_9k_be/ Thd_9k_be	BE input Setup/Hold time (9K mode)	- 0.031/0.085	MIN	ns
Tsu_9k_oe/ Thd_9k_oe	OCE input Setup/Hold time (9K mode)	- 0.040/0.086	MIN	ns
Tsu_9k_rst/ Thd_9k_rst	Synchronous reset input Setup/Hold time (9K mode)	0.022/0.023	MIN	ns
Tsu_18k_ad/ Thd_18k_ad	Address input Setup/Hold time (18k mode)	- 0.196/0.250	MIN	ns
Tsu_18k_d/ Thd_18k_d	Data Entry Setup/Hold time (18k mode)	- 0.103/0.157	MIN	ns
Tsu_18k_ce/ Thd_18k_ce	CE input Setup/Hold time (18k mode)	0.061/-0.010	MIN	ns
Tsu_18k_we/ Thd_18k_we	WE input Setup/Hold time (18k mode)	0.040/0.013	MIN	ns
Tsu_18k_be/ Thd_18k_be	BE input Setup/Hold time (18k mode)	0.042/0.012	MIN	ns
Tsu_18k_oe/ Thd_18k_oe	OCE input Setup/Hold time (18k mode)	- 0.056/0.092	MIN	ns
Tsu_18k_rst/ Thd_18k_rst	Synchronous reset input Setup/Hold time (18k mode)	0.038/0.008	MIN	ns
Tsu_fifo_wctl/ Thd_fifo_wctl	WREOP (WRERR) input Setup/Hold time	0.083/-0.037	MIN	ns
Tsu_fifo_rctl/ Thd_fifo_rctl	RDNAK input Setup/Hold time	0.058/-0.013	MIN	ns
Tmpw_norm	CLKA/CLKB MPW (NW/TW)	1.643	MIN	ns
Tmpw_rbw	CLKA/CLKB MPW (RBW)	2.350	MIN	ns
Tmpw_fifo	CLKA/CLKB MPW (FIFO)	1.766	MIN	ns

Note: The data in the above table is subject to the timing report of PDS

4.4 APM AC characteristic parameters

Table 28 APM Module AC Characteristics

AC CHARACTERISTIC PARAMETER DESCRIPTION	PRE-ADDER	MULTIPLIER	POST-ADDER	VALUE - 6	UNIT
Data / Control Pin to input register clk setup and hold time					
Z -> preadd unit register CLK setup/hold	YES	NA	NA	2.638/-0.712	ns
X-> preadd unit register CLK setup/hold	YES	NA	NA	2.604/-0.526	ns
Z- > input unit register CLK setup/hold	NA	NA	NA	0.850/-0.088	ns
X- > input unit register CLK setup/hold	NA	NA	NA	0.871/ -0.99	ns
Y -> input unit register CLK setup/hold	NA	NA	NA	0.876/-0.086	ns
MODEX - > preadd unit register CLK setup/hold	YES	NA	NA	1.422/-0.368	ns
Data Pin to pipeline register clk setup and hold time					
Y-> Multiplier unit register CLK setup/hold	NA	YES	NO	1.911/-0.381	ns
X-> Multiplier unit register CLK setup/hold	YES	YES	NO	2.415 / - 0.593	ns
X-> Multiplier unit register CLK setup/hold	NO	YES	NO	1.924 / - 0.443	ns
Z-> Multiplier unit register CLK setup/hold	YES	YES	NO	2.451/-0.660	ns
Data / control Pin to output register clk setup and hold time					
Y-> post add unit register CLK setup/hold	NA	YES	YES	2.606/-0.681	ns
X-> post add unit register CLK setup/hold	NO	YES	YES	2.643/-0.701	ns
X-> post add unit register CLK setup/hold	YES	YES	YES	3.129/-0.840	ns
Z-> post add unit register CLK setup/hold	YES	YES	YES	3.165/-0.931	ns
Z-> post add unit register CLK setup/hold	NA	NA	YES	2.713/-0.415	ns
CPI -> post add unit register CLK setup/hold	NA	NA	YES	2.200/-0.226	ns
Register from all levels clk to APM output Pin time					
Post add unit register CLK -> P output	NA	NA	NA	0.884	ns
Multiplier unit register CLK -> output	NA	NA	YES	0.881	ns
Pre add unit register CLK -> DPO _ output	YES	YES	YES	2.559	ns
Z input unit register CLK -> DPO _ output	NO	NO	YES	1.728	ns
Combinational logic delay from data / control pin to APM output pin					
Y -> P output	NA	YES	NO	2.474	ns
Y->P output	NA	YES	YES	3.068	ns
X ->P output	NO	YES	NO	2.094	ns
X ->P output	YES	YES	NO	2.474	ns
X -> P output	YES	YES	YES	3.068	ns
Z -> P output	YES	YES	YES	3.068	ns
CPI ->P output	NA	NA	YES	2.107	ns

Note: The data in the above table is subject to the timing report of PDS

4.5 PLL AC characteristic parameters

Table 29 PLL AC Characteristics

PARAMETER	DESCRIPTION	MINIMUM VALUE	TYPICAL VALUE	MAXIMUM VALUE	UNIT
F_{in}	PLL input reference frequency	5		625	MHz
t_{RST_PLL}	PLL initialization high level reset signal width	0.3			MS
F_{pfd}	PFD input frequency	5		320	MHz
F_{SW}	When the input clock automatic switching function is supported, the PLL input parameter Frequency supported by test clock			320	MHz
F_{OUT}	PLL output clock frequency	1.172		625	MHz
F_{VCO}	VCO working range	600		1250	MHz
t_{FPA}	Fine phase error (CLKOUT1 all settings)	- 50	0	50	ps
t_{OPW}	Output clock width (high or low)	0.8			ns
t_{OPJIT}	output clock period jitter (f_{OUT} >= 100MHz)			300	ps p -p
	output clock period jitter (f_{OUT} < 100MHz)			0.03	UIPP
t_{OPJIT_cyc}	Output clock cycle-to-cycle jitter (f_{OUT} >=100MHz)			300	ps p -p
	Output clock cycle-to-cycle jitter (f_{OUT} < 100MHz)			0.03	UIPP
t_{LOCK}	Lock time (5 – 320 MHz)			200	us
Input Clock Requirements					
t_{IPJIT_cyc}	Input clock cycle-to-cycle jitter (fPFD >=100MHz)			0.15	UIPP
	Input clock cycle-to-cycle jitter (fPFD <100MHz)			750	ps p -p
IN DUTY CYCLE	Input Clock Duty Cycle	40%		60%	-
OUT DUTY CYCLE	Output clock duty cycle (CLKOUT1, at 50 % setting)	45%	50%	55%	-

4.6 DQS AC characteristic parameters

DQS phase adjustment is as follows:

Table 30 DQS AC characteristics

CATEGORY	SPEED CLASS	AC CHARACTERISTIC PARAMETER DESCRIPTION			UNIT
		MINIMUM VALUE	TYPICAL VALUE	MAXIMUM VALUE	
DQS	- 6	15	25	34	ps

4.7 Global Clock Network AC Characteristic Parameters

Table 31 Global Clock Network AC Characteristics

NAME	DESCRIPTION	MAXIMUM FREQUENCY	MAXIMUM SKEW
		- 6	- 6
GLOBAL CLK	Global Clock Network	400MHZ	200PS

4.8 Regional Clock Network AC Characteristic Parameters

Table 32 Regional Clock Network AC Characteristics

NAME	DESCRIPTION	MAXIMUM FREQUENCY	MAXIMUM SKEW
		- 6	- 6
REGIONAL CLK	regional clock network	400MHZ	200PS

4.9 IO clock network AC characteristic parameters

Table 33 IO Clock Network AC Characteristics

NAME	DESCRIPTION	MAXIMUM FREQUENCY	MAXIMUM SKEW
		- 6	- 6
IO CLK	IO clock network	470	60PS

4.10 Configure and program AC characteristic parameters

4.10.1 Power-up Timing characteristics

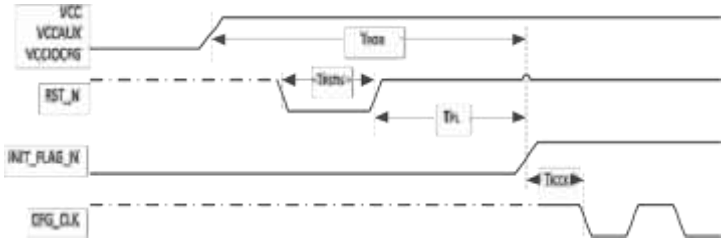


Figure 2 Device Power-up Timing characteristics

Table 34 Power-up Timing characteristic parameters

NAME	DESCRIPTION	VALUE	ATTRIBUTE	UNITS
T_{PL}	Program Latency	0.6	Maximum	ms
T_{POR}	Power-on-Reset	10.6	Maximum	ms
T_{ICCK}	CFG_CLK output delay	400	Maximum	ns
T_{RSTN}	RST_N low pulse width	384	Maximum	ns

4.10.2 Communication characteristics of each download mode

Table 35 AC characteristics of each download mode supported by Logos series FPGAs

CATEGORY	AC CHARACTERISTIC PARAMETER DESCRIPTION	VALUE	UNIT	ATTRIBUTES	REMARK
JTAG	TCK frequency	50	MHz	MAX	use download offline When loading, it is limited by the download line rate
	TCK low pulse width	10	ns	MIN	
	TCK high pulse width	10	ns	MIN	
	TMS/TDI setup time (TCK rising edge)	2	ns	MIN	
	TMS hold time (TCK rising edge)	1	ns	MIN	
	TDI hold time (TCK rising edge)	6	ns	MIN	
	TCK falling edge to TDO output valid	7	ns	MAX	
Serial Slave	CFG_CLK frequency	100	MHz	MAX	Download the clock from External Host device
	CFG_CLK low pulse width	5	ns	MIN	
	CFG_CLK high pulse width	5	ns	MIN	
	D[1] setup time (CFG_CLK rising edge)	2	ns	MIN	
	D[1] hold time (CFG_CLK rising edge)	1	ns	MIN	
	D[1] setup time (CFG_CLK falling edge)	2	ns	MIN	
	D[1] hold time (CFG_CLK falling edge)	1	ns	MIN	
	CFG_CLK falling edge to daisy_o output is valid	7.5	ns	MAX	
Parallel Slave	CFG_CLK frequency	100	MHz	MAX	Download the clock from External Host device
	CFG_CLK low pulse width	2.5	ns	MIN	
	CFG_CLK high pulse width	2.5	ns	MIN	
	D[31:0] setup time (CFG_CLK rising edge)	4	ns	MIN	
	D[31:0] hold time (CFG_CLK rising edge)	1	ns	MIN	
	CS_N/RDWR_N setup time (CFG_CLK rising edge)	3	ns	MIN	
	CS_N/RDWR_N/ Hold time (CFG_CLK rising edge)	1	ns	MIN	
	CFG_CLK rising edge to D[31:0] output is valid	9	ns	MAX	
	CFG_CLK rising edge to BUSY output is valid	8	ns	MAX	
	CS_N to daisy_o output delay	7	ns	MAX	
SPI Slave	CFG_CLK frequency	100	MHz	MAX	Download the clock from External Host device
	CFG_CLK low pulse width	2.5	ns	MIN	
	CFG_CLK high pulse width	2.5	ns	MIN	
	CS_N/D[3]/D[0] setup time (CFG_CLK rising edge)	3	ns	MIN	
	CS_N/D[3]/D[0] hold time (CFG_CLK rising edge)	1	ns	MIN	
	CFG_CLK falling edge to d[1] output is valid	8	ns	MAX	
	CFG_CLK falling edge to daisy_o output is valid	8	ns	MAX	

SPI Master	CFG_CLK frequency	50	MHz	MAX	The rate defaults to 12.5MHz
	CFG_CLK duty cycle	45%/55%		MIN/MAX	
	CFG_CLK frequency deviation	20%		MAX	
	D[7:0] setup time (CFG_CLK rising edge)	8	ns	MIN	
	D[7:0] hold time (CFG_CLK rising edge)	0	ns	MIN	
	D[7:0] setup time (CFG_CLK falling edge)	8	ns	MIN	
	D[7:0] hold time (CFG_CLK falling edge)	0	ns	MIN	
	CFG_CLK falling edge to d[0]/d[4] output is valid	2	ns	MAX	
	CFG_CLK falling edge to fcs_n/fcs2_n output is valid	2	ns	MAX	
	CFG_CLK falling edge to daisy_o output is valid	1	ns	MAX	
BPI Master	CFG_CLK frequency (asynchronous low speed)	10	MHz	MAX	
	CFG_CLK frequency (asynchronous high speed)	33	MHz	MAX	
	CFG_CLK frequency synchronous low speed)	25	MHz	MAX	
	CFG_CLK frequency (synchronous high speed)	50	MHz	MAX	
	CFG_CLK duty cycle	45%/55%		MIN/MAX	
	CFG_CLK frequency deviation	20 %		MAX	
	d[15:0] setup time (CFG_CLK rising edge)	8	ns	MIN	
	d[15:0] hold time (CFG_CLK rising edge)	0	ns	MIN	
	d[15:0] setup time (CFG_CLK falling edge)	8	ns	MIN	
	d[15:0] hold time (CFG_CLK falling edge)	0	ns	MIN	
	CFG_CLK falling edge to d[31:0]/adr[31:16] output is valid	3	ns	MAX	
	CFG_CLK falling edge to fce_n/fwe_n/foe_n/adv_n input valid out	2	ns	MAX	
	CFG_CLK falling edge to daisy_o output is valid	1	ns	MAX	
Internal Parallel Slave Mode	ipal_clk frequency	100	MHz	MAX	
	IPAL_CLK low pulse width	2.5	ns	MIN	
	IPAL_CLK high pulse width	2.5	ns	MIN	
	IPAL_CS_N/IPAL_RDWR_N/IPAL_DIN[31:0] Setup time (IPAL_CLK rising edge)	2	ns	MIN	
	IPAL_CS_N/IPAL_RDWR_N/IPAL_DIN[31:0] Hold time (IPAL_CLK rising edge)	1	ns	MIN	
	IPAL_CLK rising edge to IPAL_DOUT[31:0]/IPAL_BUSY output valid	4	ns	MAX	
	IPAL_CLK rising edge to RBCRC_VALID/SEU_VALID output valid	2	ns	MAX	
Master Internal SPI Mode	CFG_I_FCLK frequency	70	MHz	MAX	
	CFG_I_FCLK duty cycle	45%/55%		MIN/MAX	
	CFG_I_FCLK frequency deviation	20 %		MAX	
	i_d[3:0] setup time (CFG_I_FCLK rising edge)	6	ns	MIN	
	i_d[3:0] hold time (CFG_I_FCLK rising edge)	0	ns	MIN	
	i_d[3:0] setup time (CFG_I_FCLK falling edge)	6	ns	MIN	
	i_d[3:0] hold time (CFG_I_FCLK falling edge)	0	ns	MIN	
	CFG_I_FCLK falling edge to i_d[0] output is valid	1	ns	MAX	
	CFG_I_FCLK falling edge to i_fcs_n output valid	1	ns	MAX	

5. PERFORMANCE PARAMETERS

This chapter lists the performance features that implement common applications of Logos series FPGAs.

5.1 LVDS performance parameters

Table 36 LVDS performance

DESCRIPTION	IO RESOURCE	MAX RATE	UNIT
		- 6	
DDR LVDS Transmitter	OSERDES(DATA _WIDTH =7TO 8)	800	Mbps
DDR LVDS Receiver	ISERDES(DATA _WIDTH =7 TO 8)	800	Mbps

5.2 MIPI performance parameters

Table 37 MIPI performance

DESCRIPTION	MAX RATE	UNIT
	- 6	
MIPI Receiver	800	Mbps
MIPI Transmitter	800	Mbps

5.3 Storage Interface Performance Parameters

Table 38 Storage Interface Performance

NAME	DESCRIBE	HARD CORE SPEED	SOFT CORE SPEED	UNIT
		- 6	- 6	
DDR3	DDR3 interface	800	800	Mbps
DDR2	DDR2 interface	667	- -	Mbps
DDR	DDR interface	533	- -	Mbps
LPDDR	LPDDR interface	300	- -	Mbps

5.4 DRM performance parameters

Table 39 DRM performance

CATEGORY	SCHEMA DESCRIPTION	PERFORMANCE (MHZ)
		- 6
$F_{max\_DRM9K\_NW}$	DRM (NW Mode & Read Register Enable) @ 9K memory mode	300
$F_{max\_DRM9K\_TW}$	DRM (TW Mode & Read Register Enable) @ 9K memory mode	300
$F_{max\_DRM9K\_RBW}$	DRM (RBW Mode & Read Register Enable) @ 9K memory mode	200
$F_{max\_DRM18K\_NW}$	DRM (NW Mode & Read Register Enable) @ 18K memory mode	300
$F_{max\_DRM18K\_TW}$	DRM (TW Mode & Read Register Enable) @ 18K memory mode	300
$F_{max\_DRM18K\_RBW}$	DRM (RBW Mode & Read Register Enable) @ 18K memory mode	200
$F_{max\_DRM\_AFIFO}$	DRM (Asynchronous FIFO Mode & Read Register Enable)	275
$F_{max\_DRM\_SFIFO}$	DRM (synchronous FIFO Mode & Read Register Enable)	275

5.5 APM performance parameters

Table 40 APM performance

CONDITION	PERFORMANCE (MHZ)
	- 6
All registers used (using the registers of each level of APM)	400
Only use INREG and PREG (only use APM's input and output registers)	200
No register used (no registers used)	100

6. ADC CHARACTERISTIC PARAMETERS

This chapter mainly introduces the characteristic parameters of the ADC hard core of the Logos series FPGA, as shown in Table 40

Table 41 ADC hard core features

PARAMETER	DESCRIPTION	MINIMUM VALUE	TYPICAL VALUE	MAXIMUM VALUE	UNIT
VCCAUX_A	Analog supply voltage	2.97	3.3	3.63	V
VCC	Digital supply voltage	0.99	1.1	1.21	V
IVCCAUXA	Analog supply current		1.5		mA
Resolution	Resolution		10		bit
Sample Rate	1M mode		1		MSPS
	default scan mode			0.015	MSPS
Channel	Number of channels			12	
Voltage Reference	Reference voltage (internal or external)		2.5		V
Offset error	Offset error (Bipolar)		± 4		LSB
Gain error	Gain Error (External reference voltage)		± 0. 3		%FS
DNL	Differential Nonlinear (when FS>=1V)		± 1		LSB
INL	Integeral Nonlinear		± 3		LSB
SNR	Signal to Noise Ratio (bipolar full differential mode)	52			dB
Temperature Measurement	Temperature detection		-40~85 ℃: ± 4; 85~105 ℃: ± 6; 105~125 ℃: ± 8;		℃

Note: 1.1V digital power supply for ADC consumes less current

7. DEVICE QUIESCENT CURRENT

Table 42 Quiescent Current

NAME	DESCRIPTION	DEVICE	SPEED CLASS	UNIT
			-6	
I_{vcc}	Core Supply Quiescent Current	PGL12G	13	mA
		PGL22G	19	mA
		PGL25G	28	mA
		PGL50G	45	mA
		PGL50H	48	mA
		PGL100H	92	mA
I_{vccio}	BANK voltage quiescent current	PGL12G	3	mA
		PGL22G	3	mA
		PGL25G	3	mA
		PGL50G	3	mA
		PGL50H	3	mA
		PGL100H	6	mA
I_{vccaux_a}	Auxiliary Voltage VCCAUX_A Quiescent Current	PGL12G	2	mA
		PGL22G	2	mA
I_{vccaux}	Auxiliary Voltage VCCAUX (3.3V) Quiescent Current	PGL12G	11	mA
		PGL22G	32	mA
		PGL25G	9	mA
		PGL50G	8	mA
		PGL50H	8	mA
		PGL100H	9	mA

Note: 1. The above quiescent current values are tested at normal pressure and Tj=25 ℃. For 100 ℃, the analysis tool PPP can be used to evaluate with PPC, the core voltage of PGL12G and PGL22G adopts 1.1V, and the core voltage of PGL25G adopts 1.2V

2. The above data are obtained when the blank device has no output current load, no pull-up internal resistance, and all I/Os are in tri-state.

8. HIGH-SPEED SERIAL TRANSCEIVER (HSSTLP) FEATURES

This chapter mainly introduces the characteristics of the HSSTLP hard core of the Logos series FPGA, mainly including the absolute limit rated voltage / current, recommended operating conditions, AC/DC characteristics, and characteristics in support of typical protocol operating modes.

8.1 HSSTLP hard core absolute limit voltage

Table 43 HSSTLP absolute limit voltage

NAME	MINIMUM VALUE	MAXIMUM VALUE	UNIT	DESCRIPTION
VCCA_LANE	–0.5	1.32	V	HSST analog power supply 1.2V voltage
VCCA_PLL_0	–0.5	1.32	V	HSST PLL analog power supply 1.2V voltage
VCCA_PLL_1	–0.5	1.32	V	HSST PLL analog power supply 1.2V voltage

Note: Stresses above extreme ratings may cause permanent damage to the device.

8.2 HSSTLP hard core recommended working conditions

The table below lists the recommended operating voltage for the HSSTLP hard core of Logos series FPGAs

Table 44 HSSTLP hard core recommended working conditions

NAME	MINIMUM VALUE	TYPICAL VALUE	MAXIMUM VALUE	UNIT	DESCRIPTION
Voltage value					
VCCA_LANE	1.14	1.2	1.26	V	HSST analog power supply 1.2V voltage
VCCA_PLL_0	1.14	1.2	1.26	V	HSST PLL analog power supply 1.2V voltage
VCCA_PLL_0	1.14	1.2	1.26	V	HSST PLL analog power supply 1.2V voltage

8.3 HSSTLP hard core DC characteristic parameters

Table 45 HSSTLP hard core DC characteristics

NAME	MINIMUM VALUE	TYPICAL VALUE	MAXIMUM VALUE	UNIT	CONDITION	DESCRIPTION
Input and output signal DC characteristics						
HSST_V DINPP	150	-	1000	mV	External AC coupling	Differential input peak-to-peak current to press
HSST_V DIN	0	-	VCCA_LANE	mV	DC-coupled, VCCA_LANE =1.2V	Enter the absolute voltage value
HSST_V INCM	-	3/4 VCCA_LANE	-	mV	DC-coupled, VCCA_LANE=1.2V	Common mode input voltage value
HSST_V DOUTPP	800	-	-	mV	Swing setting max.	Differential output peak-to-peak voltage
HSST_V OUTCMDC	VCCA_LANE–HSST_V_{DOUTPP} /4			mV	DC common-mode output voltage is the case when the sending end is floating condition	
HSST_R DIN	-	100	-	Ω	Differential input resistance	
HSST_R DOUT	-	100	-	Ω	Differential output resistance	
HSST_TX SKEW	-	-	14	ps	P -side and N- side skew of Tx output	
HSST_C DEXT	-	100	-	f	Recommended External AC Coupling Capacitor Values	
Reference clock input DC characteristics						
HSST_VRCLKPP	400	-	1000	mV	Differential Input Peak-to-Peak Voltage	
HSST_R RCLK	-	100	-	Ω	Differential input resistance	
HSST_C RCLKEXT	-	100	-	f	Recommended External AC Coupling Capacitor Values	

8.4 AC Characteristics of High Speed Serial Transceiver HSSTLP

AC characteristics of the HSSTLP hard core are shown in Table 46 to Table 51

Table 46 HSSTLP hard core performance parameters

NAME	GRADE	UNIT	DESCRIPTION
	-6		
HSST_Fmax	6.375	Gbps	HSST MAX data rate
HSST_Fmin	0.6	Gbps	HSST minimum data rate
HSST_Fpllmax	3.1875	GHz	HSSTPLL MAX frequency
HSST_Fpllmin	1	GHz	HSSTPLL minimum frequency

The HSSTLP reference clock switching characteristics are shown in the table below.

Table 47 HSSTLP Hard Reference Clock Switching Characteristics

NAME	VALUE			UNIT	CONDITION	DESCRIPTION
	MINIMUM VALUE	TYPICAL VALUE	MAXIMUM VALUE			
HSST_FREFCLK	60	-	625	MHz	Reference Clock Frequency Range	
HSST_TRCLK	-	200	-	ps	20%-80 %	Reference Clock Rise Time
HSST_TFCLK	-	200	-	ps	80%- 20%	Reference Clock Fall Time
HSST_TRATIO	45	50	55	%	PLLs	Reference Clock Duty Cycle

Table 48 HSSTLP Hard PLL/Lock Lock Time Characteristics

NAME	VALUE			UNIT	CONDITION	DESCRIPTION
	MINIMUM VALUE	TYPICAL VALUE	MAXIMUM VALUE			
HSST_TPLLLOCK	-	-	1.5	ms		PLL lock time, the time from reset release to lock
HSST_TCDRLOCK	-	60,000	2,500,000	UI	After the PLL locks to the reference clock and after switching to external input data, the time for CDR to lock	CDR lock time

The HSSTLP hard core user clock switch characteristics are shown in the table below

Table 49 HSSTLP Hard User Clock Switching Characteristics

NAME	FREQUENCY	UNIT	DESCRIPTION
Data Interface Clock Switching Characteristics			
HSST_FT2C	160	MHz	MAX frequency of P_CLK2CORE_TX
HSST_FR2C	160	MHz	MAX frequency of P_CLK2CORE_RX
HSST_FTFC	160	MHz	MAX frequency of P_TX_CLK_FR_CORE
HSST_FRFC	160	MHz	MAX frequency of P_RX_CLK_FR_CORE
APB Dynamically configure interface clock switching characteristics			
HSST_FAPB	100	MHz	APB CLK MAX frequency

The switch characteristics of the HSSTLP hard core Transmitter on the sending side are shown in the table below.

Table 50 HSSTLP hard core Transmitter send side switch characteristics

NAME	MINIMUM VALUE	TYPICAL VALUE	MAXIMUM VALUE	UNIT	CONDITION	DESCRIPTION
HSST_T TXR	-	100	-	ps	20%-80 %	TX Rise Time
HSST_T TXF	-	100	-	ps	80%- 20%	TX fall time
HSST_T CHSKEW	-	-	500	ps	-	TX channel skew
HSST_VTXIDLEAMP	-	-	30	mV	-	Electrical idle Amplitude
HSST_VTXIDLETIME	-	-	150	ns	-	Electrical idle transition time
HSST_TJ 0.6G	-	-	0.1	UI	0.6Gbps	Total Jitter
HSST_DJ 0.6G	-	-	0.05	UI		Deterministic Jitter
HSST_TJ 1.25G	-	-	0.15	UI	1.25Gbps	Total Jitter
HSST_DJ 1.25G	-	-	0.07	UI		Deterministic Jitter
HSST_TJ 2.5G	-	-	0.3	UI	2.5Gbps	Total Jitter
HSST_DJ 2.5G	-	-	0.15	UI		Deterministic Jitter
HSST_TJ 3.125G	-	-	0.3	UI	3.125Gbps	Total Jitter
HSST_DJ 3.125G	-	-	0.15	UI		Deterministic Jitter
HSST_TJ 5.0G	-	-	0.35	UI	5.0Gbps	Total Jitter
HSST_DJ 5.0G	-	-	0.17	UI		Deterministic Jitter
HSST_TJ 6.375G	-	-	0.4	UI	6.375Gbps	Total Jitter
HSST_DJ 6.375G	-	-	0.15	UI		Deterministic Jitter

The switch characteristics of the receiving side of the HSSTLP hard-core Receiver are shown in the following table.

Table 51 HSSTLP hard core Receiver receiving side switch characteristics

NAME	MINIMUM VALUE	TYPICAL VALUE	MAXIMUM VALUE	UNIT	DESCRIPTION
HSST_T $_{RXIDLETIME}$	-		255	T_{REFCLK}	Time from RXELECIDLE state to LOS signal response
HSST_RX $_{VPPOOB}$	100	-	-	mV	OOB detection threshold peak-to-peak
HSST_RX $_{TRACK}$	- 5000	-	0	ppm	Receiver spread spectrum follow, modulation frequency 33kHz
HSST_RX $_{LENGTH}$	-	-	150	UI	Support the length of RX continuous long 0 or long 1
HSST_RX $_{TOLERANCE}$	- 1500	-	1500	ppm	Frequency Offset Tolerance of Data / Reference Clock
Sine Jitter Tolerance					
HSST_SJ_0.6	TBD	-	-	UI	Sine Jitter (1), 0.6Gbps
HSST_SJ_1.25	0.42	-	-	UI	Sine Jitter (1), 1.25Gbps
HSST_SJ_2.5	0.42	-	-	UI	Sine Jitter (1), 2.5Gbps
HSST_SJ_3.125	0.4	-	-	UI	Sine Jitter (1), 3.125Gbps
HSST_SJ_5.0	0.4	-	-	UI	Sine Jitter (1), 5.0Gbps
HSST_SJ_6.375	0.3	-	-	UI	Sine Jitter (1), 6.375Gbps

Note: 1. The frequency of the injected sinusoidal jitter is 80MHz

9. PCIE HARD CORE FEATURES

Table 52 PCIe performance parameters

NAME	VALUE	UNIT	DESCRIPTION
Fpclk	250	MHz	PCIe core clock frequency
Fpclk_div2	125	MHz	User interface MAX clock frequency

OPERATING PROCEDURES AND PRECAUTIONS

The device must be handled with anti-static precautions. Wear anti-static gloves when handling the chip to prevent the electrostatic impact of the human body charge on the chip and damage the chip. When inserting the chip into the base on the circuit board and when taking the chip out of the base on the circuit board, pay attention to the direction of force to ensure that the pins of the chip are evenly stressed. Do not damage the pins of the chip due to excessive force, making it unusable.

The following actions are recommended:

a) Devices should be operated on an anti-static workbench, or with finger cots;

b) Test equipment and appliances should be grounded;

c) Do not touch the device leads;

d) Devices should be stored in containers made of conductive material;

e) Plastic, rubber or silk fabrics that cause static electricity should be avoided during production, testing, use and transfer;

f) The relative humidity should be kept above 50% ± 30% as much as possible.

10. TRANSPORT AND STORAGE

The recommended chip storage environment is: temperature 20°C-35°C, relative humidity 50%±20% .

Use the designated moisture-proof and anti-static bag (MBB) to seal, and the bag contains a desiccant and a temperature indicator card; during transportation, ensure that the chip does not collide with foreign objects.

11. UNPACKING AND INSPECTION

When using the chip out of the box, please observe the product logo on the chip case. Make sure the product is clearly marked, free from smudges and scratches At the same time, pay attention to check the chip shell and pins. Make sure that the shell is not damaged or scratched, and the pins are

neat, missing or deformed.

12. QUALITY ASSURANCE AND AFTER-SALES SERVICE

Shenzhen Ziguang Tongchuang Electronics Co., Ltd., a subsidiary of Ziguang Group, specializes in the research, development, production and sales of programmable logic devices (FPGA, CPLD, etc.). The proprietary programmable logic device platform and system solutions are one of the important components of "core" in Tsinghua Unigroup's "core cloud strategy".

Ziguang Tongchuang has a registered capital of 300 million yuan and is a national high-tech enterprise. The product market covers communication networks, industrial control, video surveillance, consumer electronics and other fields.

Tsinghua Unigroup was founded in mainland China, headquartered in Shenzhen, and has branches in Shanghai and Beijing. The company has more than 400 employees, and R&D personnel account for more than 85%. It has nearly 200 patents, and invention and software patents account for about 85%. The company brings together global expert talent resources to create an excellent FPGA ecosystem environment.