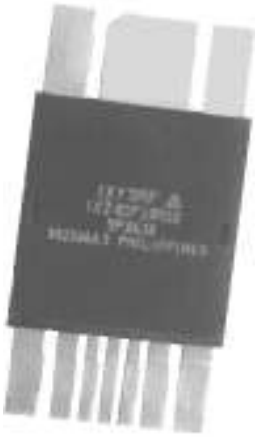
IXZ421DF12N100
RF Power MOSFET & DRIVER

Driver / MOSFET Combination
DEIC421 Driver combined with a DE375-102N12A MOSFET
Gate driver matched to MOSFET

1000 Volts
12 A
0.9 Ohms



Features

- Isolated Substrate
  - high isolation voltage (>2500V)
  - excellent thermal transfer
  - Increased temperature and power cycling capability
- IXYS advanced Z-MOS process
- Low $R_{DS(on)}$
- Very low insertion inductance (<2nH)
- No beryllium oxide (BeO) or other hazardous materials
- Built using the advantages and compatibility of CMOS and IXYS HDMOS™ processes
- Latch-Up Protected
- Low Quiescent Supply Current

Advantages

- Optimized for RF and high speed
- Easy to mount—no insulators needed
- High power density
- Single package reduces size and heat sink area

Applications

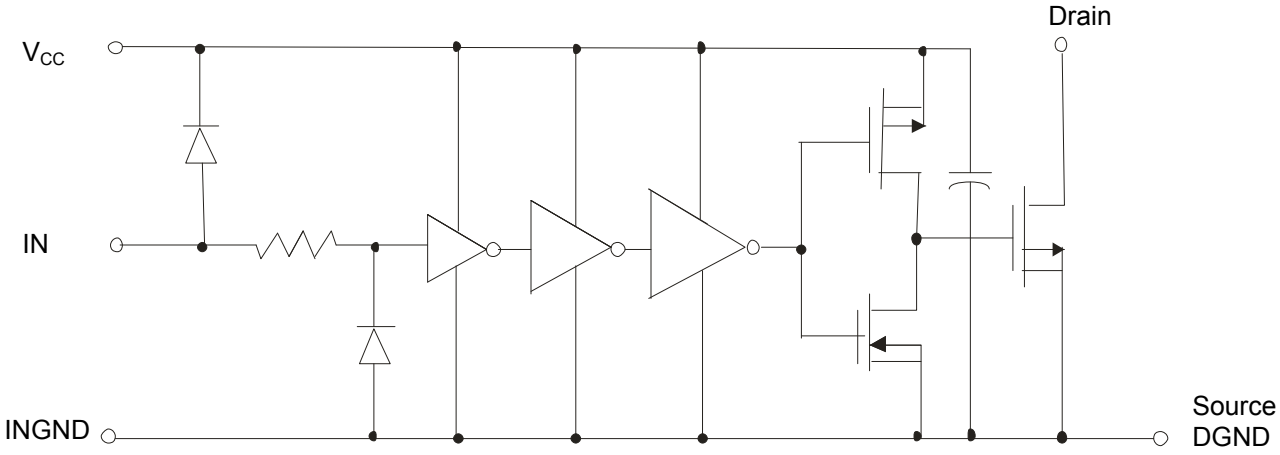
- Class D or E Switching Amplifier
- Multi MHz Switch Mode Power Supplies (SMPS)

Description

The IXZ421DF12N100 is a CMOS high speed high current gate driver and a MOSFET combination specifically designed Class D, E, HF, RF applications at up to 30MHz, as well as other applications. The IXZ421DF12N100 in pulse mode can provide 72A of peak current while producing voltage rise and fall times of less than 5ns, and minimum pulse widths of 8ns. The input of the driver is fully immune to latch up over the entire operating range. Designed with small internal delays, the IXZ421DF12N100 is suitable for higher power operation where combiners are used. Its features and wide safety margin in operating voltage and power make the IXZ421DF12N100 unmatched in performance and value.

The IXZ421DF12N100 is packaged in DEIs low inductance RF package incorporating DEI's RF layout techniques to minimize stray lead inductances for optimum switching performance. The IXZ421DF12N100 is a surface-mountable device.

Figure 1.
Functional Diagram



Device Specifications

Parameter	Value
Maximum Junction Temperature	150°C
Operating Temperature Range	- 40°C to 85°C
Weight	5.5g

Symbol	Test Conditions	Maximum Ratings
f_{MAX}	$I_D = 0.5I_{DM25}$	30MHz
V_{DSS}		1000V
V_{CC}, V_{CCIN}		20V
I_{DSS}	$V_{DS} = 0.8V_{DSS}$ T_J = 25C V_{GS} = 0V T_J = 125C	50uA 1mA
I_{DM25}	T_C = 25°C	12A
I_{DM}	T_C = 25°C, Pulse limited by T_{JM}	72A
I_{AR}	T_C = 25°C	12A
P_T (MOSFET and Driver)	T_C = 25°C	TBD 500W
R_{thJC}		0.25 °C/W
R_{thJHS}		0.45 °C/W

Device Performance

Symbol	Test Condition	Minimum	Typical	Maximum
$R_{ds(ON)}$	V_{CC} = 15V, $I_D = 0.5I_{DM25}$ Pulse Test, t ≤ 300µS, Duty Cycle ≤ 2%		0.92 Ω	
V_{CC}		8V	15V	20V
IN (Signal Input)		- 5V		V_{CC} + 0.3V
V_{IH} (High Input Voltage)		3.5V		
V_{IL} (Low Input Voltage)				0.8V
Z_{IN}	f = 1MHz		1248-j10550 Ω	
C_{stray}	f = 1MHz Any one pin to the back plane metal		46pf	
C_{OSS}	V_{GS} = 0V, V_{DS} = 0.8$V_{DSS(max)}$, f =1MHz		150pf	
t_{ONDLY}	T_C = 25°C V_{CC}, V_{CCIN}, V_{IN} = 15V 1µS Pulse, V_{DS}= 50V, R_L = 2.5Ω		32nS	
t_{OFFDLY}			35nS	
t_R	T_C = 25°C V_{CC}, V_{CCIN}, V_{IN} = 15V 1µS Pulse, V_{DS} = 50V, R_L = 2.5Ω		4nS	
t_F			3nS	

Fig. 2

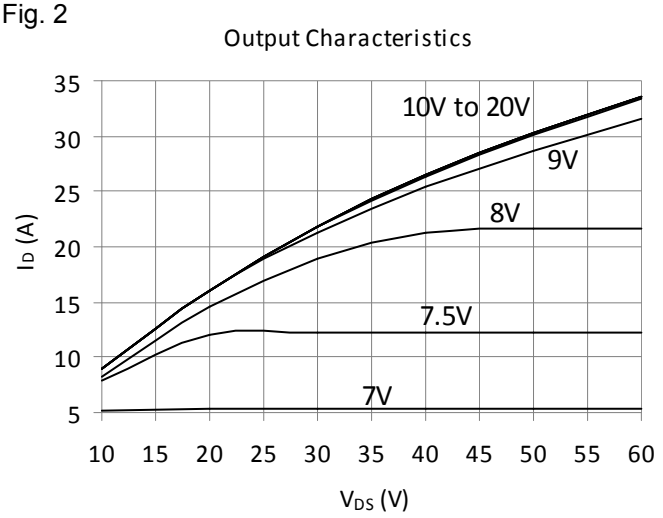


Fig. 3

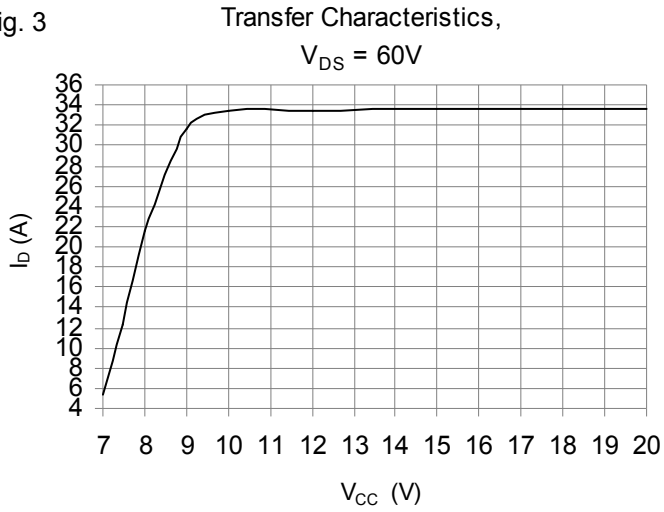


Fig. 4

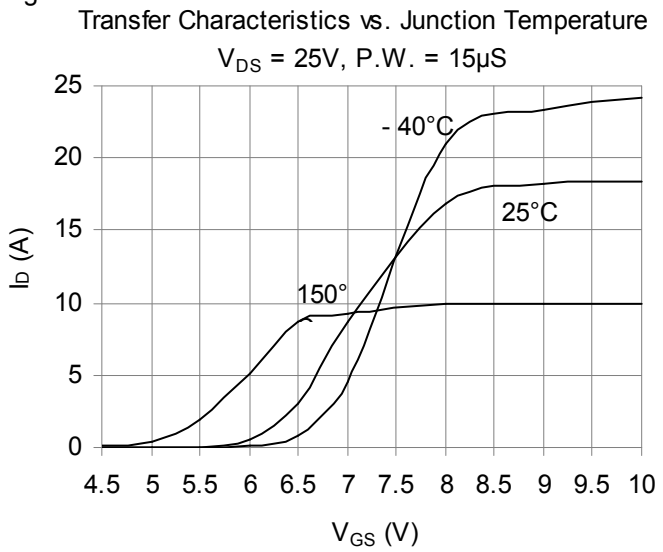


Fig. 5

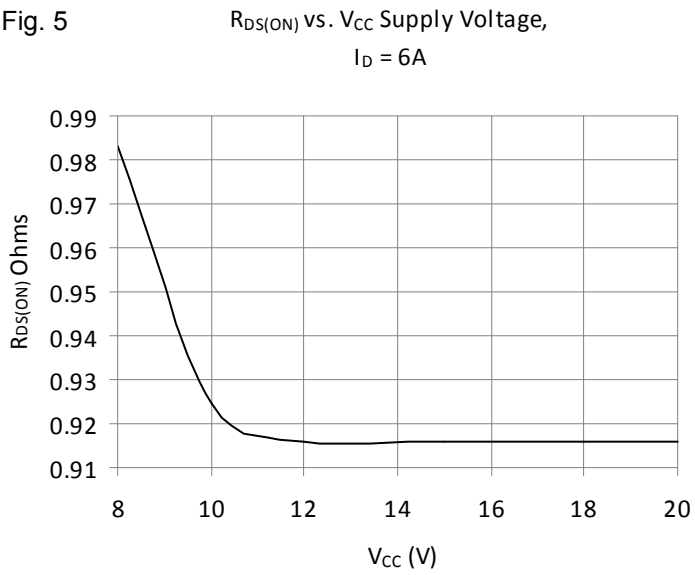


Fig. 6

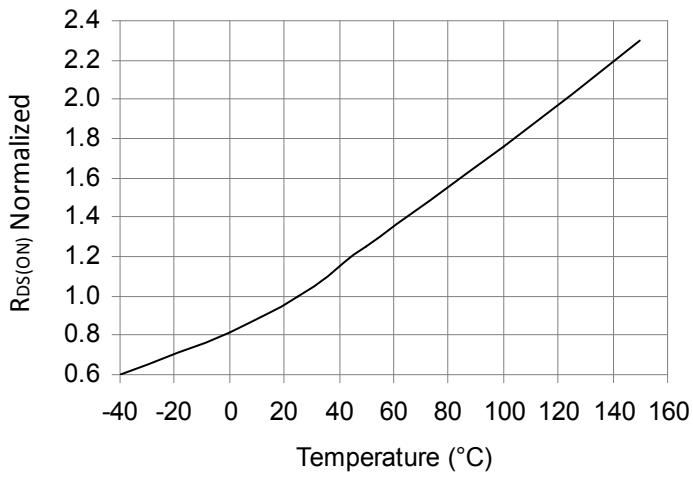


Fig. 7

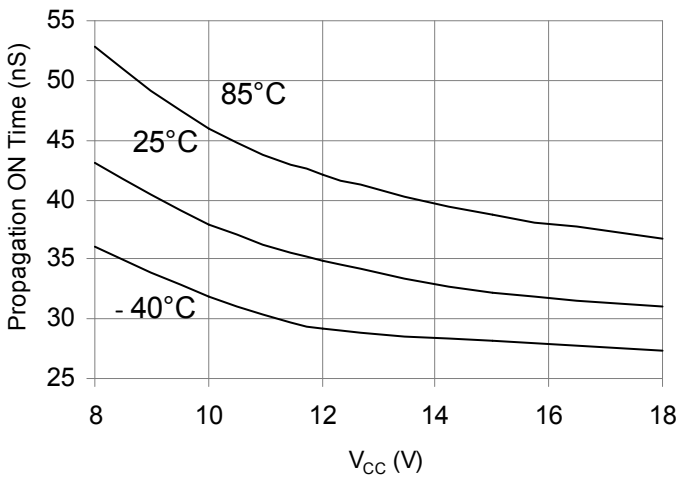


Fig. 8

Propagation OFF Delay vs. V_{CC} Supply Voltage
I_D = 6A

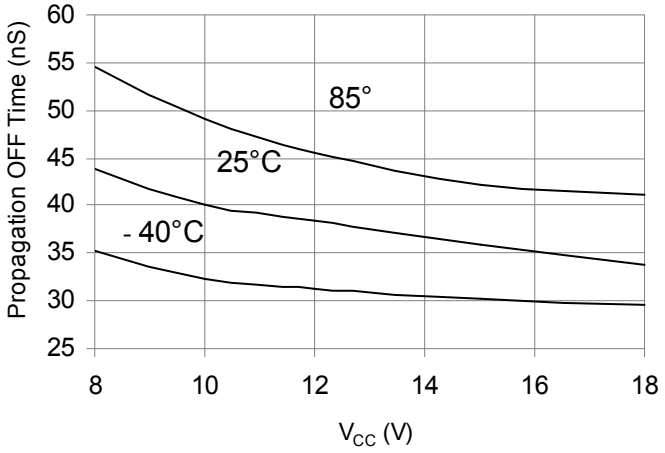


Fig. 9

Propragation Delay vs. Temperature
V_{CC} = 15V, I_D = 6A

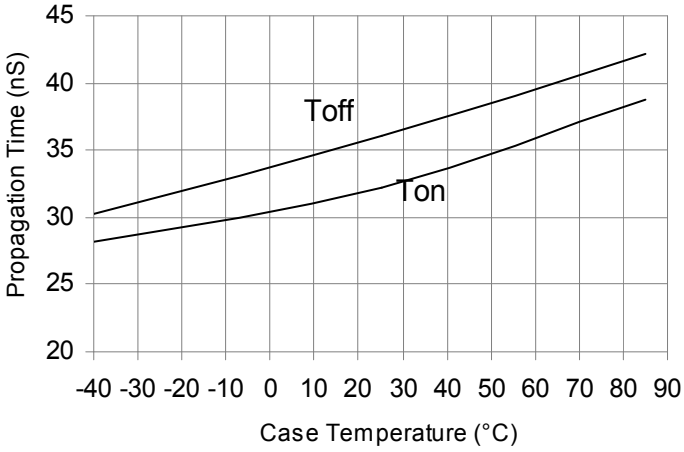


Fig. 10

Rise Time vs. V_{CC} Supply Voltage
I_D = 6A

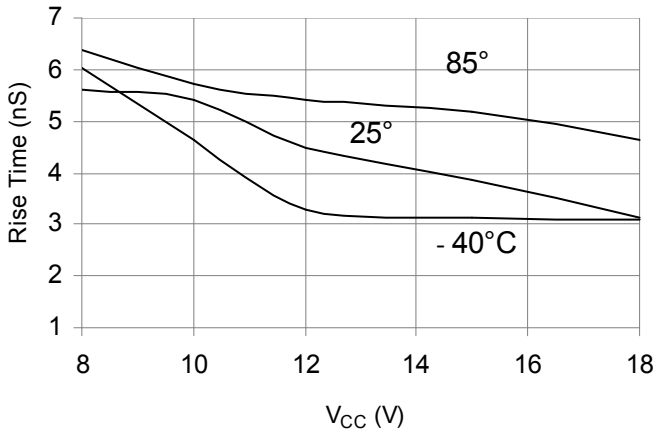


Fig. 11

Fall Time vs. V_{CC} Supply Voltage
I_D = 6A

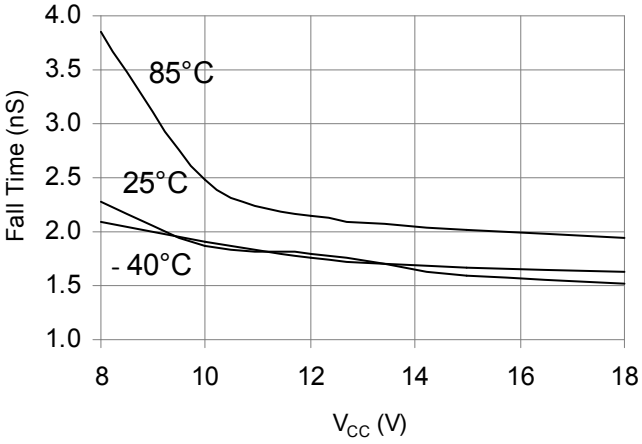


Fig. 12

Rise and Fall Time vs. Temperature
V_{CC} = 15V, I_D = 6A

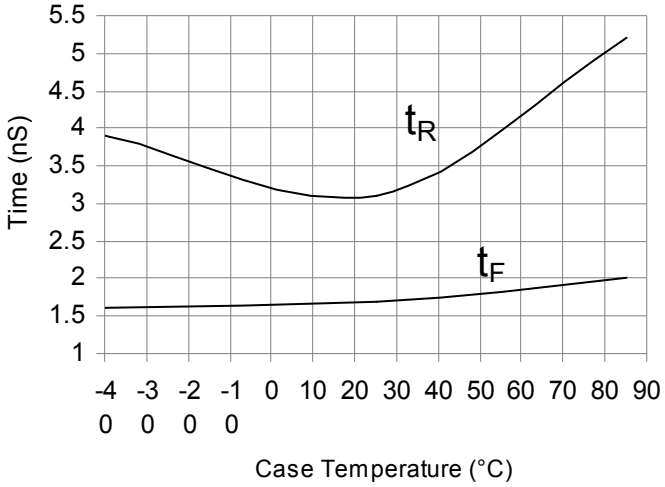
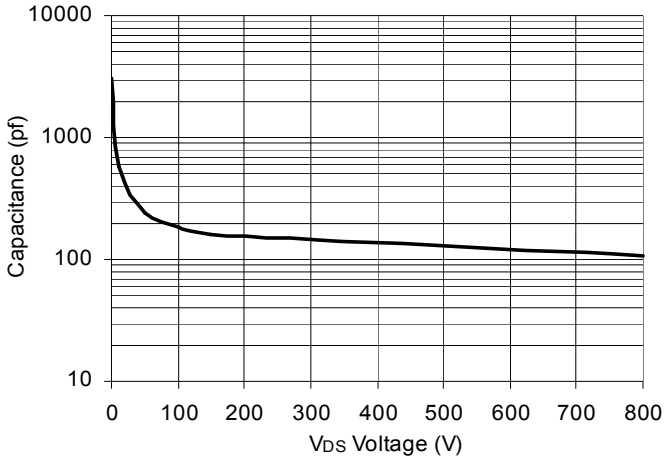


Fig. 13

V_{DS} vs. Output Capacitance



Lead Description

SYMBOL	FUNCTION	DESCRIPTION
Drain	MOSFET Drain	Drain of Power MOSFET.
Source	MOSFET Source	Source of Power MOSFET. This connection is common to DGND.
VCC	Driver Section Supply Voltage	Power supply input for the logic input and driver output sections.
IN	Input	Input signal.
DGND	Power Driver Ground	The system ground leads. Internally connected to all circuitry, these leads provide ground reference for the entire chip. These leads should be connected to a low noise analog ground plane for optimum performance.

Figure 14 Package Drawing

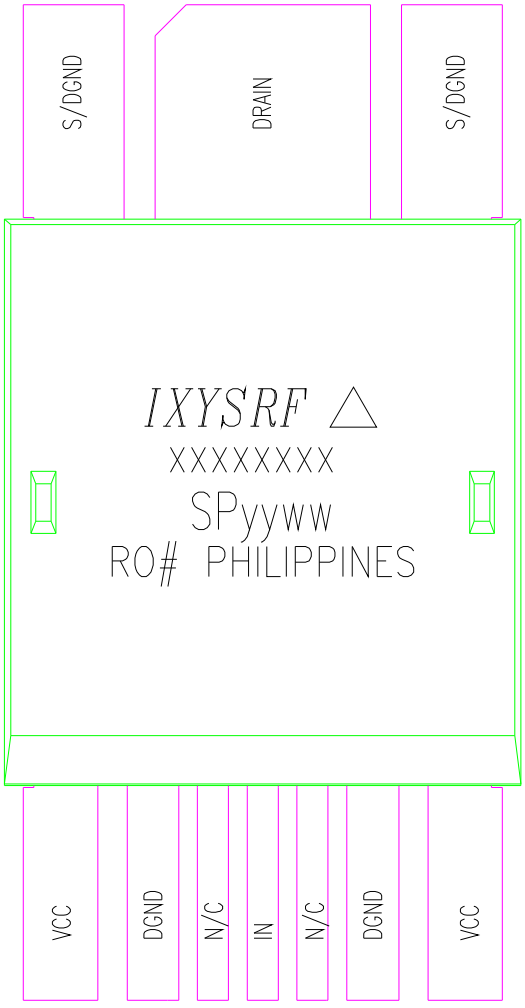
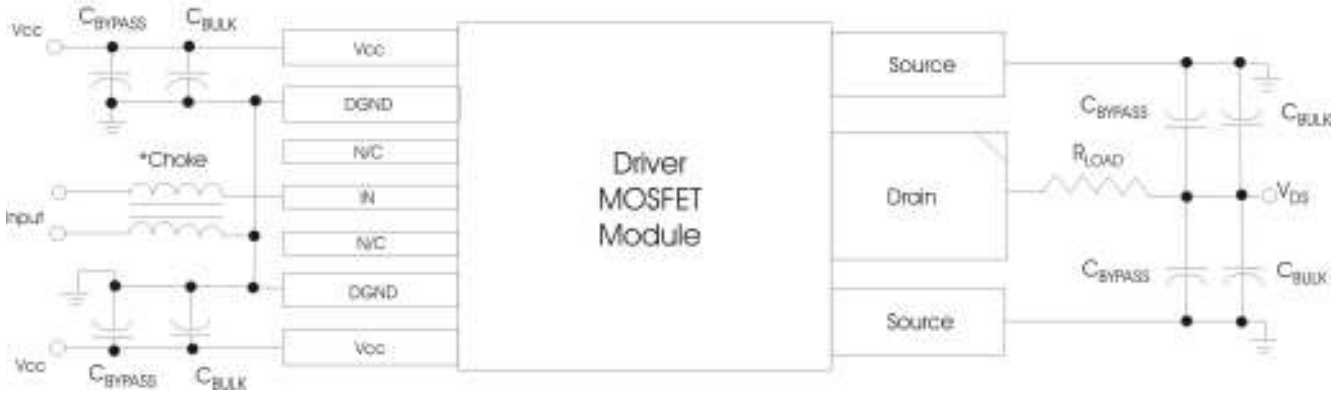


Figure 15 Test Circuit



***Choke– A Common Mode Choke is optional and can be used to help stabilize threshold levels due to ground bounce and minimize false triggering.**

C_{BULK}-

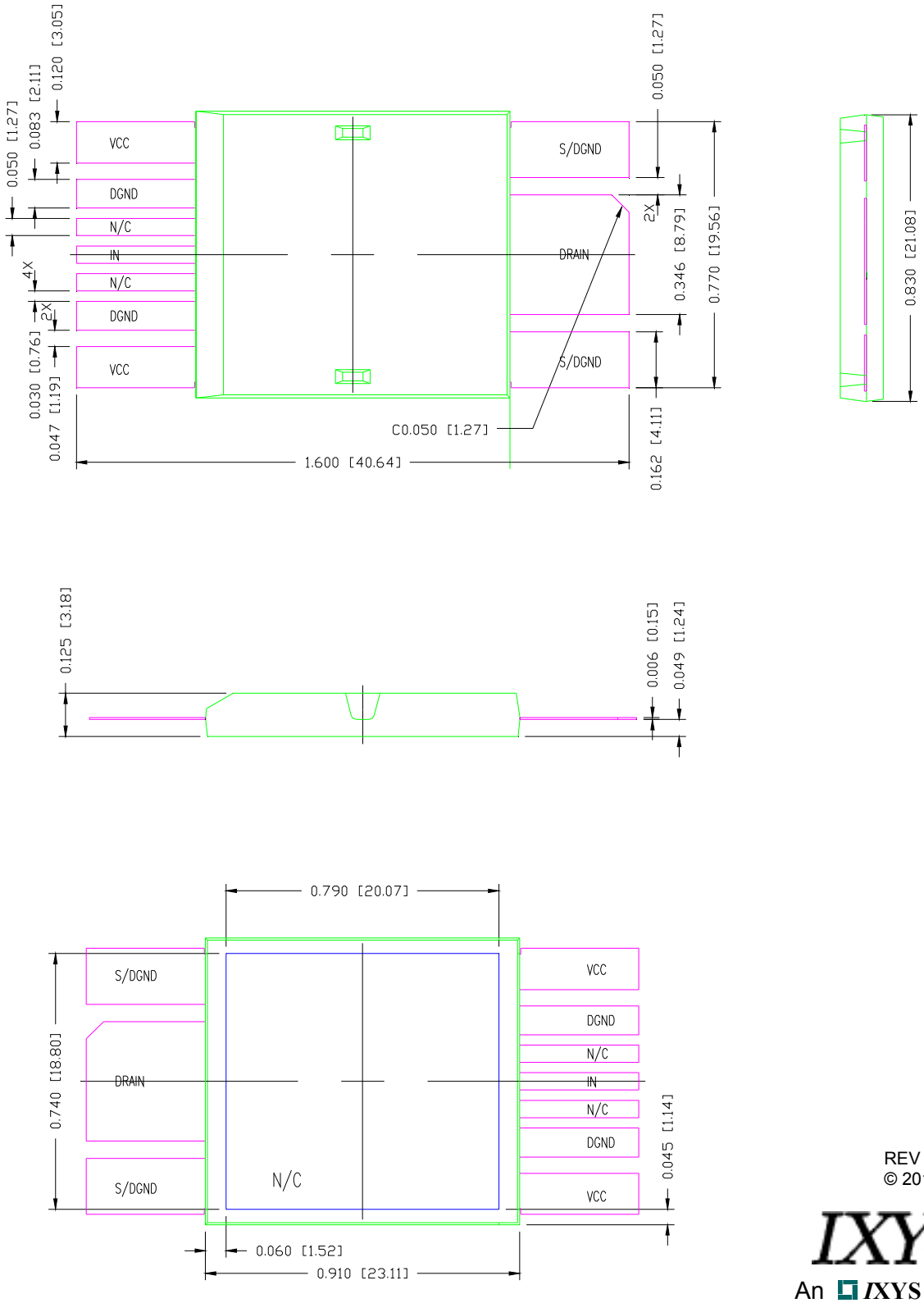
Bulk capacitance helps to stabilize both Vds for the drain Drain circuit and Vcc for the Driver circuit. Actual values vary according to load and operating conditions. For the driver section, Tantalum capacitors are recommended for their low ESR and fast energy delivery.

C_{BYPASS}-

Ideally, the benefits realized through bypass capacitance increase as more is used with overlapping impedance curves, lowering the overall broadband impedance to ground. Typically a range of 0.1uF, 0.01uF, 0.001uF capacitors in sufficient quantities give good results.

Circuit and PCB layout should be carefully considered for optimized operation. Each of the Vcc pins on the driver section should be treated as its own supply pin as it applies to bulk and bypass capacitance considerations. Likewise, the source pins of the MOSFET are connected symmetrically to the MOSFET and the ground return path for bulk and bypass capacitance should also be noted in the layout. Excessive parasitic inductance can result in V = L di/dt drops causing unstable operation.

Fig. 16 IXZ421DF12N100 Package Outline



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