Doc. version :	0.0
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Product Specification

7.0" COLOR TFT-LCD MODULE

MODEL NAME: A070VW04 V0

< □ >Preliminary Specification

< >Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0	2007/01/23		Draft.

Contents

A. General Description

A070VW04 is a amorphous transmissive type TFT (Thin Film Transistor) LCD (Liquid crystal Display). This model is composed of TFT-LCD, drive IC, FPC (flexible printed circuit), and backlight unit.The timing controller is embedded, so it is easily to design for consumer product.

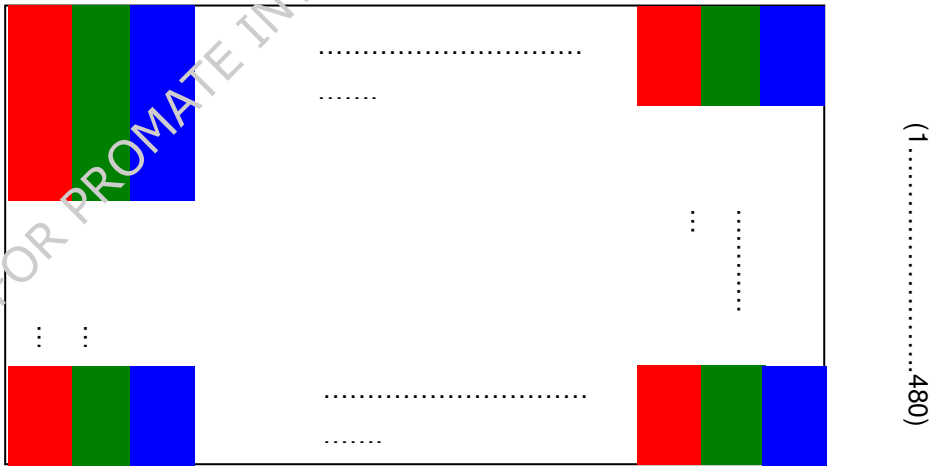
B. Features

- 7-inch display size
- WVGA resolution and stripe dot arrangement
- Built in timing controller
- LED backlight
- Standby mode supported
- Up/Down, Left/Right reversion selection
- SYNC + DE Mode
- Parallel 18/24bits interface support
- 16 M color supported
- Wide viewing angle
- RoHS compliant green design

C. General Information

NO.	Item	Unit	Specification	Remark
1	Display Resolution	dot	800RGB(H)×480(V)	
2	Active Area	mm	152.40(H)×91.44(V)	
3	Screen Size	inch	7.0(Diagonal)	
4	Pixel Pitch	mm	0.1905(H)×0.1905(V)	
5	Color Configuration	--	R. G. B. Stripe	Note 1
6	Color Depth	--	16.7M Colors	Note 2
7	Overall Dimension	mm	164(H) × 103(V) × 5.1(T)	Note 3
8	Weight	g	153.5 +/- 10%	
9	Panel surface treatment	--	Anti-Glare	
10	Display Mode	--	Normally White	

Note 1: Below figure shows dot stripe arrangement.

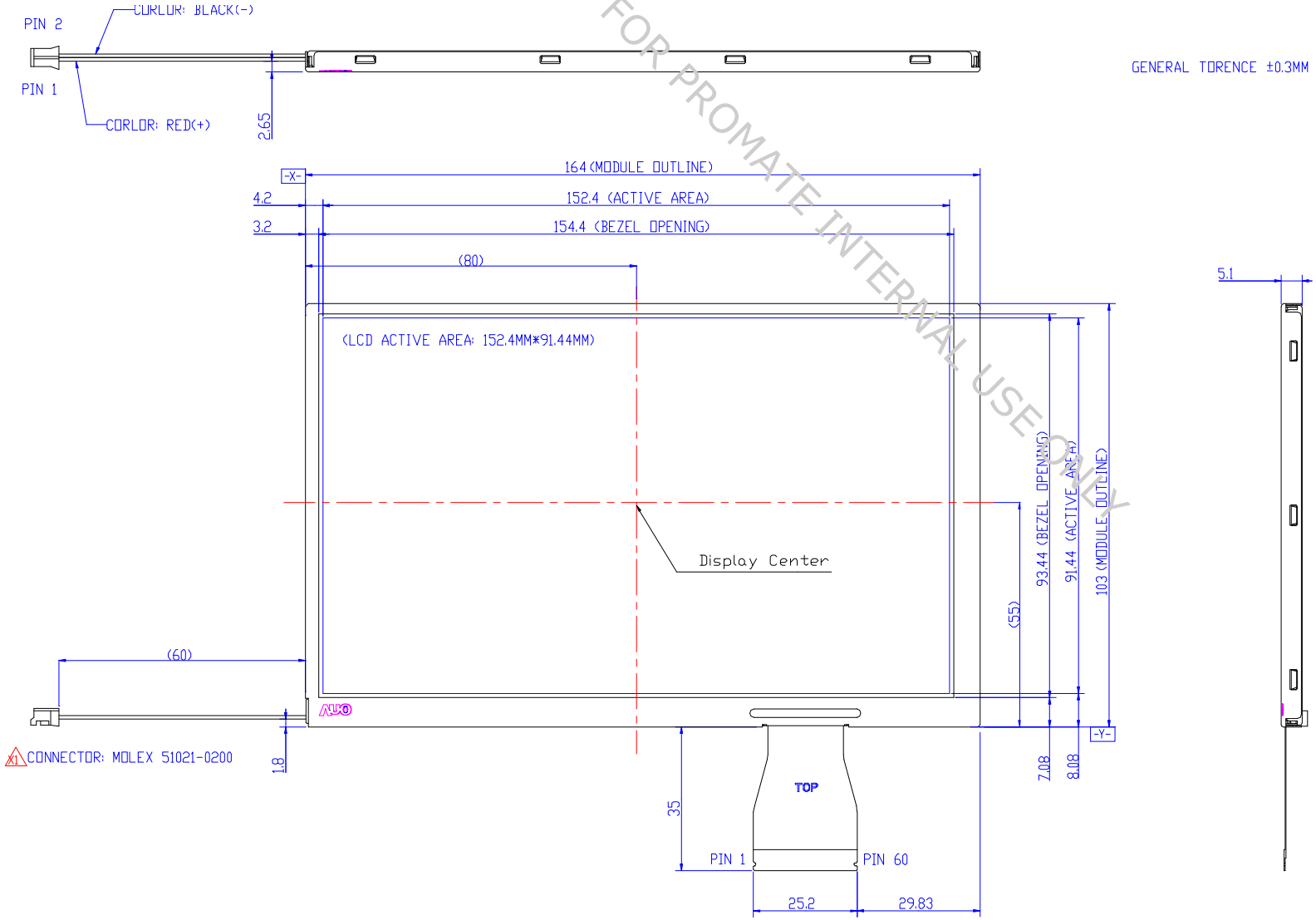


Note 2: The full color display depends on 8-bit data signal (pin 4~27).

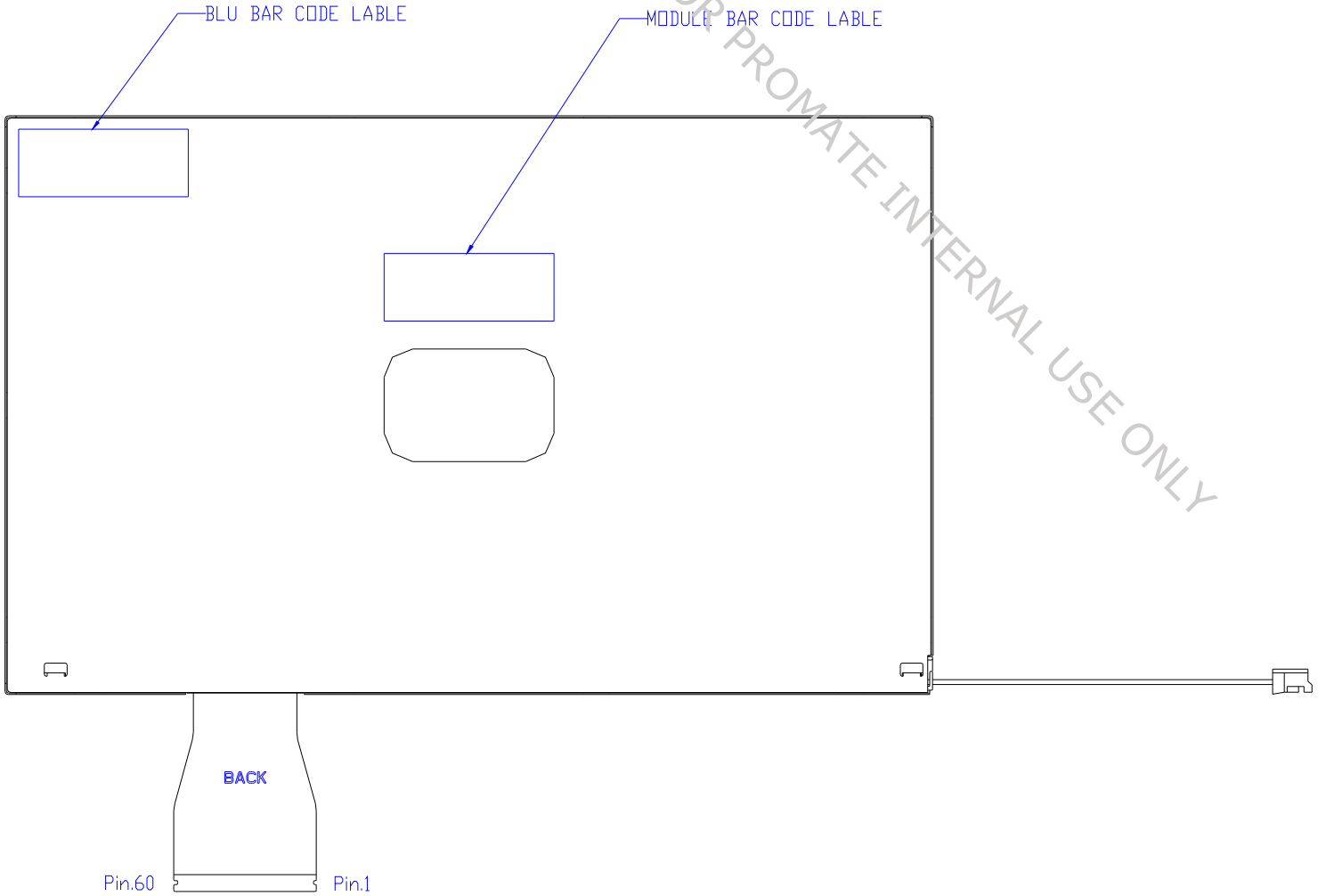
Note 3: Not include blacklight cable and FPC. Refer next page to get further information.

D. Outline Dimension

1. TFT-LCD Module – Front View



2. TFT-LCD Module – Rear View



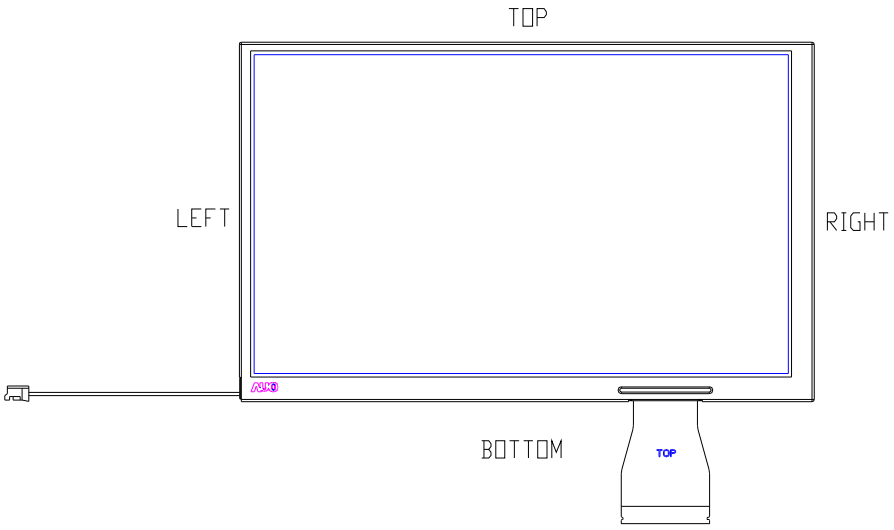
E. Electrical Specifications

1. FPC Pin Assignment (HRS FH27-60S-0.4SH)

Pin no	Symbol	I/O	Description
1	AGND2	P	Analog Ground
2	AVDD2	P	Analog Power
3	VDD	P	Digital Power
4	R0	I	Data input (LSB)
5	R1	I	Data input
6	R2	I	Data input
7	R3	I	Data input
8	R4	I	Data input
9	R5	I	Data input
10	R6	I	Data input
11	R7	I	Data input (MSB)
12	G0	I	Data input (LSB)
13	G1	I	Data input
14	G2	I	Data input
15	G3	I	Data input
16	G4	I	Data input
17	G5	I	Data input
18	G6	I	Data input
19	G7	I	Data input (MSB)
20	B0	I	Data input (LSB)
21	B1	I	Data input
22	B2	I	Data input
23	B3	I	Data input
24	B4	I	Data input
25	B5	I	Data input
26	B6	I	Data input
27	B7	I	Data input (MSB)
28	DCLK	I	Clock input
29	DE	I	Data enable signal
30	HSYNC	I	Horizontal sync input. Negative polarity
31	VSYNC	I	Vertical sync input. Negative polarity
32	SCL	I	Serial communication clock input
33	SDA	I	Serial communication data input
34	CSB	I	Serial communication chip select
35	FBA	I	DCDC feed back signal

36	VDD	P	Digital Power
37	DRVA	O	DCDC PWM signal
38	GND	P	Digital ground
39	AGND1	P	Analog ground
40	AVDD1	P	Analog Power
41	VCOMin	I	For external VCOM DC input (Optional)
42	NC	-	Not connect
43	NC	-	Not connect
44	VCOM	O	connect a capacitor
45	V10	P	Gamma correction voltage reference
46	V9	P	Gamma correction voltage reference
47	V8	P	Gamma correction voltage reference
48	V7	P	Gamma correction voltage reference
49	V6	P	Gamma correction voltage reference
50	V5	P	Gamma correction voltage reference
51	V4	P	Gamma correction voltage reference
52	V3	P	Gamma correction voltage reference
53	V2	P	Gamma correction voltage reference
54	V1	P	Gamma correction voltage reference
55	NC	-	Not connect
56	VGH	P	Positive power for TFT
57	GVCC	P	Digital Power
58	VGL	P	Negative power for TFT
59	GGND	P	Digital Ground
60	CAP	C	Connected to a capacitor

I: Input pin; P: Power pin; G: Ground pin; C: capacitor pin



2 Absolute Maximum Ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power voltage	VCC	GND=0	-0.5	5	V	Note 1
	AVDD	AGND=0	-0.5	15	V	Note 1
Operating temperature	Topa	--	0	60	□	Ambient Temperature
Storage temperature	Tstg	--	-10	70	□	Ambient Temperature

Note 1: Functional operation should be restricted under normal ambient temperature.

F. Electrical Characteristics

The following items are measured under stable condition and suggested application circuit.

1 TFT- LCD Typical Operation Condition (AGND = AGND2 = GND = GGND = 0V)

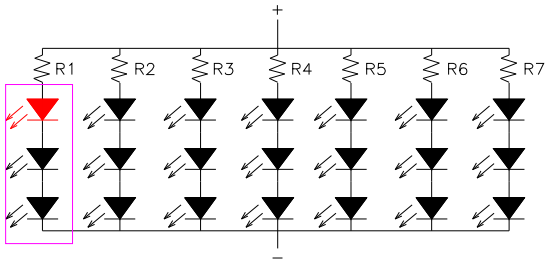
ITEM		Symbol	MIN.	TYP.	MAX.	UNIT	Remark
Power supply		VCC	3.3		3.6	V	
		AVDD	TBD	TBD	TBD	V	
		VGH	TBD	TBD	TBD	V	
		VGL	TBD	TBD	TBD	V	
Input Signal	H Level	V_{IH}	$0.7V_{CC}$	-	V_{CC}	V	
	L Level	V_{IL}	GND	-	$0.3V_{CC}$	V	
Input Reference Voltage		V1 ~ V5	AVDD/2	-	AVDD – 0.1	V	
		V6 ~ V10	0.1	-	AVDD/2	V	
VCOM		V_{CDC}	TBD	TBD	TBD	V	

Note: Above every operation range is based on stable operation from suggested application circuit.

2. Backlight Driving Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED lightbar Current	I_L	---	160	---	mA	---
LED light bar Voltage	V_L	---	12	---	V	---
LED Life Time	L_L	10,000	---	---	Hr	Note 2, 3

Note 1: The LED driving condition is defined for LED module (21 LED).



Note 2: Define “LED Lifetime”: brightness is decreased to 50% of the initial value. LED Lifetime is restricted under normal condition, ambient temperature = 25□ and LED lightbar voltage = 12V.

Note 3: If it uses larger LED lightbar voltage more than 12V, it maybe decreases the LED lifetime.

3. AC Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clock High time	T_{WCL}		8	-	-	ns
Clock Low time	T_{WCH}		8	-	-	ns
Clock rising time	T_{RCLK}		-	-	1	ns
Clock falling time	T_{ACK}		-	-	1	ns
Hsync setup time	T_{HSU}		5			ns
Hsync hold time	T_{HHD}		10			ns
Vsync setup time	T_{VSU}		0			ns
Vsync hold time	T_{VHD}		2			ns
Data setup time	T_{DSU}		5			ns
Data hold time	T_{DHD}		10			ns
Data enable set-up time	T_{ESU}		4			ns
Data enable hold time	T_{EHD}		2			ns

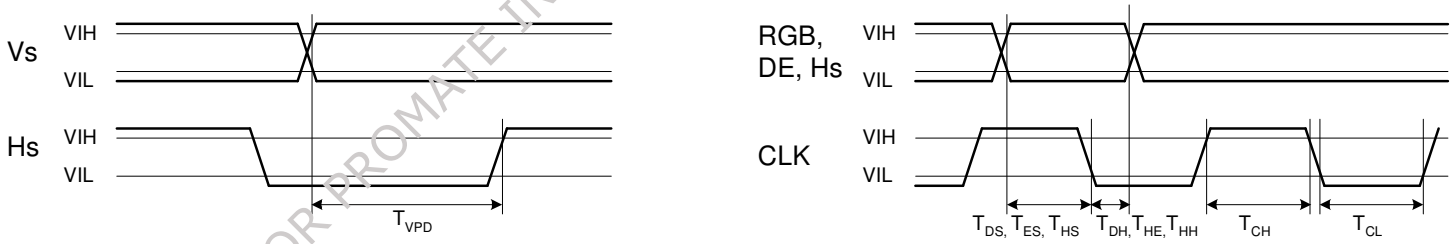


Figure 1 : Input timing details

4. RGB Parallel Input Timing

a. Horizontal Timing

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX	UNIT
DCLK frequency	F_{DCLK}		25	33	40	MHz
DCLK period	T_{DCLK}		25	30.3	40	ns
Hsync Period (= T_{HD} + T_{HBL})	T_H		986	1056	1183	DCLK
Active Area	T_{HD}		-	800	-	DCLK
Horizontal blanking (= T_{HF} + T_{HE})	T_{HBL}		186	256	383	CLK
Hsync front porch	T_{HF}			40	-	CLK
Delay from Hsync to 1st data input (= T_{HW} + T_{HB})	T_{HE}	Function of HDL[5..0] settings	146	216	343	DCLK
Hsync pulse width	T_{HW}		1	128	136	CLK
Hsync back porch	T_{HB}		10	88	342	CLK

b. Vertical Timing

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vsync period (= T_{VD} + T_{VBL})	T_V		497	505	512	Th
Active lines	T_{VD}			480		Th
Vertical blanking (= T_{VF} + T_{VE})	T_{VBL}		17	25	32	Th
Vsync front porch	T_{VF}			1	-	Th
GD start pulse delay	T_{VE}	Function of VDL[3..0] settings	16	24	31	HS
Vsync pulse width	T_{VW}		1	3	16	Th
Hsync/ Vsync phase shift	T_{VPD}		2	320	-	CLK

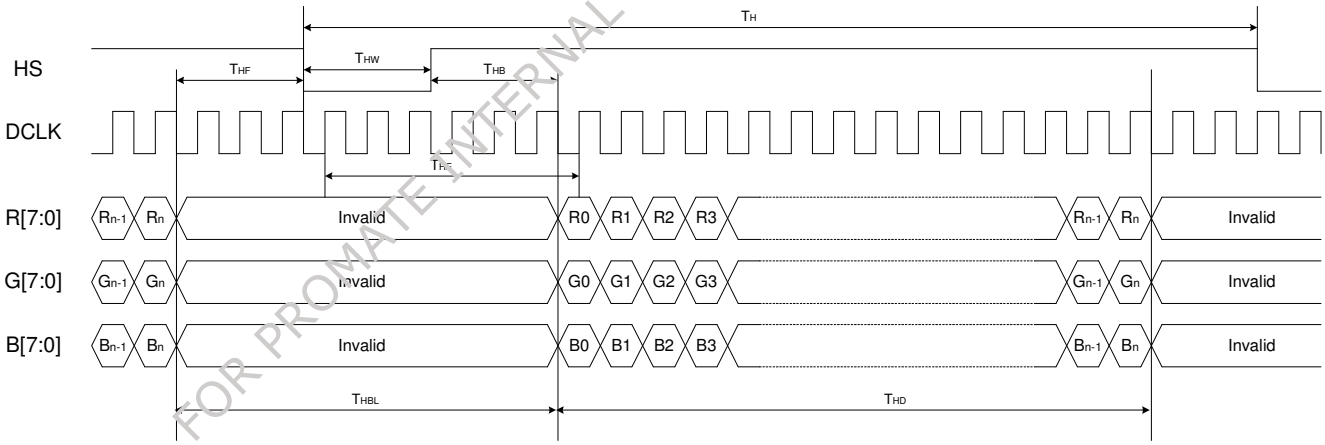


Figure 2 Horizontal input timing. (HV mode)

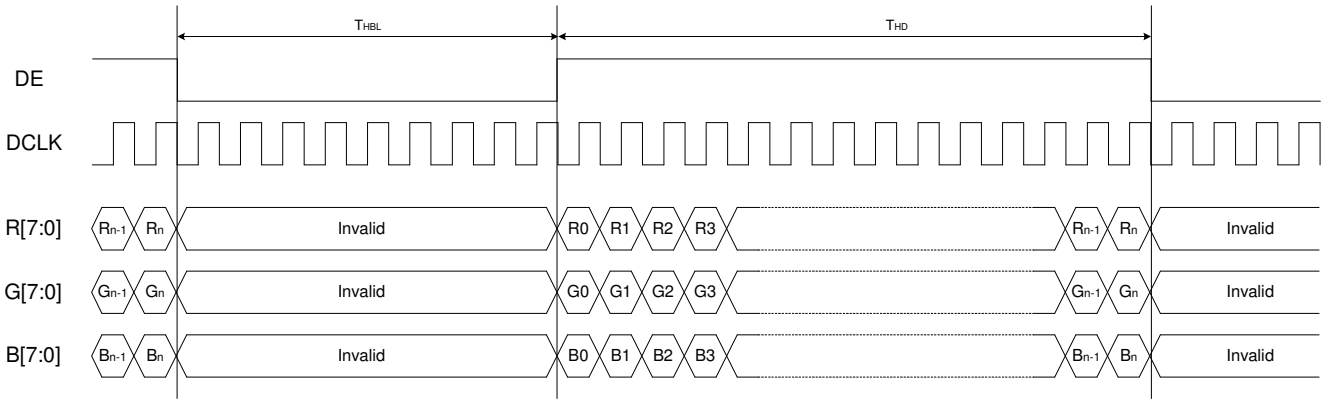


Figure 3: Horizontal input timing. (DE mode)

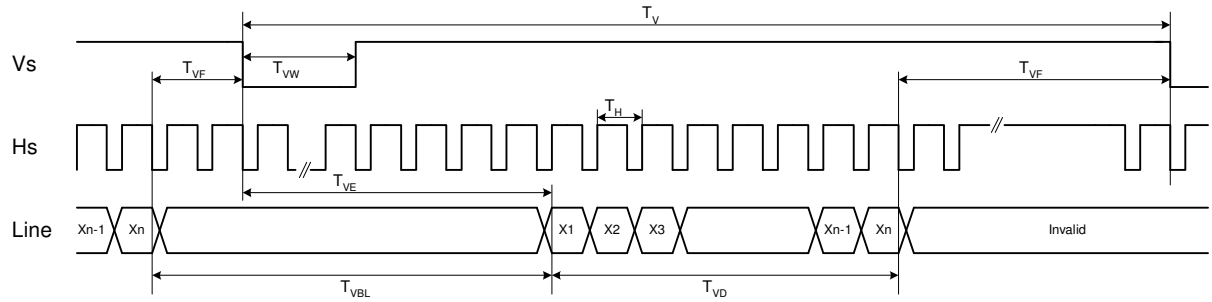


Figure 4: Vertical timing. (HV mode)

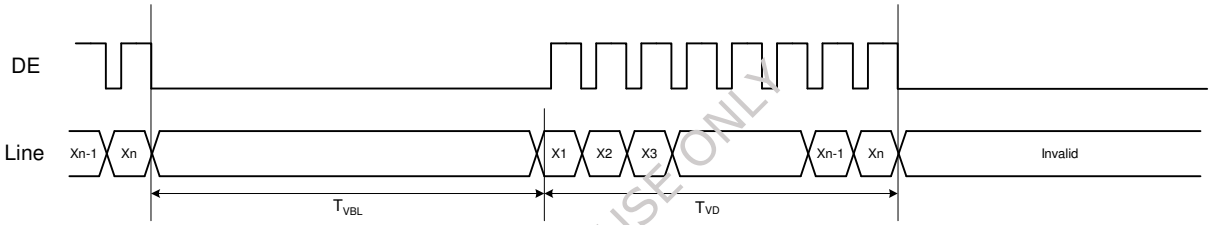


Figure 5: Vertical timing. (DE mode)

5. Serial Control Interface AC Characteristic

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Serial clock	T_{SCK}		320			ns
SCL pulse duty	T_{SCW}		40	50	60	%
Serial data setup time	T_{IST}		120			ns
Serial data hold time	T_{IHD}		120			ns
Serial clock high/low	T_{SSW}		120			ns
CSB setup time	T_{CST}		120			ns
CSB hold time	T_{CHD}		120			ns
Chip select distinguish	T_{CD}		1			us
Delay from CSB to VSYNC	T_{CV}		1			us
Serial data output delay	T_{ID}	CL=20pF	-	-	60	ns

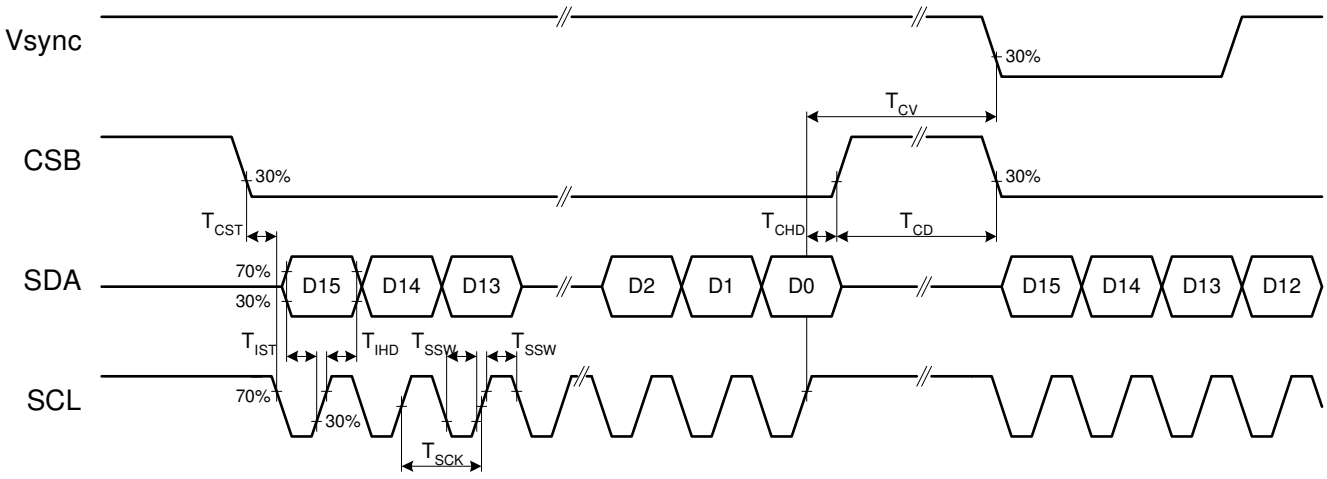


Figure 6 : AC serial interface write mode timing

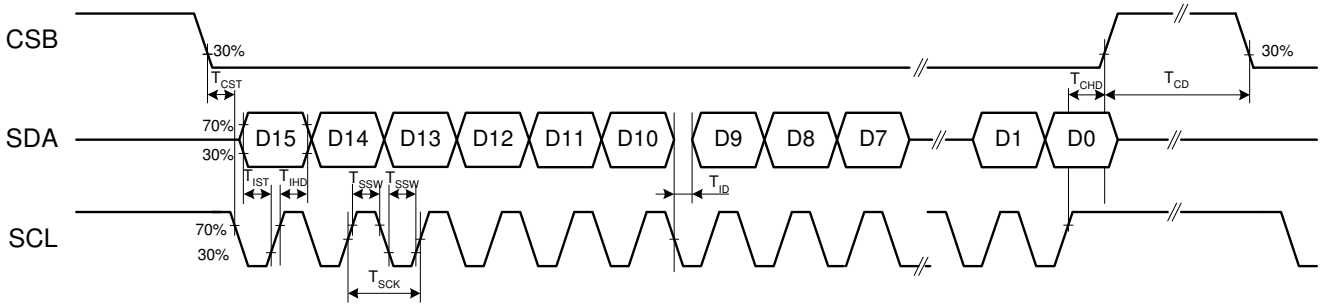


Figure 7 : AC serial interface read mode timing

6. Register Information

There is a total of 6 registers each containing several parameters. For a detailed description of the parameters refer to register table.The serial register has read/write function. D[15:12] are the register address, D[11] defines the read or write mode and D[10:0] are the data.

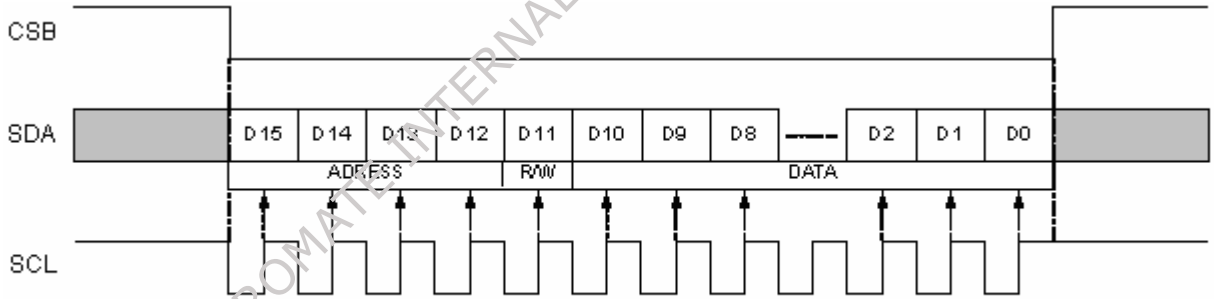


Figure 8: Serial interface write/read sequence

1. At power-on, the default values specified for each parameter are taken.
2. If less than 16-bit data are read during the CS low time period, the data is cancelled.
   a. The write operation is cancelled.
   b. The read operation is interrupt.
3. If more than 16-bit data are read during the CS low time period, the last 16 bits are kept.
   a. Address & R/W are always defined form CSB falling edge.
   b. The write operation load last 11 bit data before CSB rising edge.
   c. The read operation is “D0” is output to SDA until CSB rising edge.
4. All items are set at the falling edge of the vertical sync, except R0[1:0].
5. When GRB is activated through the serial interface, all registers are cleared, except the GRB value.
6. Register R/W setting: D11 = “L” → write mode; D11 = “H” → read mode.
7. The register setting values are valid when VCC already goes to high and after VSYNC starts.
8. It is suggested that VSYNC, HSYNC, DCLK always exists in the same time. But if HSYNC, DCLK stops, only VSYNC operating, the register setting is still valid.
9. If the chip goes to standby mode, the register value will still keep. MCU can wake up the chip only by changing standby mode value from low to high.

10. The register setting values are rewritten by the influence of static electricity, a noise, etc. to unsuitable value, incorrect operating may occur. It is suggested that the SPI interface will setup as frequently as possible.

7. Register Table

Reg	ADDRESS				R/W	DATA										
No.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	R/W	01		01		DITH (1)	U/D (0)	SHL (1)	SHDB1 (1)	0	GRB (1)	STB (1)
R1	0	0	0	1	R/W	X	01		VCOM_M (10)		VCOM_LVL (2Fh)					
R2	0	0	1	0	R/W	X	X	X	HDL							
R3	0	0	1	1	R/W	X	X	X	X							
R6	0	1	1	0	R/W	X	0	EnGB12 (0)	EnGB11 (1)	EnGB10 (0)	0	0	EnGB5 (0)	EnGB4 (1)	EnGB3 (0)	0
R15	1	1	1	1	R/W	X	X	X	X	X	X	X	X	X	1	1

X : Reserved, please set to “0”.

8. Register Description

R0 settings

Address	Bit	Description		Default
0000	[10..0]	Bits 10-9	AUO Internal Use	01
		Bits7-8	AUO Internal Use	01
		Bit6 (DITH)	Dithering function.	
		Bit5 (U/D)	Vertical shift direction selection.	
		Bit4 (SHL)	Horizontal shift direction selection.	
		Bit3 (SHDB1)	AVDD DC-DC converter shutdown setting.	
		Bit2	AUO Internal Use	0
		Bit1 (GRB)	Global reset.	
		Bit0 (STB)	Standby mode setting.	

Bit6	DITH function
0	DITH off.
1	DITH on. **(default)**

Bit5	U/D function
0	Scan down; First line=Gn→ Gn-1 →…→ G2 → Last line=G1. **(default)**
1	Scan up; First line=G1 → G2 → … → Gn-1 → Last line=Gn.

Bit4	SHL function

0	Shift left; First data=Y600 → Y601 → …→ Y2 → Last data=Y1.
1	Shift right: First data=Y1→ Y2 → …→ Y600 → Last data=Y600. **(default)**

Bit3	**SHDB1 function**
0	AVDD DC-DC converter is off.
1	AVDD DC-DC converter is on. **(default)**

Bit1	**GRB function**
0	The controller is reset. Reset all registers to default value.
1	Normal operation. **(default)**

Bit0	**STB function**
0	T-CON, source driver and DC-DC converters are off, and all outputs are High-Z.
1	Normal operation. (**default)**

R1 settings

Address	**Bit**	**Description**		**Default**
0001	[8..0]	Bit9-8	AUO Internal Use	01
		Bit7-6 (VCOM_M)	VCOM mode signal.	
		Bit5-0 (VCOM_LVL)	VCOM level adjustment. Step 31.25mV/LSB @AVDD=12.5V (AVDD/400)	

Bit7-6	**VCOM_M function.**
00	VCOM generator disabled. VCOM is generated externally.
01	VCOM internal reference disabled. DC voltage of VCOM follows VCOMin signal.
1x	VCOM generator enabled. DC voltage of VCOM follows VCOM_LVL settings. (**default**)

NOTE: Please refer to to Figure40.

Bit5-0	**VCOM_LVL function @V1=12.5V**
00h	VCOM_LVL = V1/2–47*31.25mV = 4.78125V
01h	VCOM_LVL = V1/2–46*31.25mV = 4.8125V
2Fh	VCOM_LVL = V1/2 = 6.25V (**default**)
3Eh	VCOM_LVL = V1/2+15*31.25mV = 6.71875V
3Fh	VCOM_LVL = V1/2+16*31.25mV = 6.75V

R2 settings

Address	Bit	Description		Default
0010	[7..0]	Bit7-0 (HDL)	Horizontal start pulse adjustment function	

Bit7-0	HDL function.
00h	$T_{HE} = T_{HEtyp}$ – 128 CLK period.
80h	$T_{HE} = T_{HEtyp}$. **(default)**
FFh	$T_{HE} = T_{HEtyp}$ + 127 CLK period.

R3 settings

Address	Bit	Description		Default
0011	6..0]	Bit6	AUO Internal Use	0
		Bit5	AUO Internal Use	0
		Bit4	AUO Internal Use	0
		Bit3-0 (VDL)	Vertical start pulse adjustment function	

Bit3-0	VDL function.
0000	$T_{VE} = T_{VEtyp}$ – 8 Hs period.
0001	$T_{VE} = T_{VEtyp}$ – 7 Hs period.
0010	$T_{VE} = T_{VEtyp}$ – 6 Hs period.
0011	$T_{VE} = T_{VEtyp}$ – 5 Hs period.
0100	$T_{VE} = T_{VEtyp}$ – 4 Hs period.
0101	$T_{VE} = T_{VEtyp}$ – 3 Hs period.
0110	$T_{VE} = T_{VEtyp}$ – 2 Hs period.
0111	$T_{VE} = T_{VEtyp}$ – 1 Hs period.
1000	$T_{VE} = T_{VEtyp}$. **(default)**
1001	$T_{VE} = T_{VEtyp}$ + 1 Hs period.
1010	$T_{VE} = T_{VEtyp}$ + 2 Hs period.
1011	$T_{VE} = T_{VEtyp}$ + 3 Hs period.
1100	$T_{VE} = T_{VEtyp}$ + 4 Hs period.
1101	$T_{VE} = T_{VEtyp}$ + 5 Hs period.
1110	$T_{VE} = T_{VEtyp}$ + 6 Hs period.
1111	$T_{VE} = T_{VEtyp}$ + 7 Hs period.

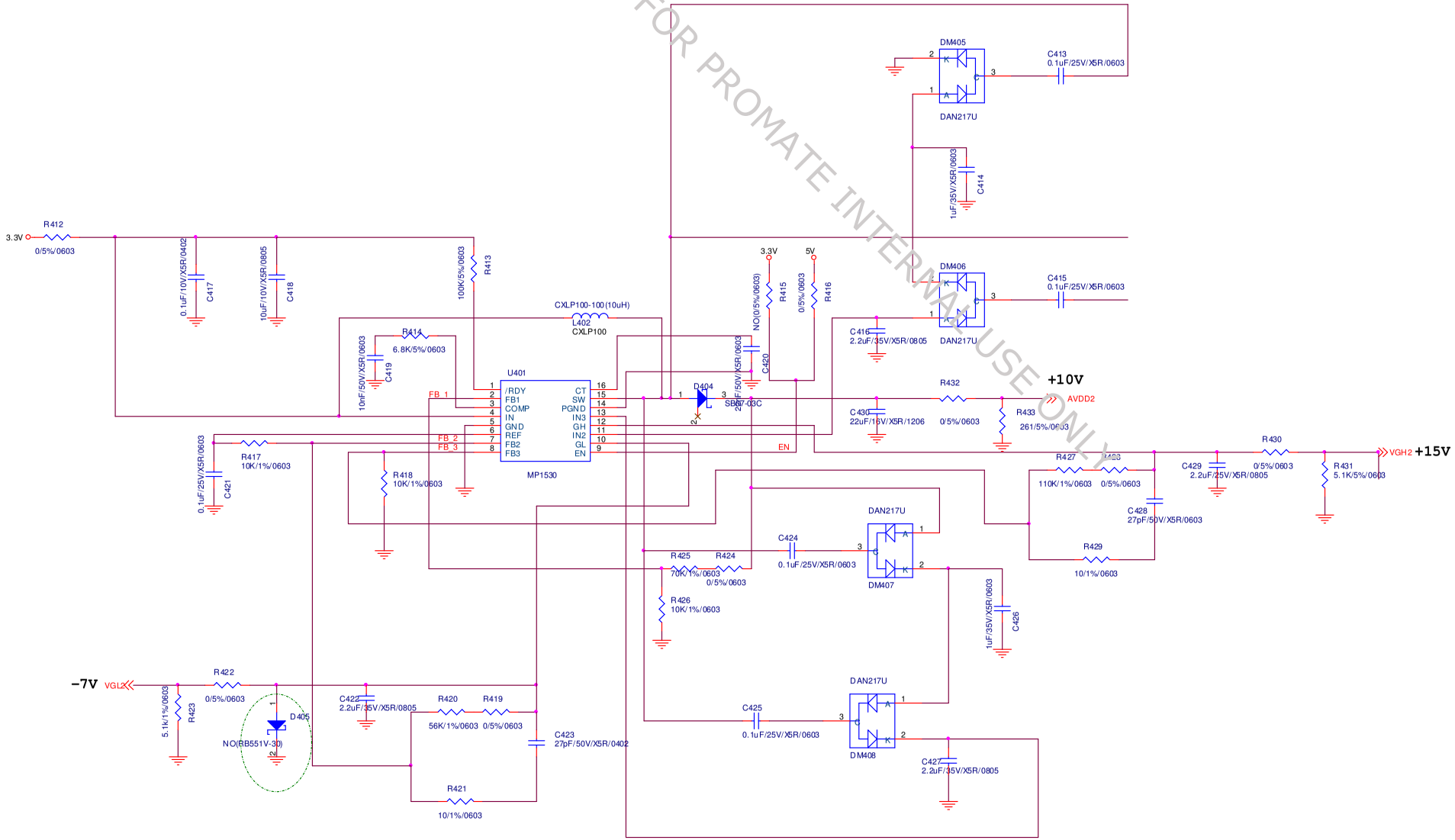
R6 settings

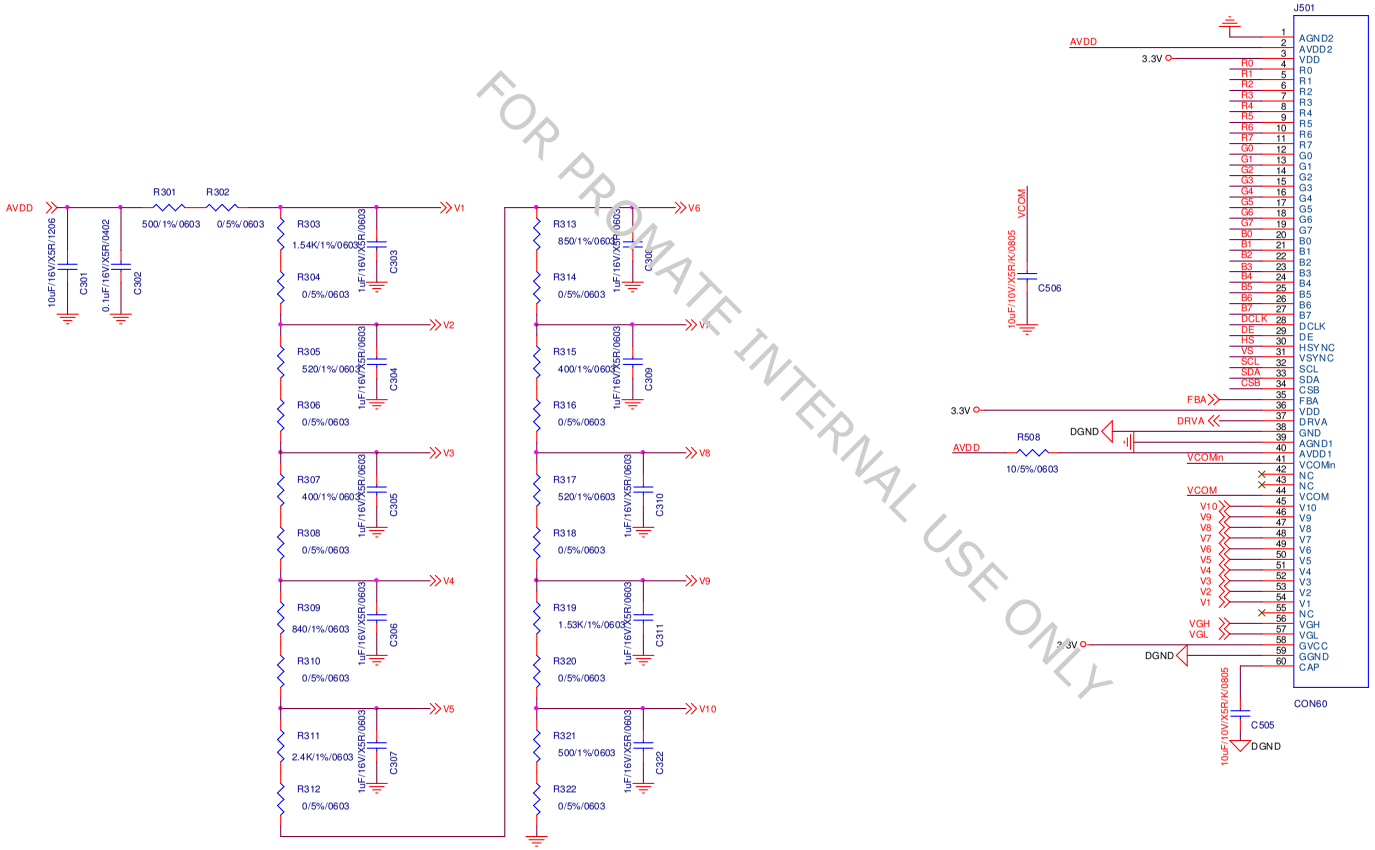
Address	Bit	Description		Default
0110	[9..0]	Bit9	AUO Internal Use	0

		Bit8(EnGB12)	Gamma buffer Enable for V12	
		Bit7(EnGB11)	Gamma buffer Enable for V11	
		Bit6(EnGB10)	Gamma buffer Enable for V10	
		Bit5	AUO Internal Use	0
		Bit4	AUO Internal Use	0
		Bit3(EnGB5)	Gamma buffer Enable for V5	
		Bit2(EnGB4)	Gamma buffer Enable for V4	
		Bit1(EnGB3)	Gamma buffer Enable for V3	
		Bit0	AUO Internal Use	0

Bitx	**EnGBx function**
0	Gamma buffer for VX is disable (High Z).
1	Gamma buffer is enable. VX must be connected externally.

9. Suggested Application Circuit

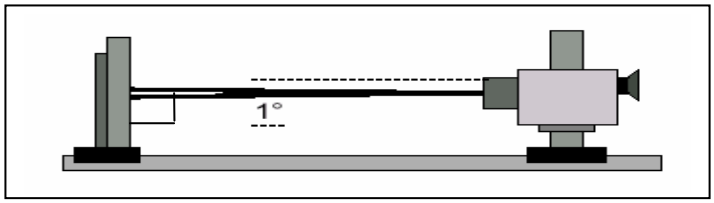




G. Optical specification

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time							
Rise	Tr	θ=0°	-	12	20	ms	Note 3
Fall	Tf		-	18	30	ms	
Contrast ratio	CR	At optimized viewing angle	200	400	-		Note 4
Viewing Angle							
Top			30	40	-		
Bottom		CR≧10	50	60	-	deg.	Note 5
Left			50	60	-		
Right			50	60	-		
Brightness	Y_L	θ=0°	150	200	-	cd/m^2	Note 6
White Chromaticity	X	θ=0°	0.25	0.30	0.35		
	y	θ=0°	0.27	0.32	0.37		

Note 1:Ambient temperature =25℃ and LED lightbar voltage V_L = 12 V. To be measured in the dark room.

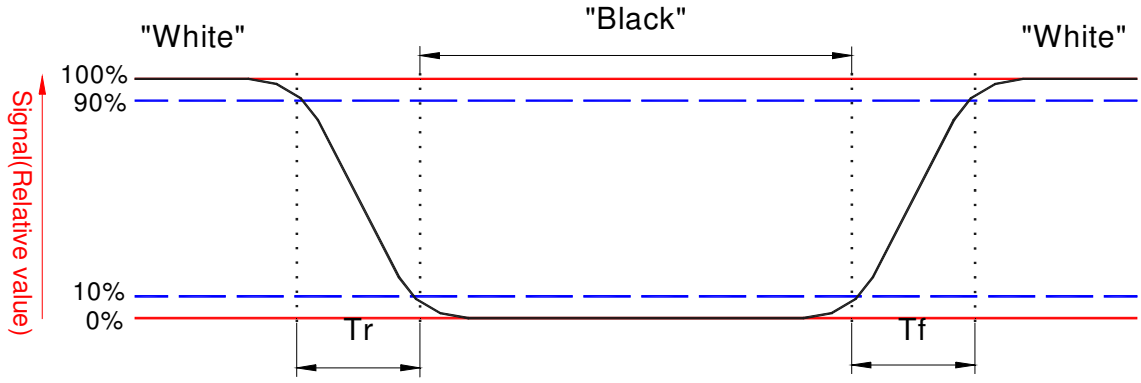


Note 2:To be measured on the center area of panel with a viewing cone of 1° by Topcon luminance meter BM-7, after 15 minutes operation.

Note 3. Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.

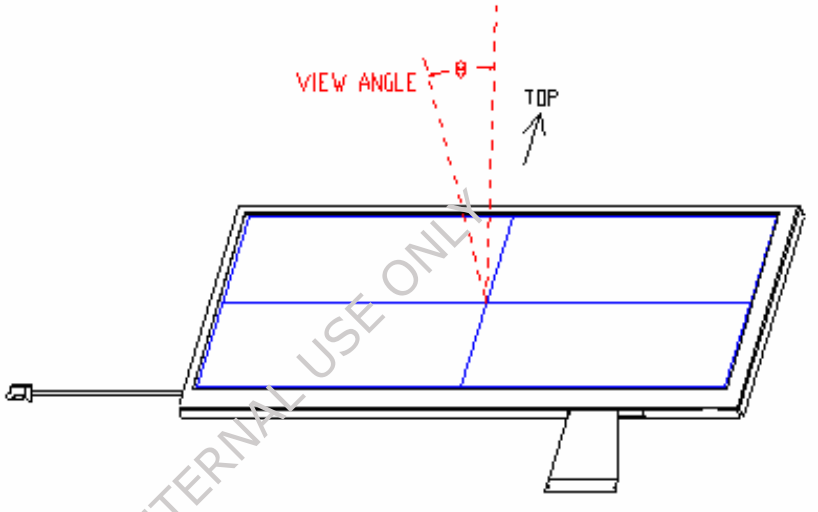


Note 4.Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

Note 5. Definition of viewing angle, θ, Refer to figure as below.



Note 6. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

H. Absolute Ratings of Ambient Environment

No.	Test items	Conditions	Remark
1	High Temperature Storage	Ta= 70□ 240Hrs	
2	Low Temperature Storage	Ta= -10□ 240Hrs	
3	High Ttemperature Operation	Ta= 60□ 240Hrs	
4	Low Temperature Operation	Ta= 0□ 240Hrs	
5	High Temperature & High Humidity	Ta= 50□. 80% RH 240Hrs	Operation
6	Heat Shock	-10□~60□, 50 cycle, 2Hrs/cycle	Non-operation
7	Electrostatic Discharge	±200V,200pF(0Ω), once for each terminal	Non-operation
8	Vibration	Frequency range : 8~33.3Hz Stoke : 1.3mm Sweep :2.9G ,33.3~400Hz 2 hours for each direction of X,Y,Z 4 hours for Y direction	Non-operation JIS C7021, A-10 condition A : 15 minutes
9	Mechanical Shock	100G . 6ms, ±X,±Y,±Z 3 times for each direction	Non-operation JIS C7021, A-7 condition C
10	Vibration (With Carton)	Random vibration: 0.015G^2/Hz from 5~200Hz –6dB/Octave from 200~500Hz	IEC 68-34
11	Drop (With Carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	

Note 1: Ta: Ambient Temperature.

Note 2: Note 2: In the standard conditions, there is not display function NG issue occurred. All the cosmetic specification is judged before the reliability stress.

I. Packing Form