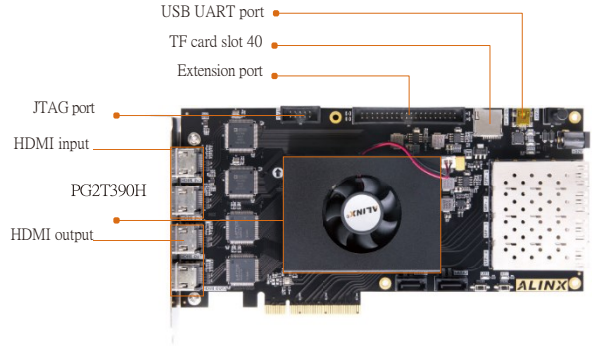
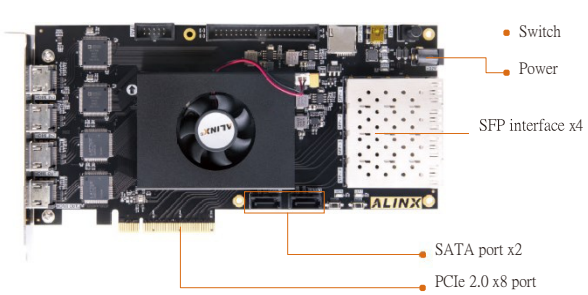
AXP391

Pango Micro Titan-2 FPGA Platform Development Platform

Product parameters

- Based on PG2T390H -6IFFBG900 FPGA
- 2GB DDR3, 64bit; 8GB DDR4, 64bit; 64MB QSPI FLASH
- x4y SFP optical fiber interface, up to 10Gbps
- PCIe 2.0 x8, single channel up to 5Gbps
- x2 HDMI video input interface
- x2 HDMI output interface
- Integrated SATA, USB Common interfaces such as UART, JTAG, 40 -pin expansion port, and TF card
- High-end customized cooling fan
- Provide core board schematic diagram, bottom board schematic diagram, bottom board PCB, chip datasheet Provides rich Demo source code and supporting tutorials, making it easier to get started



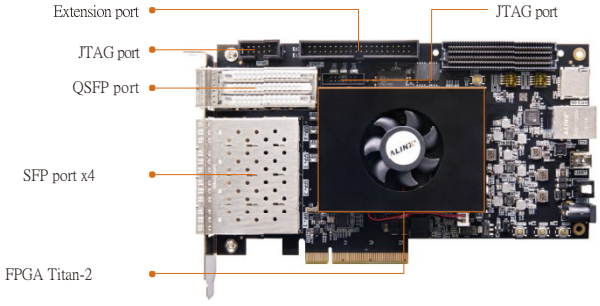


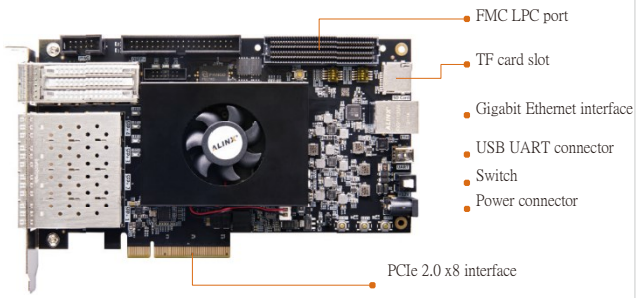
AXP390

Titan-2 Platform Development Platform

Product parameters

- Based on PG2T390H-6IFFBG900 FPGA
- 8GB DDR4 64bit; 2GB DDR3 64bit
- 64MB QSPI FLASH
- x1 QSFP fiber optic interface, speed up to 40Gb/s
- x4 SFP optical fiber interface, each channel connection supports up to 10Gb/s
- 1 standard FMC LPC extension port, compatible with ALINX FMC boards
- 1 PCIe 2.0 x8 interface, single-channel communication rate up to 5Gbps
- Integrated Gigabit Ethernet, UART, TF card slot, JTAG and other common interfaces
- Provide core board schematic diagram, bottom board schematic diagram, bottom board PCB Provides rich Demo source code and supporting tutorials, making it easier to get started





Logos-2 development platform

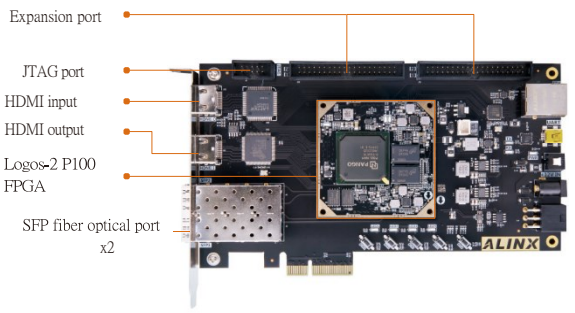
Logos- 2	Part number	PG2L25H	PG2L50H	PG2L100H	PG2L200H
Logical resources	Equivalent LUT4	26700	53700	99900	190080
	Flip-Flops (units)	35600	71600	133200	2816000
RAM	Distributed RAM (Kbit)	377	742	1274	2816
	Block RAM (36Kbit/block)	55	85	155	400
	Block RAM(Kbit)	1980	3060	5580	14400
Clock resource	GPLL + PPLL	3 +3	5 + 5	6 + 6	10 + 10
I/O resources	Maximum User I/O	150	250	300	500
	Maximum differential I/O	72	120	144	240
	DDR3 (Mbps)	1066	1066	1066	1066
Hardcore resources	APM (18*25)	40	120	240	800
	ADC core	1	1	1	1
	PCIe Gen2x4	1	1	1	1
	AES module	1	1	1	1
	HSST (6.6Gbps)	4	4	8	16

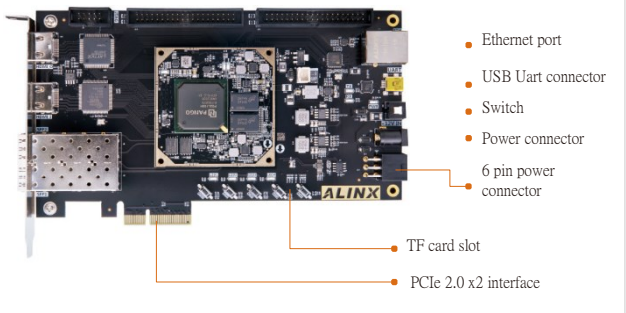
AXP100

Logos-2 FPGA development platform

Product parameters

- Based on PG2L100H -6IFBG676 FPGA
- 1GB DDR3, 32bit; 64MB QSPI FLASH
- x2 SFP Optical fiber interface, up to 6.6Gbps
- PCIe 2.0 x2, single channel up to 5Gbps
- 1 channel 10 / 100 / 1000M Ethernet, EEPROM 24LC04
- HDMI input & output interface, support 1080P@60Hz
- Integrated USB UART, JTAG, 40 -pin expansion port, TF card slot and other common interfaces
- Provide core board schematic diagram, bottom board schematic diagram, bottom board PCB
- Provides rich Demo source code and supporting tutorials, making it easier to get started



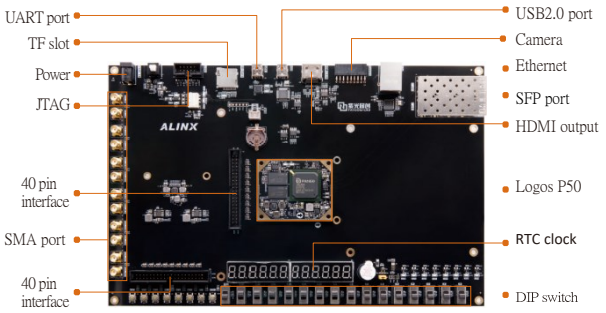


AXP50

Logos experiment kit

Product parameters

- Based on PGL50H-6IFBG484 FPGA
- 1GB DDR3, 32bit; 16MB QSPI FLASH
- AXP50 open board 1 block
- AN831, AN5640, AN9767, AN9238, AN970 modules
- x1 CMOS camera interface, connected to the camera module
- x2 SFP optical fiber interface, x1 Gigabit Ethernet interface
- x1 USB interface, x1 UART interface, x1 HDMI output interface
- x1 40 Pin expansion port, external Companion module port
- integrated TF card slot, JTAG, LEDs, DIP switch, SMA and other interfaces

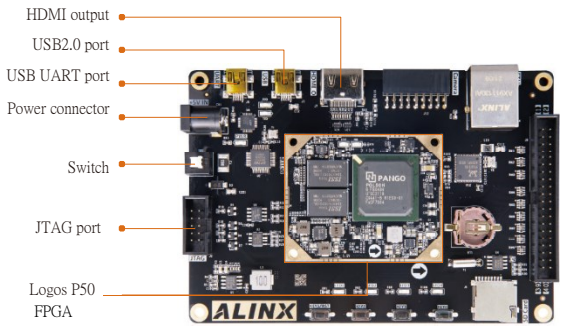


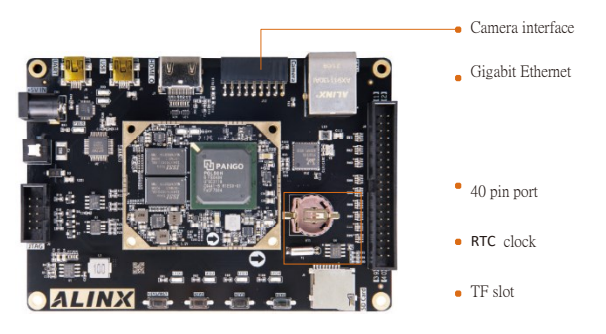
AXPGL50H

Logos FPGA development platform

Product parameters

- Based on PGL50H-6IFBG484 FPGA
- 1GB DDR3, 32bit; 16MB QSPI FLASH
- 1 piece of I2C interface EEPROM 24LC04
- 1CH 10 / 100 / 1000M Ethernet
- x1 CMOS camera interface, order camera module
- x1 USB Uart interface, used for communicate & debugging
- x1 40 Pin expansion port, external Companion module port
  Integrated HDMI, USB, TF card slot, JTAG and other common interface
- Provide core board schematic diagram, bottom board schematic diagram, bottom board PCB
  Provides rich Demo source code and supporting tutorials, making it easier to get started



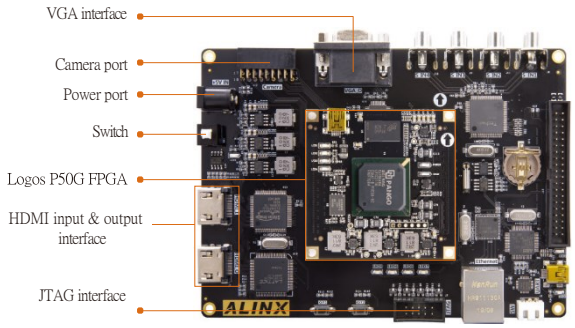


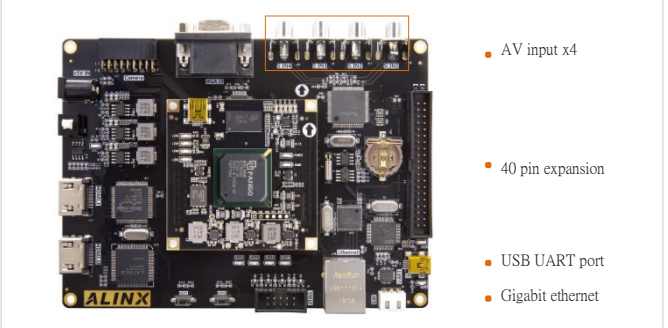
AVP50G

Logos video image development board

Product parameters

- Based on PGL50G-6IFBG484 FPGA
- 256MB DDR3, 16bit
- 8MB QSPI Flash
- 1CH 10 / 100 / 1000M Ethernet
- 1 ch CMOS camera interface, connected to OV5640 camera
- x1 HDMI input and output, x1 VGA output
- x4 AV inputs
- Integrated USB UART, JTAG, 40 -pin expansion port and other common interfaces
- Provide core board schematic diagram, bottom board schematic diagram, bottom board PCB, Provides rich Demo source code and supporting tutorials, making it easier to get started



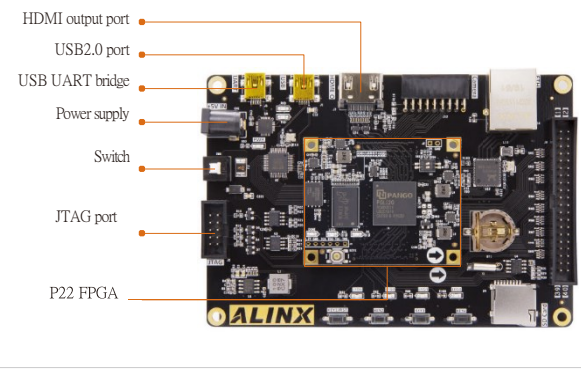


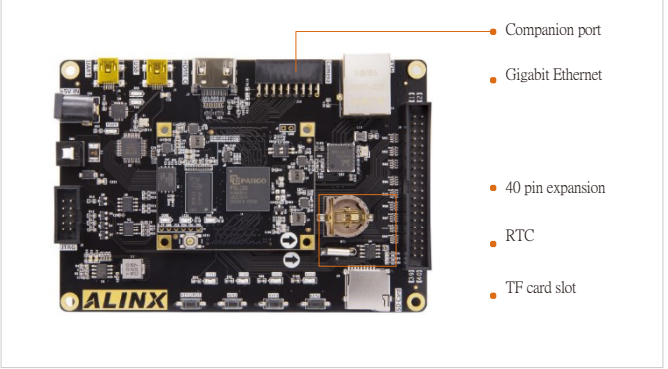
PGL22G

Logos FPGA development platform

Product parameters

- Based on PGL22G-6CMBG324 FPGA
- 256MB DDR3, 16bit; 16MB QSPI FLASH
- x1 I2C EEPROM 24LC04
- 1CH 10 / 100 / 1000M Ethernet
- x1 CMOS camera interface, order camera module
- x1 USB-UART interface, used for communication & debugging
- x1 40 Pin expansion port, Companion module interface
- Integrated HDMI, USB, TF card slot, JTAG and other common interface
- Provide core board schematic diagram, bottom board schematic diagram, bottom board PCB, Provide rich Demo source code and supporting tutorials, making it easier to get started



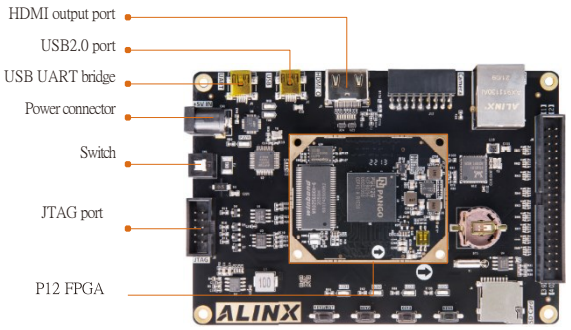


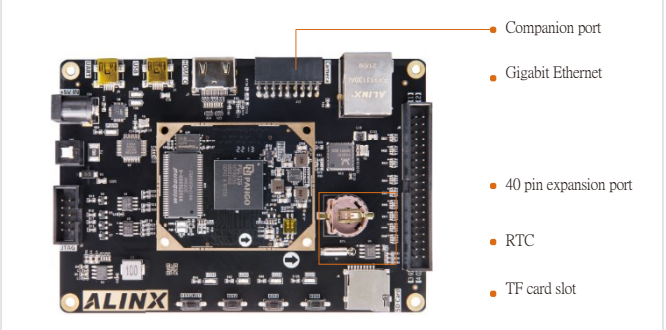
AXP12

Logos FPGA development platform

Product parameters

- Based on PGL12G-6CFBG256 FPGA
- 256Mbit SDRAM, 16bit; 64Mbit QSPI FLASH
- x1 I2C EEPROM 24LC04
- 1CH 10 / 100 / 1000M Ethernet
- x1 CMOS camera interface, order camera module
- x1 USB-UART interface, used for communication & debugging
- x1 40 Pin expansion port, external Companion module
- Integrated HDMI, USB, TF card slot, JTAG and other common interface
- Provide core board schematic diagram, base board schematic diagram, bottom board PCB, Provides rich Demo source code and supporting tutorials, making it easier to get started



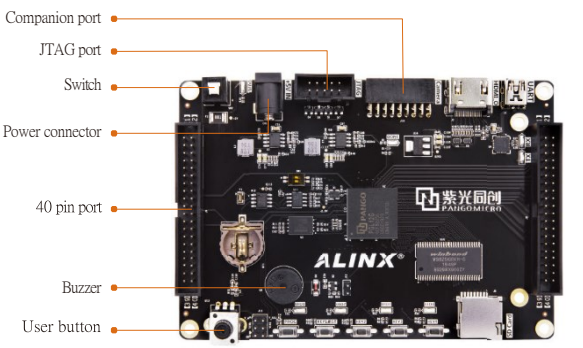


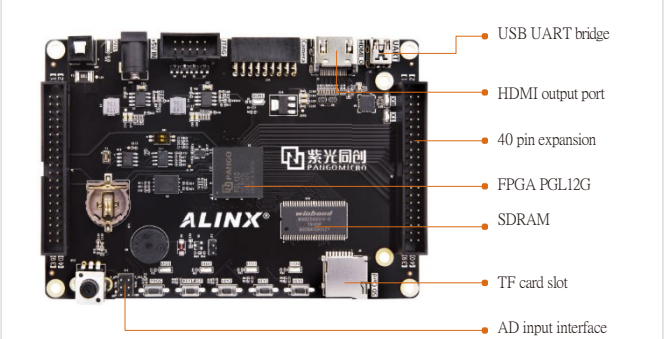
PGL12G

Logos FPGA development platform

Product parameters

- Based on PGL12G-6CFBG256 FPGA
- 256Mbit SDRAM, 16bit; 64Mbit QSPI FLASH
- x1 CMOS camera interface, order camera module
- x1 USB-Uart interface, for communication & debug
- x2 40 Pin expansion port, external Companion module
- 1 HDMI output interface, integrated TF Card slot, JTAG so often interface
- Provide core board schematic diagram, bottom board schematic diagram, bottom board PCB, chip datasheet
- Provides rich Demo source code and supporting tutorials, making it easier to get started



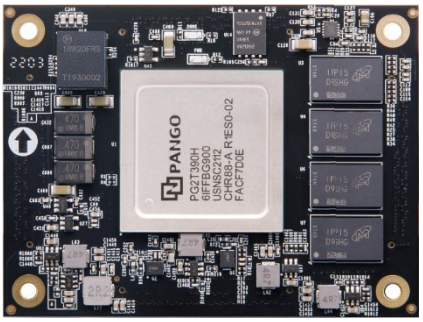


Pango Micro FPGA based coreboards selection table

Core board model	P12	P22	P50G	P50	P100	P390
FPGA series	Logos				Logos- 2	Titan- 2
FPGA chip	PGL12G-6CFBG256	PGL22G - 6CMBG324	PGL50G - 6IFBG484	PGL50H - 6IFBG484	PG2L100H - 6IFBG676	PG2T390H - 6IFFBG900
Grade	Commercial grade, 0℃~70℃		Industrial grade, - 40℃~85℃		Industrial grade, - 40℃~85℃	
Memory	256Mbit SDRAM 16bit	256MB DDR3 16bit	256MB DDR3 16bit	1GB DDR3 32bit	1GB DDR3 32bit	2GB DDR3, 64bit 8GB DDR4, 64bit
QSPI Flash	64Mbit	16MB	8MB	16MB	32MB	64MB
Equivalent LUT4	12480	21,043	51,360	51,360	99,900	365400
Flip-Flops (units)	15600	26,304	64,200	64,200	133,200	487200
Distributed RAM(Kbit)	85	70	544	544	1274	4712
Amount of block RAM	30 (18Kbit)	48 (18Kbit)	134 (18Kbit)	134 (18Kbit)	155 (36Kbit)	480 (36Kbit)
Block RAM(Kbit)	540	864	2412	2412	5,580	17280
PLLs / GPLL+PPLL	4	6	5	5	6+6	10+10
Expand IO	106	108	168	195	190	276
Differential pair	51	52	84	55	88	130
PCI- Express	—	—	—	PCIe 2.0	PCIe 2.0	PCIe 3.0
APM	20 (18*18)	30 (18*18)	84(18*18)	84(18*18)	240 (18*25)	840 (18*25)
HSST	—	—	—	4 * 6.375Gbps	8 * 6.6 Gbps	8x 13.125Gbps
ADC hard core	1	1	—	—	1	1
AES module	1	1	1	1	1	1
Connector	80pin x2		100pin x2	80pin x4	80pin x4	120pin x4
Size	55x45mm		60x60mm	55x45mm	60x60mm	80x60mm

P390 | PG2T390H

- PG2T390H-6IFFBG900
- 2GB DDR3, 64bit
- 8GB DDR4, 64bit
- 64MB QSPI FLASH
- LUT6s 243600
- Eq LUT4s 365,400
- Flip-Flops 487200
- Distr RAM 4712Kbit
- Block RAM 17280Kbit
- GPLLs 10 + PPLLs 10
- APMs 840 (18*25)
- PCIE 3.0, 8x 13.125Gbps HSST
- 276 expand I/O, 96 v/a IO
- 130 diff pairs
- Working temp -40˚C to 85˚C
- Dimension 80x60mm

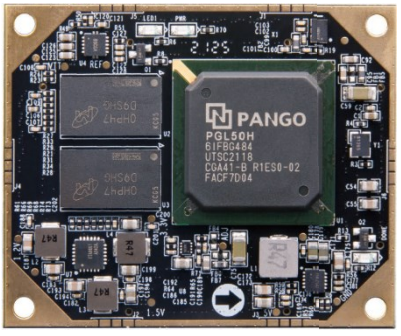


P100 | PG2L100H

- PG2L100H-6IFBG676
- 1GB DDR3, 32bit
- 32MB QSPI FLASH
- LUT6s 66600
- Eq LUT4 99,900
- Flip-Flops 133,200
- Distr RAM 1274Kbit
- Block RAM 5580Kbit
- GPLLs 6 + PPLLs 6
- APMs 240 (18*25)
- 8x 6.6Gbps HSST
- 190 user I/O, 100 v/a IO
- 88 diff pairs
- Speed grade 6, I
- Working temp -40˚C to 85˚C
- Dimension 60x60mm

P50 | PGL50H

- PGL50H-6IFBG484
- 1GB DDR3, 32bit
- 16MB QSPI FLASH
- LUT5s 42800
- Eq LUT4 51,360
- Flip-Flops 64,200
- Distr RAM 544Kbit
- Block RAM 2412Kbit
- PLLs 5, APMs 84 (18*18)
- Supports PCIE 2.0
- 4x 6.375Gbps HSST
- 195 user I/O, 113 V/A IO
- 55 diff pairs
- Speed grade 6, I
- Working temp -40˚C to 85˚C
- Dimension 55x45mm

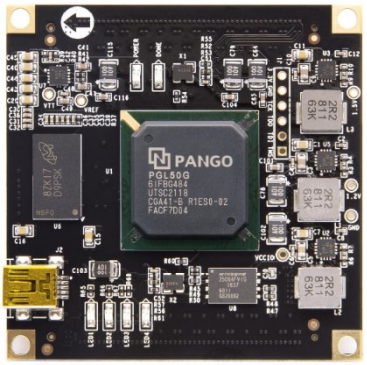


FPGA Core boards

P50G | PGL50G

- PGL50G-6IFBG484
- 256MB DDR3, 16bit
- 8MB QSPI FLASH
- LUT5s 42800
- Eq LUT4 51,360
- Flip-Flops 64,200
- Distr RAM 544Kbit

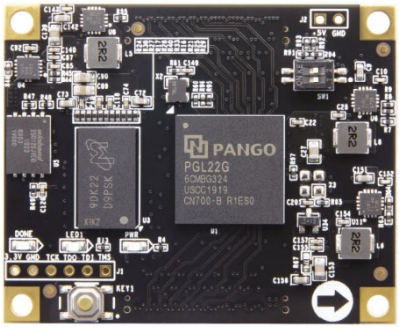
- PLLs 5, APMs 84 (18*18)
- 168 User I/O, 168 V/A IO
- 84 diff pairs
- Speed grade 6, I
- Working temp -40°C to 85°C
- Dimension 60x60mm



P22 | PGL22G

- PGL22G-6CMBG324
- 256MB DDR3, 16bit
- 16MB QSPI FLASH
- LUT5s 17536
- Eq LUT4 21043
- Flip-Flops 26304
- Distr RAM 70Kbit
- Block RAM 864Kbit

- PLLs 6
- APMs 30 (18*18)
- 108 User I/O
- 40 V/A IO
- 52 diff pair
- Speed grade 6,
- Work temp 0°C to 70°C
- Dimension 55x45mm



P12 | PGL12G

- PGL12G-6CFBG256
- 256Mbit SDRAM, 16bit
- 64Mbit QSPI FLASH
- LUT5s 10400
- Eq LUT4 12480
- Flip-Flops 15600
- Distr RAM 85Kbit
- Block RAM 540Kbit

- PLLs 4
- APMs 20(18*18)
- 106 User I/O
- 40 V/A IO
- 51diff pair
- Speed grade 6,
- Work temp 0°C to 70°C
- Dimension 55x45mm