MX25LM51245G

3V 512M-BIT [x 1/x 8]
CMOS MXSMIO® (SERIAL MULTI I/O)
FLASH MEMORY

Key Features

- *Protocol Support - Single I/O and Octa I/O*
- *Support DTR (Double Transfer Rate) Mode*
- *Support clock frequency up to 133MHz*

Contents

3V 512M-BIT [x 1/x 8] CMOS MXSMIO® (SERIAL MULTI I/O) FLASH MEMORY

1. FEATURES

GENERAL

- Supports Serial Peripheral Interface -- Mode 0
- Single Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
- 512Mb: 536,870,912 x 1 bit structure or 67,108,846 x 8 bits (Octa I/O mode) structure
- Protocol Support
  - Single I/O and Octa I/O
  - Support DTR (Double Transfer Rate) Mode
- Fast frequency support
  - Support clock frequency up to
    - Single I/O mode: 133MHz
    - Octa I/O mode: 133MHz
  - Configurable dummy cycle number for OPI read operation
- Octa Peripheral Interface (OPI) available
- Equal Sectors with 4K byte each, or Equal Blocks with 64K byte each
  - Any Block can be erased individually
- Programming :
  - 256byte page buffer
  - Octa Input/Output page program to enhance program performance
- Typical 100,000 erase/program cycles
- 20 years data retention

SOFTWARE FEATURES

- Input Data Format
  - SPI: 1-byte command code
  - OPI: 2-byte command code
- Advanced Security Features
  - Block lock protection

  The BP0-BP3 and T/B status bits define the size of the area to be protected against program and erase instructions
  - Individual Sector Protection (Solid Protect)
- Additional 8K bit security OTP
  - Features unique identifier
  - Factory locked identifiable, and customer lockable
- Command Reset
- Program/Erase Suspend and Resume operation
- Electronic Identification
  - JEDEC 1-byte manufacturer ID and 2-byte device ID
- Support Serial Flash Discoverable Parameters (SFDP) mode

HARDWARE FEATURES

- SCLK Input
  - Serial clock input
- SIO0 - SIO7
  - Serial Data Input or Serial Data Output
- DQS
  - Data strobe signal
- RESET#
  - Hardware Reset pin
- PACKAGE
  - 24-Ball BGA (5x5 ball array)
  - 16-Pin SOP
  - **All devices are RoHS Compliant and Halogen Free.**

2. GENERAL DESCRIPTION

MX25LM51245G is 512Mb bits Serial NOR Flash memory, which is configured as 67,108,864 x 8 internally. MX25LM51245G feature a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus while it is in single I/O mode. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

The MX25LM51245G MXSMIO® (Serial Multi I/O) provides sequential read operation on whole chip.

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis, or word basis. Erase command is executed on sector (4K-byte), or block (64K-byte), or whole chip basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

When the device is not in operation and CS# is high, it is put in standby mode.

The MX25LM51245G utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

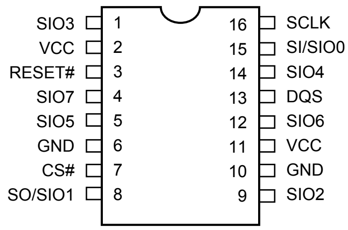
Table 1. Operating Frequency Comparison

	Numbers of Dummy Cycle							
	6	8	10	12	14	16	18	20
Octa I/O STR (MHz)	66	84	104	104	133	133	133	133*
Octa I/O DTR (MHz)	66	84	104	104	133	133	133	133*

Notes: * means default status

3. PIN CONFIGURATIONS

16-PIN SOP (300mil)



24-BALL BGA (5x5 ball array)

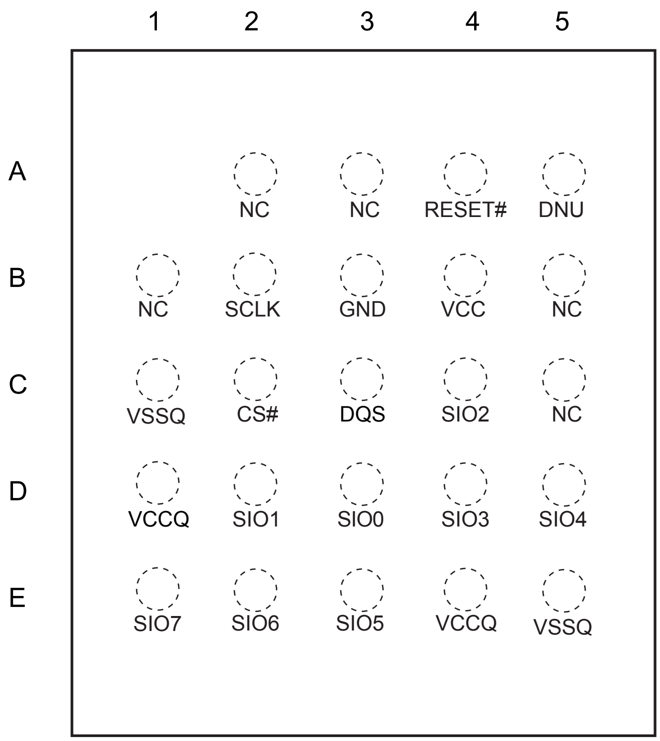
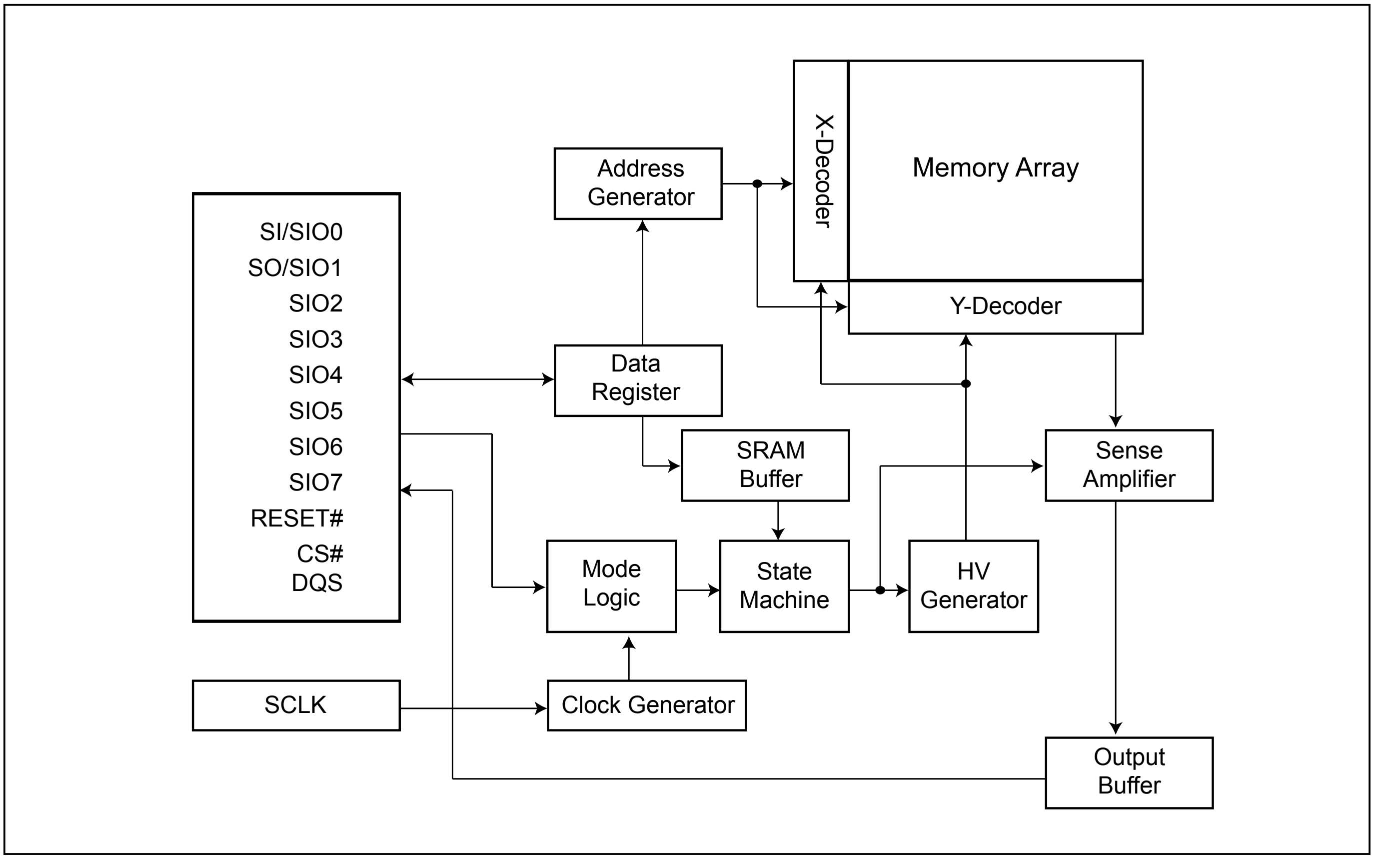


Table 2. PIN DESCRIPTION

SYMBOL	DESCRIPTION
CS#	Chip Select
SCLK	Clock Input
RESET#	Hardware Reset Pin Active low[Note 1]
DQS	Data Strobe Signal
SI/SIO0	Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for 8 x I/O read mode)
SO/SIO1	Serial Data Output (for 1 x I/O)/ Serial Data Input & Output (for 8 x I/O read mode)
SIO2-SIO7	Serial Data Input & Output (for 8 x I/O read mode)
VCC	3V Power Supply
VCCQ	3V Buffer Power Supply
GND	Ground
VSSQ	IO Ground Supply
DNU	Do not use
NC	No Connection

Notes:
1. RESET# pin has internal pull up.

4. BLOCK DIAGRAM



5. MEMORY ORGANIZATION

Block(64K-byte)	Sector	Address Range	
1023	16383	3FFF000h	3FFFFFFh
	⋮	⋮	⋮
	16376	3FF8000h	3FF8FFFh
	16375	3FF7000h	3FF7FFFh
	⋮	⋮	⋮
	16368	3FF0000h	3FF0FFFh
1022	16367	3FEF000h	3FEFFFFh
	⋮	⋮	⋮
	16360	3FE8000h	3FE8FFFh
	16359	3FE7000h	3FE7FFFh
	⋮	⋮	⋮
	16352	3FE0000h	3FE0FFFh
1021	16351	3FDF000h	3FDFFFFh
	⋮	⋮	⋮
	16344	3FD8000h	3FD8FFFh
	16343	3FD7000h	3FD7FFFh
	⋮	⋮	⋮
	16336	3FD0000h	3FD0FFFh
2	47	002F000h	002FFFFh
	⋮	⋮	⋮
	40	0028000h	0028FFFh
	39	027000h	0027FFFh
	⋮	⋮	⋮
	32	0020000h	0020FFFh
1	31	001F000h	001FFFFh
	⋮	⋮	⋮
	24	0018000h	0018FFFh
	23	0017000h	0017FFFh
	⋮	⋮	⋮
	16	0010000h	0010FFFh
0	15	000F000h	000FFFFh
	⋮	⋮	⋮
	8	0008000h	0008FFFh
	7	0007000h	0007FFFh
	⋮	⋮	⋮
	0	0000000h	0000FFFh

6. DATA PROTECTION

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.

- Valid command length (SPI Mode) or command/command# combination (OPI Mode) will be check.
- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before other command to change data.
- Deep Power Down Mode: By entering deep power down mode, the flash device also is under protected from writing all commands except Release from deep power down mode command (RDP), and softreset command.

6-1. Block lock protection

- The Software Protected Mode (SPM) use (BP3, BP2, BP1, BP0 and T/B) bits to allow part of memory to be protected as read only. The protected area definition is shown as *Table 3* Protected Area Sizes, the protected areas are more flexible which may protect various area by setting value of BP0-BP3 bits.

Table 3. Protected Area Sizes

Protected Area Sizes (T/B bit = 0)

Status bit				Protect Level
BP3	BP2	BP1	BP0	512Mb
0	0	0	0	0 (none)
0	0	0	1	1 (1 block, protected block 1023rd)
0	0	1	0	2 (2 blocks, protected block 1022nd~1023rd)
0	0	1	1	3 (4 blocks, protected block 1020th~1023rd)
0	1	0	0	4 (8 blocks, protected block 1016th~1023rd)
0	1	0	1	5 (16 blocks, protected block 1008th~1023rd)
0	1	1	0	6 (32 blocks, protected block 992nd~1023rd)
0	1	1	1	7 (64 blocks, protected block 960th~1023rd)
1	0	0	0	8 (128 blocks, protected block 896th~1023rd)
1	0	0	1	9 (256 blocks, protected block 768th~1023rd)
1	0	1	0	10 (512 blocks, protected block 512th~1023rd)
1	0	1	1	11 (1024 blocks, protected all)
1	1	0	0	12 (1024 blocks, protected all)
1	1	0	1	13 (1024 blocks, protected all)
1	1	1	0	14 (1024 blocks, protected all)
1	1	1	1	15 (1024 blocks, protected all)

Protected Area Sizes (T/B bit = 1)

Status bit				Protect Level
BP3	BP2	BP1	BP0	512Mb
0	0	0	0	0 (none)
0	0	0	1	1 (1 block, protected block 0th)
0	0	1	0	2 (2 blocks, protected block 0th~1st)
0	0	1	1	3 (4 blocks, protected block 0th~3rd)
0	1	0	0	4 (8 blocks, protected block 0th~7th)
0	1	0	1	5 (16 blocks, protected block 0th~15th)
0	1	1	0	6 (32 blocks, protected block 0th~31st)
0	1	1	1	7 (64 blocks, protected block 0th~63rd)
1	0	0	0	8 (128 blocks, protected block 0th~127th)
1	0	0	1	9 (256 blocks, protected block 0th~255th)
1	0	1	0	10 (512 blocks, protected block 0th~511th)
1	0	1	1	11 (1024 blocks, protected all)
1	1	0	0	12 (1024 blocks, protected all)
1	1	0	1	13 (1024 blocks, protected all)
1	1	1	0	14 (1024 blocks, protected all)
1	1	1	1	15 (1024 blocks, protected all)

6-2. Additional 8K-bit secured OTP

The secured OTP for unique identifier: to provide 8K-bit one-time program area for setting device unique serial number. Which may be set by factory or system customer.

- Security register bit 0 indicates whether the chip is locked by factory or not.

- To program the 8K-bit secured OTP by entering secured OTP mode (with Enter Security OTP command), and going through normal program procedure, and then exiting secured OTP mode by writing Exit Security OTP command.

- Customer may lock-down the customer lockable secured OTP by writing WRSCUR(write security register) command to set customer lock-down bit1 as "1". Please refer to *"Table 14. Security Register Definition"* for security register bit definition and *"Table 4. Secured OTP Definition"* for address range definition.

- Note: Once lock-down by factory or customer, the corresponding range cannot be changed any more. While in secured OTP mode, array access is not allowed.

Table 4. Secured OTP Definition

Address range	Size	Lock-down
xxx000~xxx1FF	4096-bit	Determined by Customer
xxx200~xxx3FF	4096-bit	Determined by Factory

7. DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.

2. When incorrect command# sequence is inputted to this device, this device becomes standby mode and keeps the standby mode until next CS# falling edge. In standby mode, SO pin of this device should be High-Z.

3. When correct command# sequence is inputted to this device, this device becomes active mode and keeps the active mode until next CS# rising edge.

4. When device under STR mode, input data is latched on the rising edge of Serial Clock (SCLK) and data shifts out on the falling edge of SCLK. When device under DTR mode, input data is latched on the both rising and falling edge of Serial Clock (SCLK) and data shifts out on both rising and falling edge of SCLK.

5. While a Write Status Register, Program or Erase operation is in progress, access to the memory array is neglected and not affect the current operation of Write Status Register, Program, Erase.

Figure 1. Input Timing (STR mode)

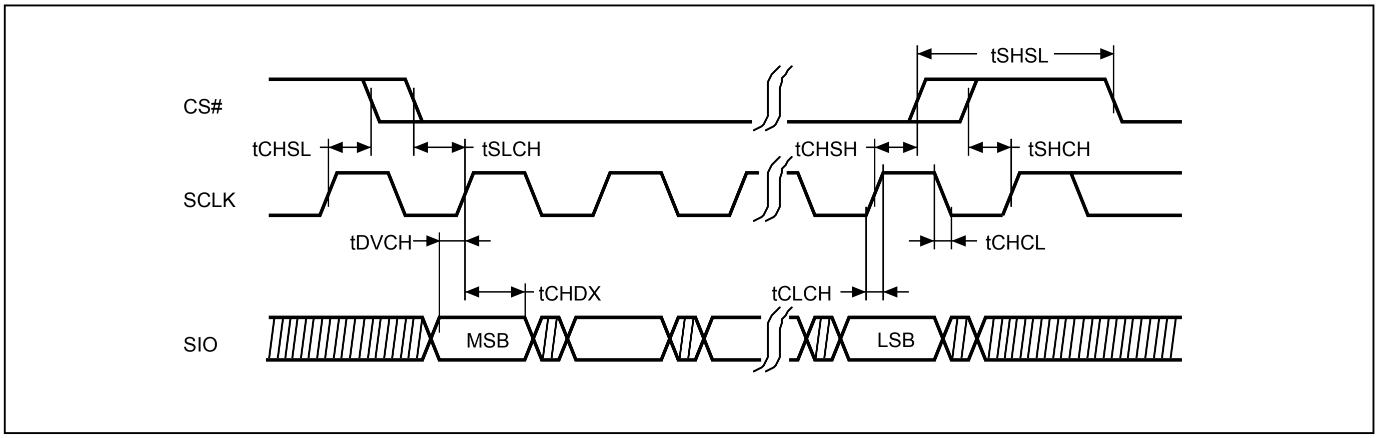


Figure 2. Input Timing (DTR mode)

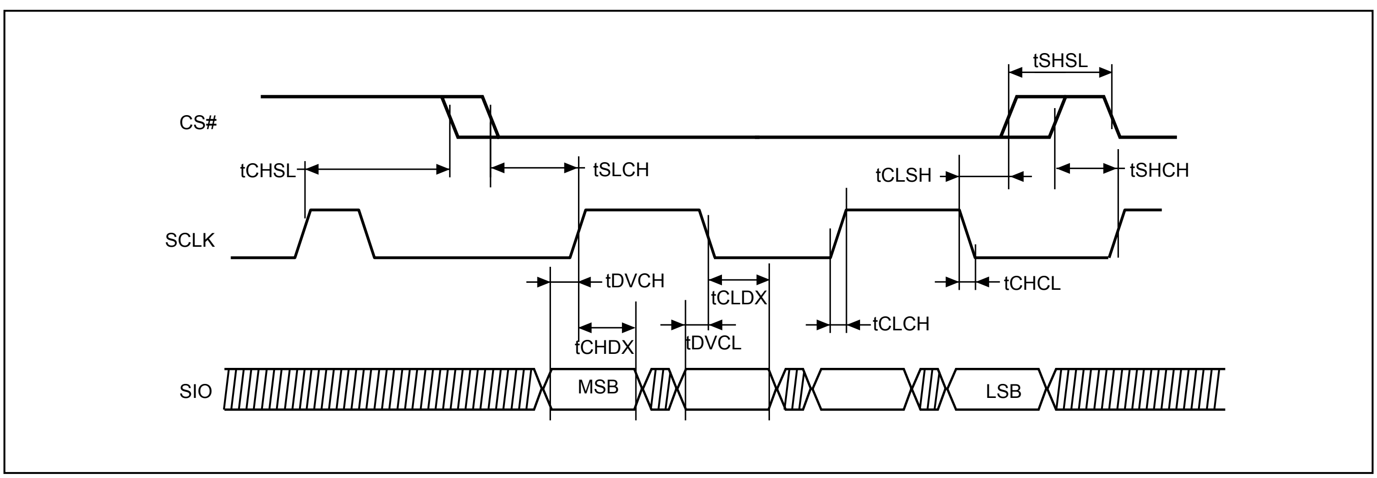


Figure 3. Output Timing (STR mode)

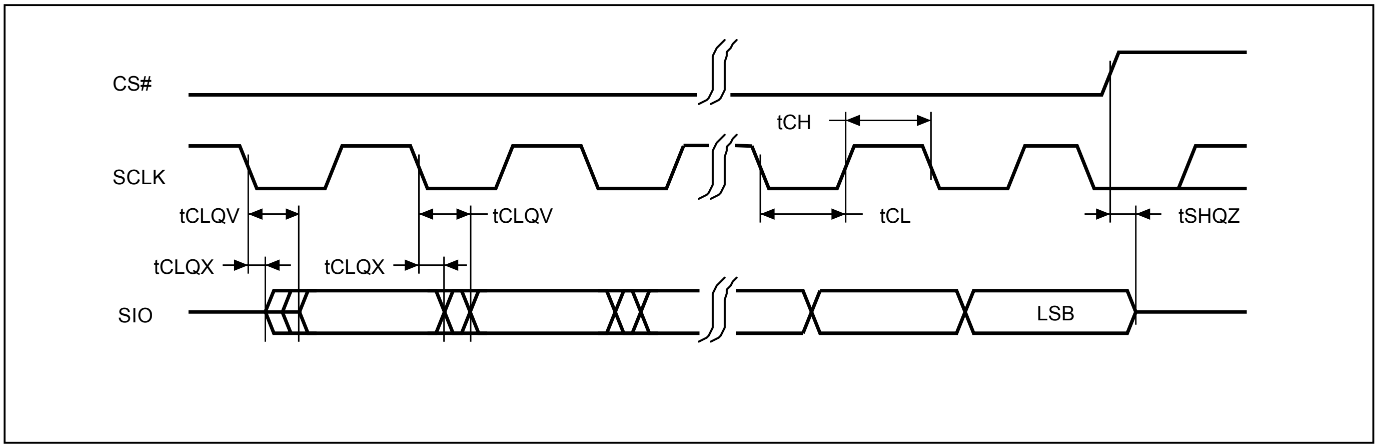
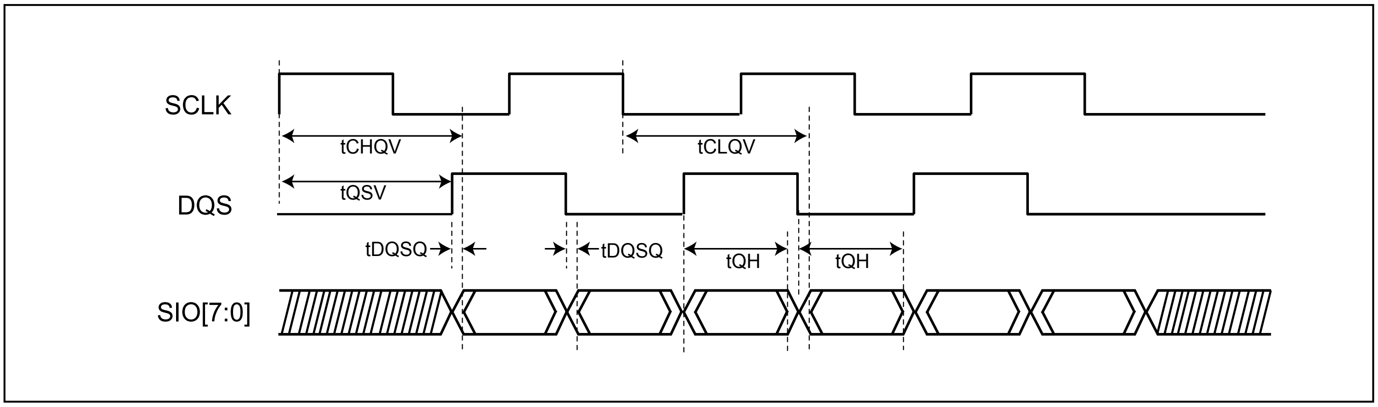


Figure 4. Output Timing (DTR mode)



8. COMMAND SET

8-1. SPI Command Set

Table 5. Read/Write Array Commands (SPI - 3 Byte Address Command Set)

Command (byte)	READ3B (normal read)	FAST_READ3B (fast read data)	PP3B (page program)	SE3B (sector erase)	BE3B (block erase 64KB)	CE (chip erase)
Address Bytes	3	3	3	3	3	
1st byte	03 (hex)	0B (hex)	02 (hex)	20 (hex)	D8 (hex)	60 or C7 (hex)
2nd byte	ADD1	ADD1	ADD1	ADD1	ADD1	
3rd byte	ADD2	ADD2	ADD2	ADD2	ADD2	
4th byte	ADD3	ADD3	ADD3	ADD3	ADD3	
5th byte		Dummy(8)				
Data Cycles			1-256			
Action	n bytes read out until CS# goes high	n bytes read out until CS# goes high	to program the selected page	to erase the selected sector	to erase the selected block	to erase whole chip

Table 6. Read/Write Array Commands (SPI - 4 Byte Address Command Set)

Command (byte)	READ4B (normal read)	FAST_READ4B (fast read data)	PP4B (page program)	SE4B (sector erase)	BE4B (block erase 64KB)
Address Bytes	4	4	4	4	4
1st byte	13 (hex)	0C (hex)	12 (hex)	21 (hex)	DC (hex)
2nd byte	ADD1	ADD1	ADD1	ADD1	ADD1
3rd byte	ADD2	ADD2	ADD2	ADD2	ADD2
4th byte	ADD3	ADD3	ADD3	ADD3	ADD3
5th byte	ADD4	ADD4	ADD4	ADD4	ADD4
6th byte		Dummy(8)			
Data Cycles			1-256		
Action	n bytes read out until CS# goes high	n bytes read out until CS# goes high	to program the selected page	to erase the selected sector	to erase the selected block

Table 7. Setting Commands (SPI)

Command (byte)	WREN (write enable)	WRDI (write disable)	PGM/ERS Suspend (Suspends Program/ Erase)	PGM/ERS Resume (Resumes Program/ Erase)	DP (Deep power down)
1st byte	06 (hex)	04 (hex)	B0 (hex)	30 (hex)	B9 (hex)
2nd byte					
3rd byte					
4th byte					
5th byte					
Data Cycles					
Action	sets the (WEL) write enable latch bit	resets the (WEL) write enable latch bit			enters deep power down mode

Command (byte)	RDP (Release from deep power down)	SBL (Set Burst Length)	ENSO (enter secured OTP)	EXSO (exit secured OTP)
1st byte	AB (hex)	C0 (hex)	B1 (hex)	C1 (hex)
2nd byte				
3rd byte				
4th byte				
5th byte				
Data Cycles		1		
Action	release from deep power down mode	to set Burst length	to enter the 8K-bit secured OTP mode	to exit the 8K-bit secured OTP mode

Table 8. Reset Commands (SPI)

Command (byte)	NOP (No Operation)	RSTEN (Reset Enable)	RST (Reset Memory)
1st byte	00 (hex)	66 (hex) (Note 2)	99 (hex) (Note 2)
2nd byte			
3rd byte			
4th byte			
5th byte			
Action			

Table 9. Register Commands (SPI)

Command (byte)	RDID (read identification)	RDSFDP	RDSR (read status register)	RDCR (read configuration register)	WRSR (write status/ configuration register)	RDCR 2 (read configuration register 2)	WRCR2 (Write configuration register 2)
1st byte	9F (hex)	5A (hex)	05 (hex)	15 (hex)	01 (hex)	71 (hex)	72 (hex)
2nd byte		ADD1				ADD1	ADD1
3rd byte		ADD2				ADD2	ADD2
4th byte		ADD3				ADD3	ADD3
5th byte						ADD4	ADD4
Data Cycles			1	1	1-2	1	1
Action	outputs JEDEC ID: 1-byte Manufacturer ID & 2-byte Device ID	Read SFDP mode	to read out the values of the status register	to read out the values of the configuration register	to write new values of the status/ configuration register		

Command (byte)	RDFBR (read fast boot register)	WRFBR (write fast boot register)	ESFBR (erase fast boot register)	RDSCUR (read security register)	WRSCUR (write security register)	WRLR (write Lock register)	RDLR (read Lock register)
Address Bytes	16 (hex)	17 (hex)					
1st byte			18 (hex)	2B (hex)	2F (hex)	2C (hex)	2D (hex)
2nd byte							
3rd byte							
4th byte							
5th byte	1-4	4					
Data Cycles						1	1
Action				to read value of security register	to set the lock-down bit as "1" (once lock-down, cannot be updated)		

Command (byte)	WRSPB (SPB bit program)	ESSPB (all SPB bit erase)	RDSPB (read SPB status)	WRDPB (write DPB register)	RDDPB (read DPB register)	WPSEL (Write Protect Selection)	GBLK (gang block lock)	GBULK (gang block unlock)
Address Bytes	4	0	4	4	4		0	0
1st byte	E3 (hex)	E4 (hex)	E2 (hex)	E1 (hex)	E0 (hex)	68 (hex)	7E (hex)	98 (hex)
2nd byte	ADD1		ADD1	ADD1	ADD1			
3rd byte	ADD2		ADD2	ADD2	ADD2			
4th byte	ADD3		ADD3	ADD3	ADD3			
5th byte	ADD4		ADD4	ADD4	ADD4			
Data Cycles			1	1	1			
Action						to enter and enable individal block protect mode	whole chip write protect	whole chip unprotect

Note 1: It is not recommended to adopt any other code/address not in the command definition table, which will potentially enter the hidden mode.

Note 2: Before executing RST command, RSTEN command must be executed. If there is any other command to interfere, the reset operation will be disabled.

Note 3: The number in parentheses after "ADD" or "Data" stands for how many clock cycles it has. For example, "Data(8)" represents there are 8 clock cycles for the data in.

8-2. OPI Command Set

Table 10. Read/Write Array Commands (OPI)

Command (byte)	8READ (Octa IO Read)	8DTRD (Octa IO DT Read)	RDID (read identification)	RDSFDP
1st byte	EC (hex)	EE (hex)	9F (hex)	5A (hex)
2nd byte	13 (hex)	11 (hex)	60 (hex)	A5 (hex)
3rd byte	ADD1	ADD1	00h	ADD1
4th byte	ADD2	ADD2	00h	ADD2
5th byte	ADD3	ADD3	00h	ADD3
6th byte	ADD4	ADD4 (Note 6)	00h	ADD4
7th byte	Dummy (Note 4)	Dummy (Note 4)		Dummy(20)
Data Cycles			3 (Note 8)	
Action	Octa I/O STR read	Octa I/O DTR read	outputs JEDEC ID: 1-byte Manufacturer ID & 2-byte Device ID	Read SFDP mode

Command (byte)	PP (page program)	SE (sector erase)	BE (block erase 64KB)	CE (chip erase)
1st byte	12 (hex)	21 (hex)	DC (hex)	60 or C7 (hex)
2nd byte	ED (hex)	DE (hex)	23 (hex)	9F or 38 (hex)
3rd byte	ADD1	ADD1	ADD1	
4th byte	ADD2	ADD2	ADD2	
5th byte	ADD3	ADD3	ADD3	
6th byte	ADD4 (Note 6)	ADD4	ADD4	
7th byte				
Data Cycles	1-256			
Action	to program the selected page	to erase the selected sector	to erase the selected block	to erase whole chip

Table 11. Setting Commands (OPI)

Command (byte)	WREN (write enable)	WRDI (write disable)	PGM/ERS Suspend (Suspends Program/ Erase)	PGM/ERS Resume (Resumes Program/ Erase)	DP (Deep power down)
1st byte	06 (hex)	04 (hex)	B0 (hex)	30 (hex)	B9 (hex)
2nd byte	F9 (hex)	FB (hex)	4F (hex)	CF (hex)	46 (hex)
3rd byte					
4th byte					
5th byte					
6th byte					
7th byte					
Data Cycles	sets the (WEL) write enable latch bit	resets the (WEL) write enable latch bit			enters deep power down mode

Command (byte)	SBL (Set Burst Length)	ENSO (enter secured OTP)	EXSO (exit secured OTP)
1st byte	C0 (hex)	B1 (hex)	C1 (hex)
2nd byte	3F (hex)	4E (hex)	3E (hex)
3rd byte	00h		
4th byte	00h		
5th byte	00h		
6th byte	00h		
7th byte	1		
Data Cycles	to set Burst length	to enter the 8K-bit secured OTP mode	to exit the 8K-bit secured OTP mode

Table 12. Reset Commands (OPI)

Command (byte)	NOP (No Operation)	RSTEN (Reset Enable)	RST (Reset Memory)
1st byte	00 (hex)	66 (hex)(Note 2)	99 (hex)(Note 2)
2nd byte	FF (hex)	99 (hex)	66 (hex)
3rd byte			
4th byte			
5th byte			
6th byte			
Data Cycles			

Table 13. Register Commands (OPI)

Command (byte)	RDSR (read status register)	RDCR (read configuration register)	WRSR (write status register)	WRCR (write configuration register)	RDCR2 (read configuration register 2)	WRCR2 (Write configuration register 2)	RDFBR (read fast boot register)
1st byte	05 (hex)	15 (hex)	01 (hex)	01 (hex)	71 (hex)	72 (hex)	16 (hex)
2nd byte	FA (hex)	EA (hex)	FE (hex)	FE (hex)	8E (hex)	8D (hex)	E9 (hex)
3rd byte	00h	00h	00h	00h	ADD1	ADD1	00h
4th byte	00h	00h	00h	00h	ADD2	ADD2	00h
5th byte	00h	00h	00h	00h	ADD3	ADD3	00h
6th byte	00h	01h	00h	01h	ADD4	ADD4	00h
7th byte	Dummy(Note 5)	Dummy(Note 5)			Dummy(Note 5)		Dummy(Note 5)
Data bytes	1	1	1	1	1	1	1-4(Note 8)
Action	to read out the values of the status register	to read out the values of the configuration register	to write new values of the status register	to write new values of the configuration register			

Command (byte)	WRFBR (write fast boot register)	ESFBR (erase fast boot register)	RDSCUR (read security register)	WRSCUR (write security register)	WRLR (write Lock register)	RDLR (read Lock register)	WRSPB (SPB bit program)
1st byte	17 (hex)	18 (hex)	2B (hex)	2F (hex)	2C (hex)	2D (hex)	E3 (hex)
2nd byte	E8 (hex)	E7 (hex)	D4 (hex)	D0 (hex)	D3 (hex)	D2 (hex)	1C (hex)
3rd byte	00h		00h		00h	00h	ADD1
4th byte	00h		00h		00h	00h	ADD2
5th byte	00h		00h		00h	00h	ADD3
6th byte	00h		00h		00h	00h	ADD4
7th byte			Dummy(Note 5)			Dummy(Note 5)	
Data bytes	4				1	1	
Action			to read value of security register	to set the lock-down bit as "1" (once lock-down, cannot be updated)			

Command (byte)	ESSPB (all SPB bit erase)	RDSPB (read SPB status)	WRDPB (write DPB register)	RDDPB (read DPB register)	WPSEL (Write Protection Selection)	GBLK (gang block lock)	GBULK (gang block unlock)
1st byte	E4 (hex)	E2 (hex)	E1 (hex)	E0 (hex)	68 (hex)	7E (hex)	98 (hex)
2nd byte	1B (hex)	1D (hex)	1E (hex)	1F (hex)	97 (hex)	81 (hex)	67 (hex)
3rd byte		ADD1	ADD1	ADD1			
4th byte		ADD2	ADD2	ADD2			
5th byte		ADD3	ADD3	ADD3			
6th byte		ADD4	ADD4	ADD4			
7th byte		Dummy(Note 4)		Dummy(Note 4)			
Data bytes		1	1	1			
Action					to enter and enable individual block protect mode	whole chip write protect	whole chip unprotect

Note 1: It is not recommended to adopt any other code/address not in the command definition table, which will potentially enter the hidden mode.

Note 2: Before executing RST command, RSTEN command must be executed. If there is any other command to interfere, the reset operation will be disabled.

Note 3: The number in parentheses after "ADD" or "Data" stands for how many clock cycles it has. For example, "Data(8)" represents there are 8 clock cycles for the data in.

Note 4: See dummy cycle and frequency table.

Note 5: 4 dummy cycles in both STR/DTR.

Note 6: The starting address must be even byte (A0 must be 0) in DTR OPI mode.

Note 7: The address data must be 00h.

Note 8: Data bytes are always output in STR.

9. REGISTER DESCRIPTION

9-1. Status Register

The definition of the status register bits is as below:

WIP bit. The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

WEL bit. The Write Enable Latch (WEL) bit, a volatile bit, indicates whether the device is set to internal write enable latch. When WEL bit sets to 1, which means the internal write enable latch is set, the device can accept program/erase/write status register instruction. When WEL bit sets to 0, which means no internal write enable latch; the device will not accept program/erase/write status register instruction. The program/erase command will be ignored if it is applied to a protected memory area. To ensure both WIP bit & WEL bit are both set to 0 and available for next program/erase/operations, WIP bit needs to be confirm to be 0 before polling WEL bit. After WIP bit confirmed, WEL bit needs to be confirm to be 0.

BP3, BP2, BP1, BP0 bits. The Block Protect (BP3, BP2, BP1, BP0) bits, non-volatile bits, indicate the protected area (as defined in *Table 3*) of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP3, BP2, BP1, BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP/PP3B/PP4B), Sector Erase (SE/SE3B/SE4B), Block Erase (BE/BE3B/BE4B) and Chip Erase (CE) instructions (only if Block Protect bits (BP3:BP0) set to 0, the CE instruction can be executed). The BP3, BP2, BP1, BP0 bits are "0" as default. Which is un-protected.

Status Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Reserved	Reserved	BP3 (level of protected block)	BP2 (level of protected block)	BP1 (level of protected block)	BP0 (level of protected block)	WEL (write enable latch)	WIP (write in progress bit)
Reserved	Reserved	(note 1)	(note 1)	(note 1)	(note 1)	1=write enable 0=not write enable	1=write operation 0=not in write operation
Reserved	Reserved	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note 1: see the *Table 3* "Protected Area Size".

9-2. Configuration Register

The Configuration Register is able to change the default status of Flash memory. Flash memory will be configured after the CR bit is set.

ODS bit
The output driver strength (ODS2, ODS1, ODS0) bits are volatile bits, which indicate the output driver level (as defined in *"Output Driver Strength Table"*) of the device. The Output Driver Strength is defaulted as 30 Ohms when delivered from factory. To write the ODS bits requires the Write Status Register (WRSR) instruction to be executed.

TB bit
The Top/Bottom (TB) bit is a non-volatile bit. The Top/Bottom (TB) bit is used to configure the Block Protect area by BP bit (BP3, BP2, BP1, BP0), starting from TOP or Bottom of the memory array. The TB bit is defaulted as “0”, which means Top area protect. When it is set as “1”, the protect area will change to Bottom area of the memory device. To write the TB bits requires the Write Status Register (WRSR) instruction to be executed.

PBE bit
The Preamble Bit Enable (PBE) bit is a volatile bit. It is used to enable or disable the preamble bit data pattern output on dummy cycles. The PBE bit is defaulted as “0”, which means preamble bit is disabled. When it is set as “1”, the preamble bit will be enabled, and inputted into dummy cycles. To write the PBE bits requires the Write Status Register (WRSR) instruction to be executed.

Configuration Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Reserved	Reserved	Reserved	PBE (Preamble bit Enable)	TB (top/bottom selected)	ODS 2 (output driver strength)	ODS 1 (output driver strength)	ODS 0 (output driver strength)
x	x	x	0=Disable 1=Enable	0=Top area protect 1=Bottom area protect (Default=0)	(Note 1)	(Note 1)	(Note 1)
x	x	x	volatile bit	OTP	volatile bit	volatile bit	volatile bit

Note 1: see *"Output Driver Strength Table"*

Output Driver Strength Table

ODS2	ODS1	ODS0	Description	Note
0	0	0	146 Ohms	Impedance at VCC/2 (Typical)
0	0	1	76 Ohms	
0	1	0	52 Ohms	
0	1	1	41 Ohms	
1	0	0	34 Ohms	
1	0	1	30 Ohms	
1	1	0	26 Ohms	
1	1	1	24 Ohms (Default)	

9-3. Configuration Register 2

Address	Bit	Symbol	Description	Define	Default	Type
00000000h	Bit 7-2	x	Reserved	Reserved	x	x
	Bit 1	DOPI [1]	DTR OPI Enable	00= SPI 01= STR OPI enable 10= DTR OPI enable 11= inhibit	0	Volatile Bit
	Bit 0	SOPI [1]	STR OPI Enable		0	Volatile Bit
00000200h	Bit 7-4	x	Reserved	Reserved	x	x
	Bit 3-2	x	Reserved	Reserved	x	x
	Bit 1	DOS	DQS on STR mode	0= Disable 1= Enable	0	Volatile Bit
	Bit 0	DQSPRC	DTR DQS pre-cycle	0= 0 cycle 1= 1 cycle	0	Volatile Bit
00000300h	Bit 7-3	x	Reserved	Reserved	x	x
	Bit 2-0	DC	Dummy cycle	Refer to *"9-3-2. Dummy Cycle and Frequency Table (MHz)"*	000	Volatile Bit
00000500h	Bit 7	x	Reserved		x	x
	Bit 6-5	x	Reserved		x	x
	Bit 4	x	Reserved		x	x
	Bit 3-1	x	Reserved	Reserved	x	x
	Bit 0	PPTSEL	Preamable pattern selection	refer to *"9-3-3. Preamable Pattern Select Bit Table"*	0	Volatile Bit
40000000h	Bit 7-4	x	Reserved	Reserved	x	x
	Bit 3	x	Reserved		x	x
	Bit 2	x	Reserved	Reserved	x	x
	Bit 1	DEFDOPI# [1,2]	Enable DOPI after power on reset	00= inhibit 01= default DTR OPI mode 10= default STR OPI mode 11= default SPI mode	1	OTP
	Bit 0	DEFSOPI# [1,2]	Enable SOPI after power on reset		1	OTP

Notes:

1. The default status of DOPI and SOPI reflect the DEFDOPI# and DEFSOPI# setting. For example, if DEFDOPI#/DEFSOPI# are 01, DOPI and SOPI value will change to 10 after next power on and default status of the device will be DTR OPI.
2. The default DEFDOPI# status depends on the device model selection.

9-3-1. Dummy Cycle and Frequency Table (MHz)

DC [2:0]	Numbers of Dummy Cycle	Octa I/O STR (MHz)	Octa I/O DTR (MHz)
000(Default)	20	133	133
001	18	133	133
010	16	133	133
011	14	133	133
100	12	104	104
101	10	104	104
110	8	84	84
111	6	66	66

9-3-2. Preamable Pattern Select Bit Table

	All SIOs (Except SIO3)	SIO3
Bit 0= 0	0011 0100 1001 1010	0011 0101 0001 0100
Bit 0= 1	0101 0101 0101 0101	0101 0101 0101 0101

9-4. Security Register

The definition of the Security Register bits is as below:

Erase Fail bit. The Erase Fail bit is a status flag, which shows the status of last Erase operation. It will be set to "1", if the erase operation fails or the erase region is protected. It will be set to "0", if the last operation is successful. Please note that it will not interrupt or stop any operation in the flash memory.

Program Fail bit. The Program Fail bit is a status flag, which shows the status of last Program operation. It will be set to "1", if the program operation fails or the program region is protected. It will be set to "0", if the last operation is successful. Please note that it will not interrupt or stop any operation in the flash memory.

Erase Suspend bit. Erase Suspend Bit (ESB) indicates the status of Erase Suspend operation. Users may use ESB to identify the state of flash memory. After the flash memory is suspended by Erase Suspend command, ESB is set to "1". ESB is cleared to "0" after erase operation resumes.

Program Suspend bit. Program Suspend Bit (PSB) indicates the status of Program Suspend operation. Users may use PSB to identify the state of flash memory. After the flash memory is suspended by Program Suspend command, PSB is set to "1". PSB is cleared to "0" after program operation resumes.

Secured OTP Indicator bit. The Secured OTP indicator bit shows the chip is locked by factory or not. When it is "0", it indicates non-factory lock; "1" indicates factory-lock.

Lock-down Secured OTP (LDSO) bit. By writing WRSCUR instruction, the LDSO bit may be set to "1" for customer lock-down purpose. However, once the bit is set to "1" (lock-down), the LDSO bit and the 8K-bit Secured OTP area cannot be updated any more. While it is in 8K-bit secured OTP mode, main array access is not allowed.

Table 14. Security Register Definition

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
WPSEL	E_FAIL	P_FAIL	Reserved	ESB (Erase Suspend bit)	PSB (Program Suspend bit)	LDSO (indicate if lock-down)	Secured OTP indicator bit
0=normal WP mode 1=individual mode (default=0)	0=normal Erase succeed 1=indicate Erase failed (default=0)	0=normal Program succeed 1=indicate Program failed (default=0)	-	0=Erase is not suspended 1= Erase suspended (default=0)	0=Program is not suspended 1= Program suspended (default=0)	0 = not lock-down 1 = lock-down (cannot program/ erase OTP)	0 = non-factory lock 1 = factory lock
Non-volatile bit (OTP)	Volatile bit	Volatile bit	-	Volatile bit	Volatile bit	Non-volatile bit (OTP)	Non-volatile bit (Read only)

10. COMMAND DESCRIPTION

10-1. Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP/PP3B/PP4B, SE/SE3B/SE4B, BE/BE3B/BE4B, CE, WRSR, WRCR2, SBL, WRFBR, ESFBR, WRSCUR, WRLR, WSPB and ESSPB which are intended to change the device content WEL bit should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low→sending WREN instruction code→ CS# goes high.

Figure 5. Write Enable (WREN) Sequence (SPI Mode)

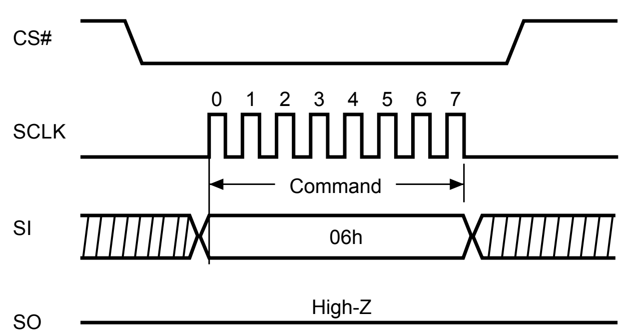


Figure 6. Write Enable (WREN) Sequence (STR-OPI Mode)

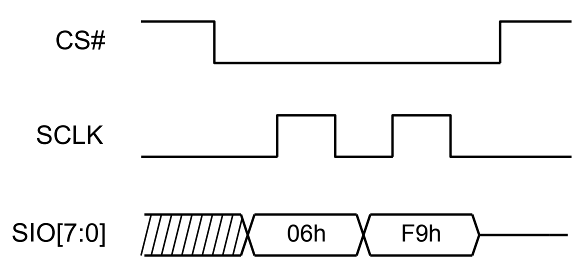
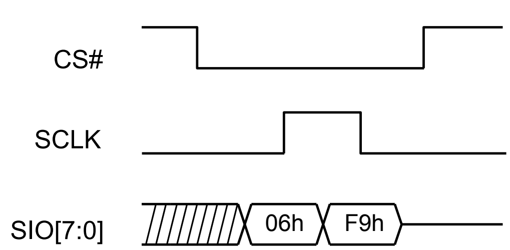


Figure 7. Write Enable (WREN) Sequence (DTR-OPI Mode)



10-2. Write Disable (WRDI)

The Write Disable (WRDI) instruction is to reset Write Enable Latch (WEL) bit. The sequence of issuing WRDI instruction is: CS# goes low→sending WRDI instruction code→CS# goes high.
The WEL bit is reset by following situations:

- Power-up
- Reset# pin driven low
- WRDI command completion
- WRSR/WRCR/WRCR2 command completion
- PP/PP3B/PP4B command completion
- SE/SE3B/SE4B/BE/BE3B/BE4B/CE command completion
- SBL command completion
- PGM/ERS Suspend command completion
- Softreset command completion
- WRSCUR command completion
- WRFBR/ESFBR command completion
- WRLR/WSPB/ESSPB command completion
- GBLK/GBULK command completion

Figure 8. Write Disable (WRDI) Sequence (SPI Mode)

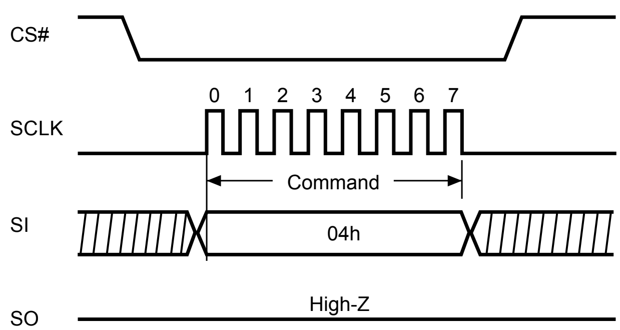


Figure 9. Write Disable (WRDI) Sequence (STR-OPI Mode)

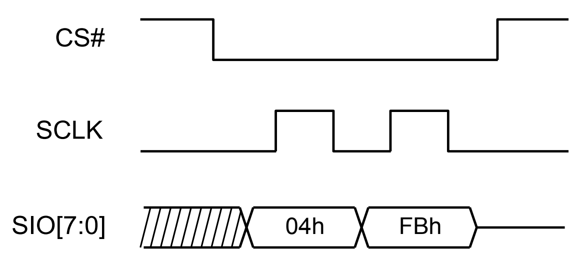
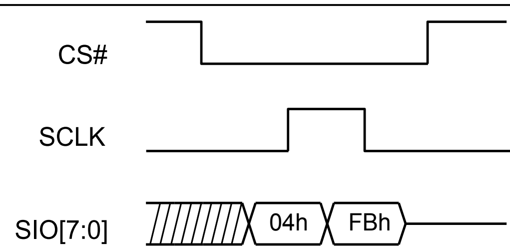


Figure 10. Write Disable (WRDI) Sequence (DTR-OPI Mode)



10-3. Read Identification (RDID)

The RDID instruction is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The Macronix Manufacturer ID and Device ID are listed as *Table 15* ID Definitions.

The sequence of issuing RDID instruction is: CS# goes low→ sending RDID instruction code→24-bits ID data out on SO→ to end RDID operation can drive CS# to high at any time during data out.

While Program/Erase operation is in progress, it will not decode the RDID instruction, therefore there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

Table 15. ID Definitions

RDID	9Fh	Manufactory ID	Memory type	Memory density
		C2	85	3A

Figure 11. Read Identification (RDID) Sequence (SPI mode)

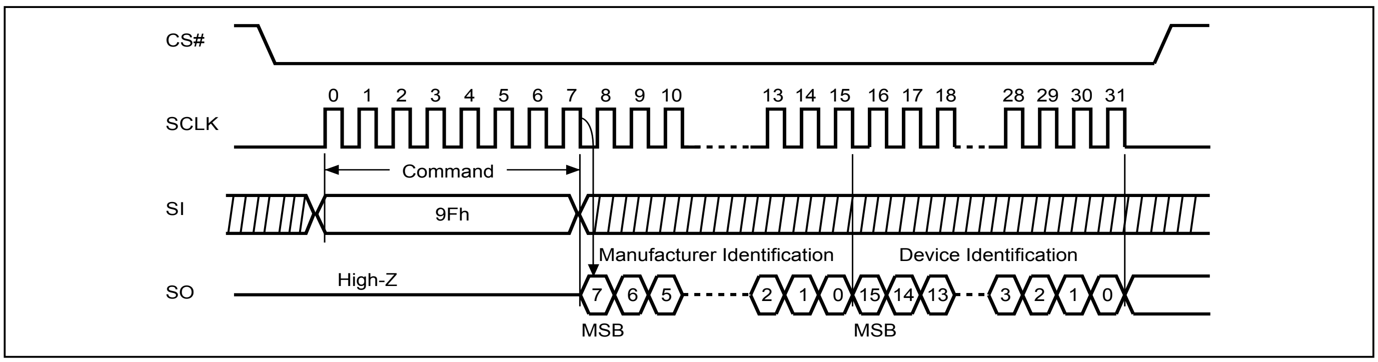


Figure 12. Read Identification (RDID) Sequence (STR-OPI Mode)

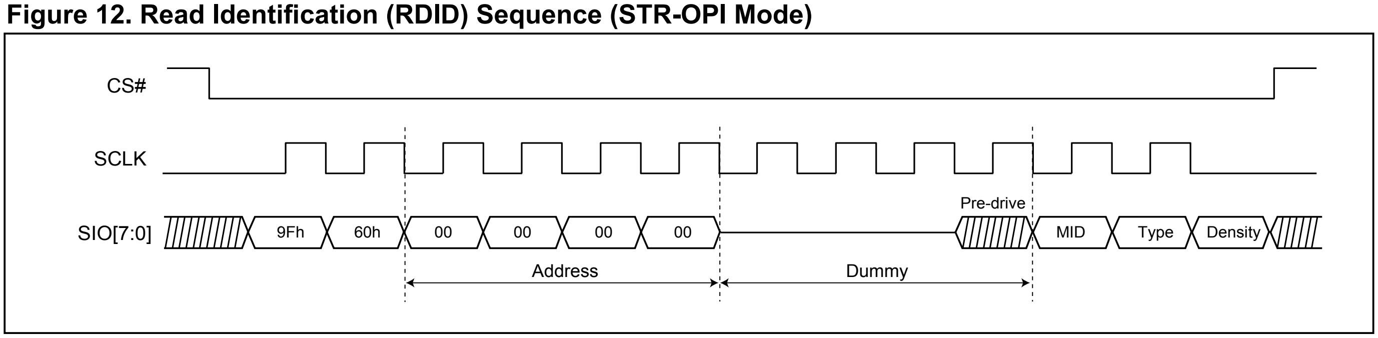
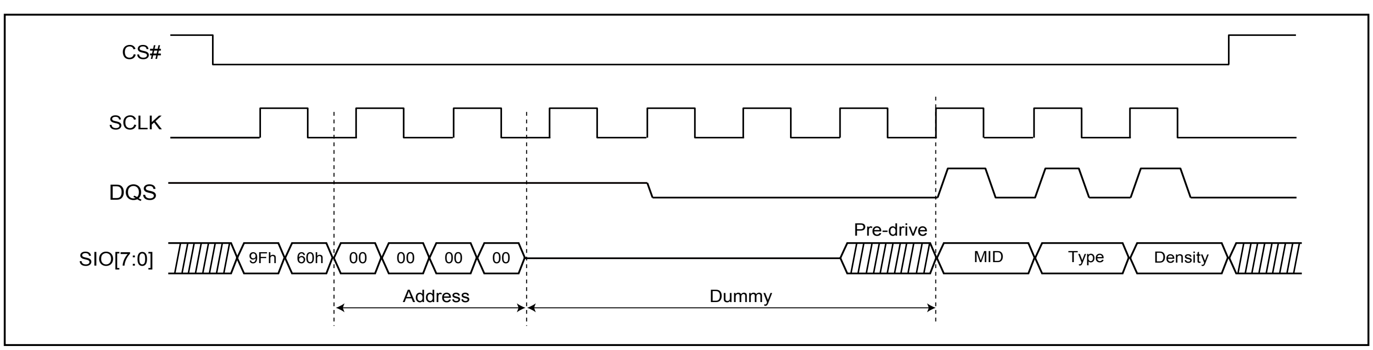


Figure 13. Read Identification (RDID) Sequence (DTR-OPI Mode)



10-4. Read Status Register (RDSR)

The RDSR instruction is for reading Status Register Bits. The Read Status Register can be read at any time (even in program/erase/write status register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDSR instruction is: CS# goes low→ sending RDSR instruction code→ Status Register data out on SO.

Figure 14. Read Status Register (RDSR) Sequence (SPI Mode)

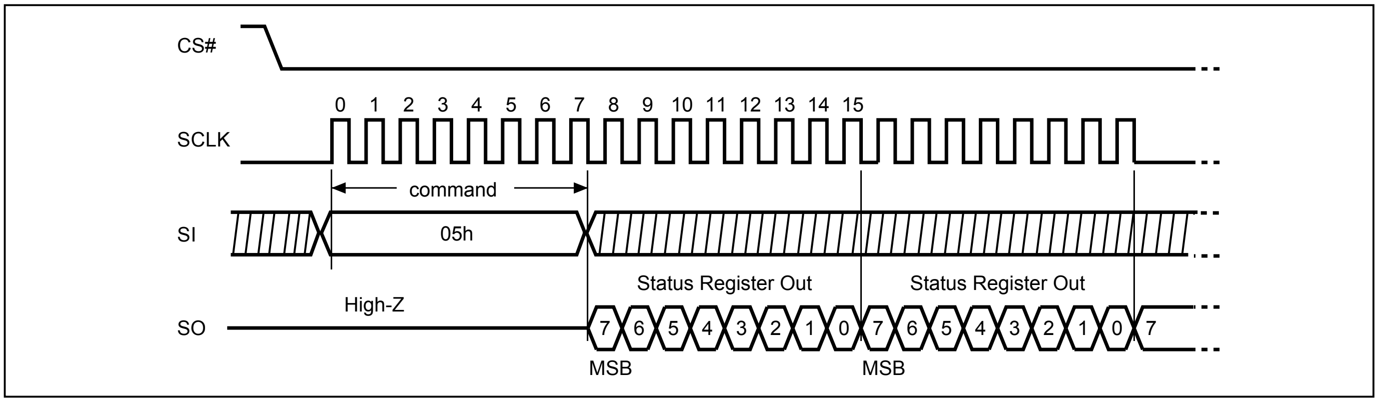


Figure 15. Read Status Register (RDSR) Sequence (STR-OPI Mode)

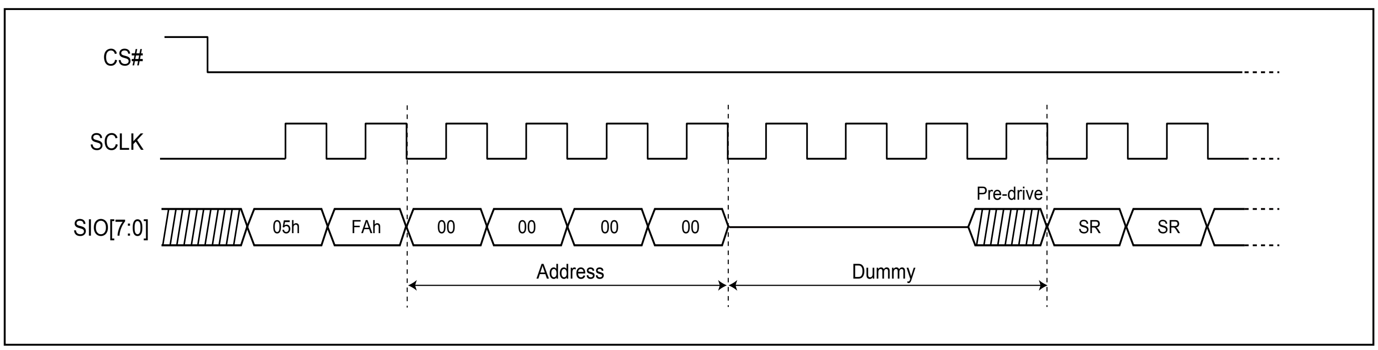
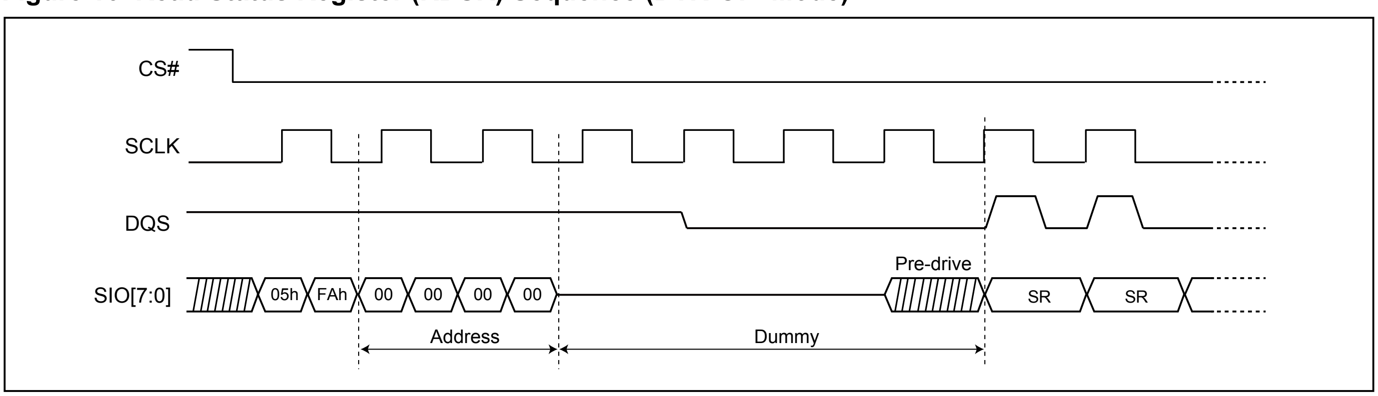


Figure 16. Read Status Register (RDSR) Sequence (DTR-OPI Mode)



For user to check if Program/Erase operation is finished or not, RDSR instruction flow are shown as follows:

Figure 17. Program/Erase flow with read array data

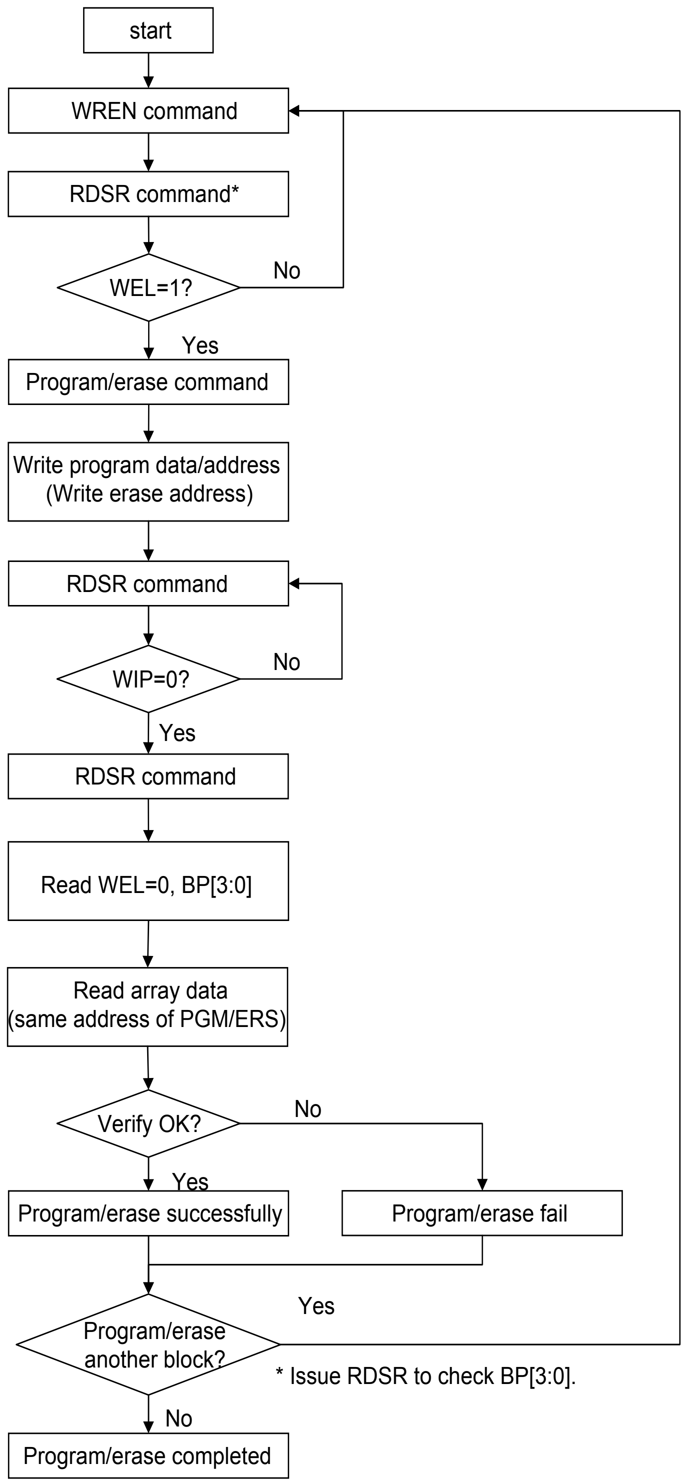
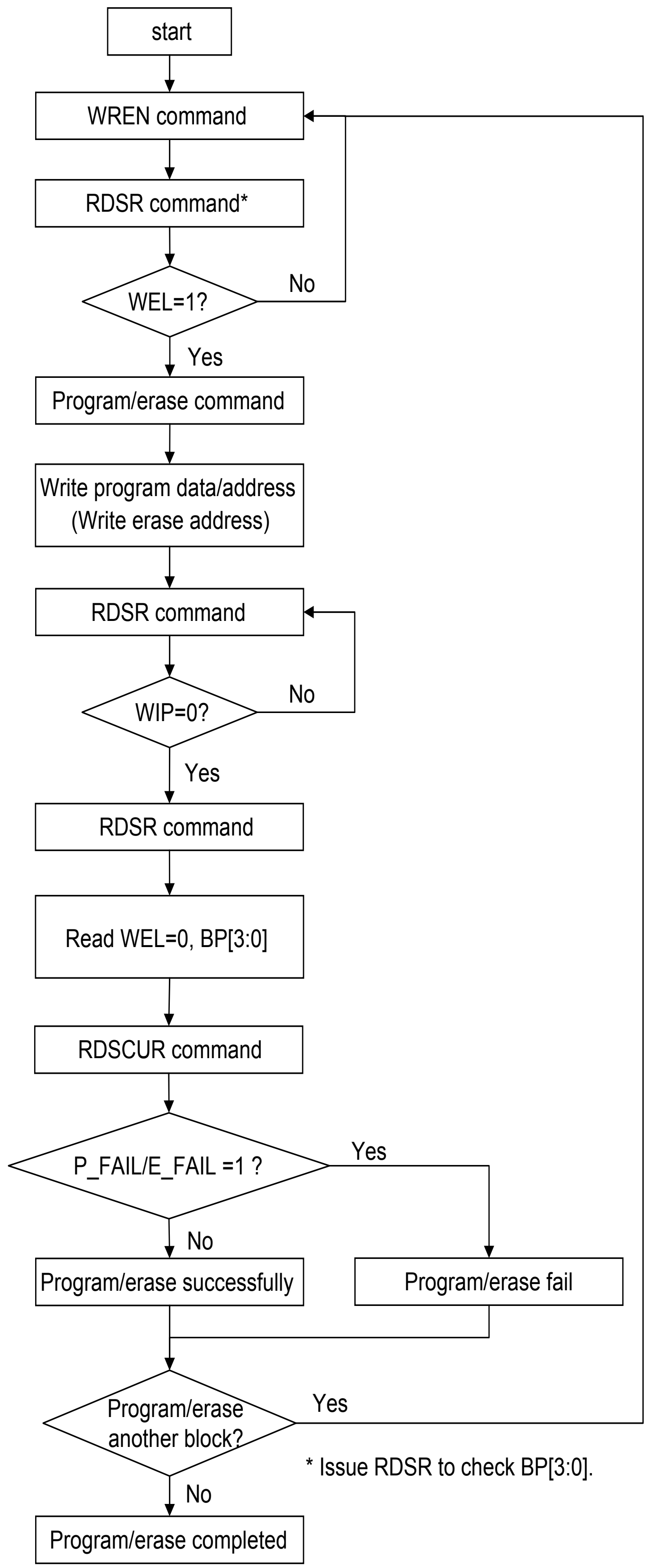


Figure 18. Program/Erase flow without read array data (read P_FAIL/E_FAIL flag)



10-5. Read Configuration Register (RDCR)

The RDCR instruction is for reading Configuration Register Bits. The Read Configuration Register can be read at any time (even in program/erase/write configuration register condition).

The sequence of issuing RDCR instruction is: CS# goes low→ sending RDCR instruction code→ Configuration Register data out on SO.

Figure 19. Read Configuration Register (RDCR) Sequence (SPI Mode)

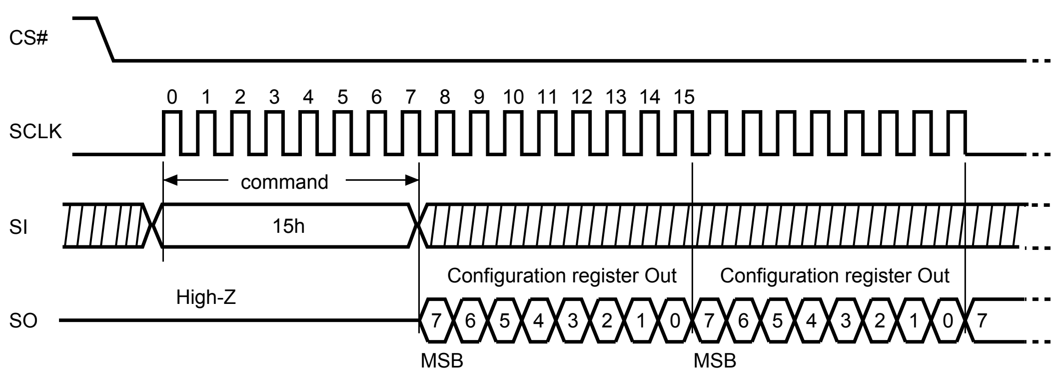


Figure 20. Read Configuration Register (RDCR) (STR-OPI Mode)

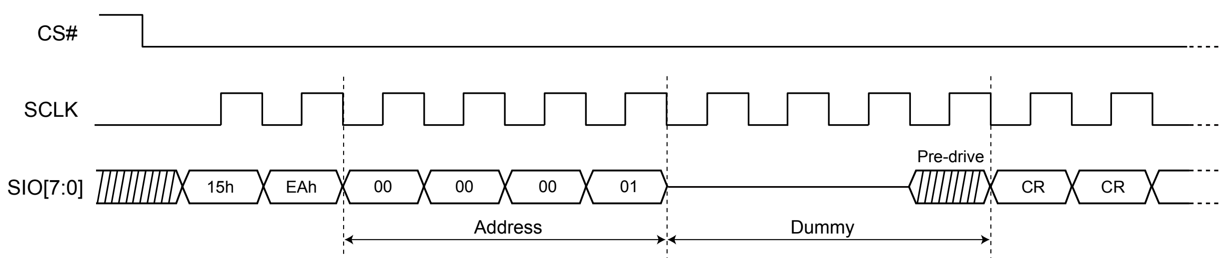
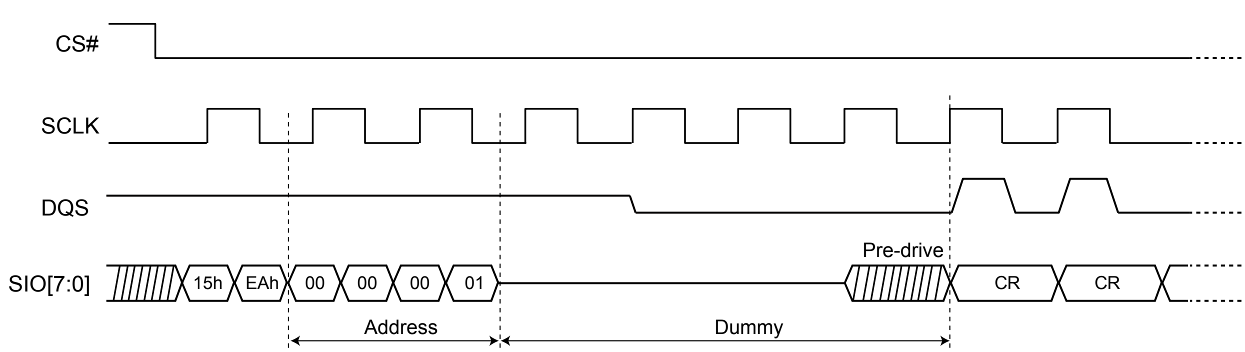


Figure 21. Read Configuration Register (RDCR) (DTR-OPI Mode)

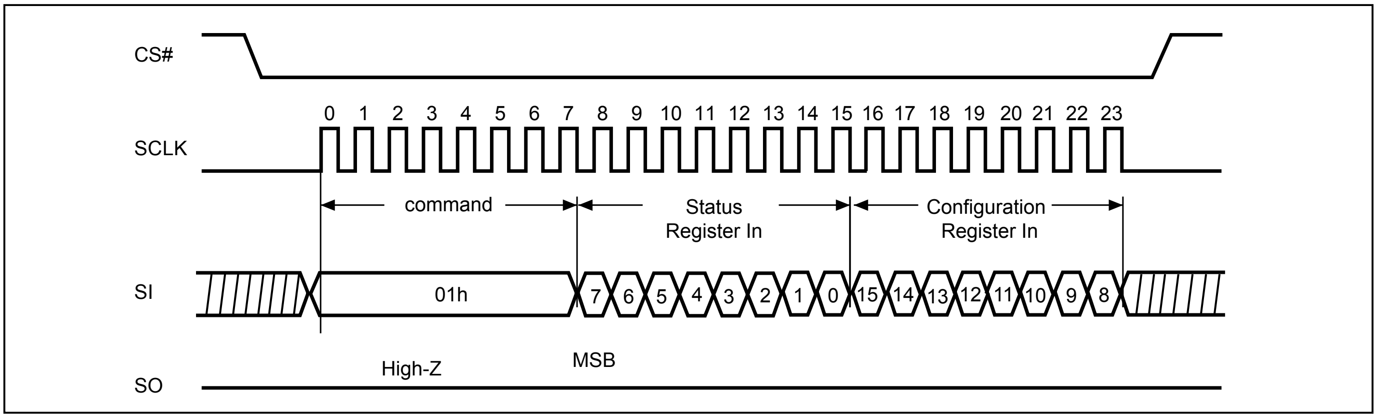


10-6. Write Status Register (WRSR) / Write Configuration Register (WRCR)

The WRSR instruction is for changing the values of Status Register Bits and Configuration Register Bits. Before sending WRSR instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR instruction can change the value of Block Protect (BP3, BP2, BP1, BP0) bits to define the protected area of memory (as shown in *"Table 3. Protected Area Sizes"*). The WRSR also can set or reset the Status Register Write Disable (SRWD) bit, but has no effect on bit1(WEL) and bit0 (WIP) of the status register.

In SPI, CS# must go high exactly at the 8 bits or 16 bits data boundary; In DOPI, CS# must go high while clock is low; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Figure 22. Write Status Register (WRSR) Sequence (SPI Mode)



Note : The CS# must go high exactly at 8 bits or 16 bits data boundary to completed the write register command.

Figure 23. Write Status Register (WRSR) Sequence (STR-OPI Mode)

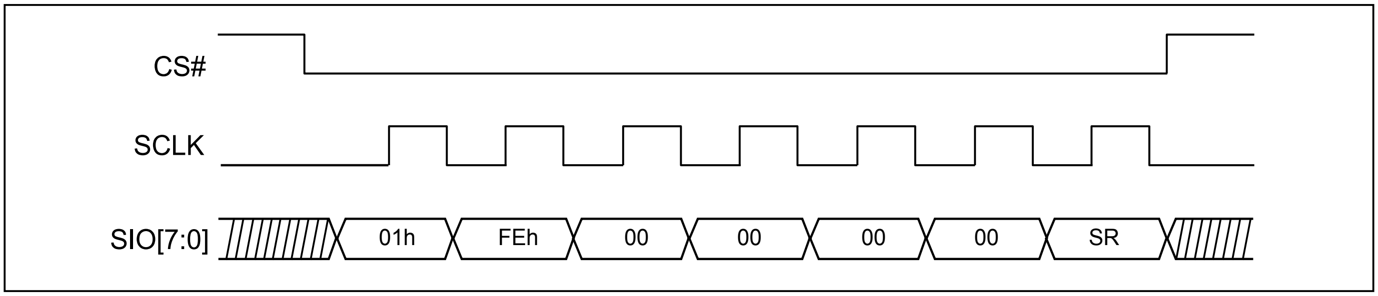
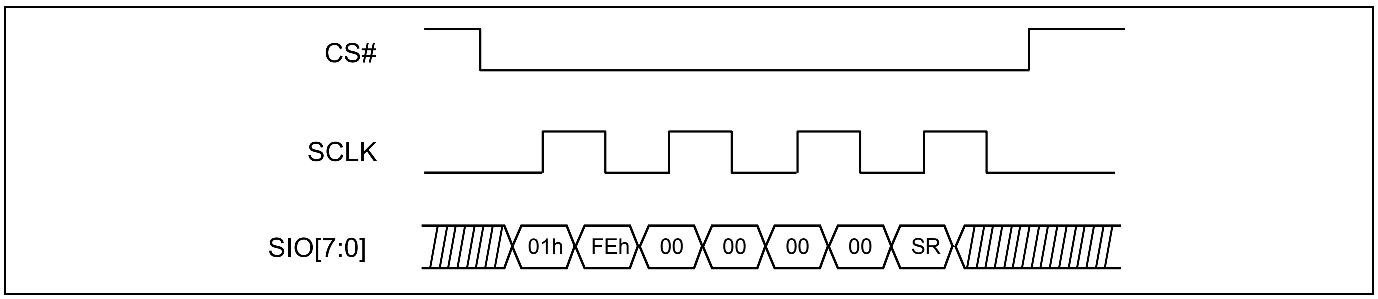


Figure 24. Write Status Register (WRSR) Sequence (DTR-OPI Mode)



Note: CS# must go high while SCLK is low.

Figure 25. Write Configuration Register (WRCR) Sequence (STR-OPI Mode)

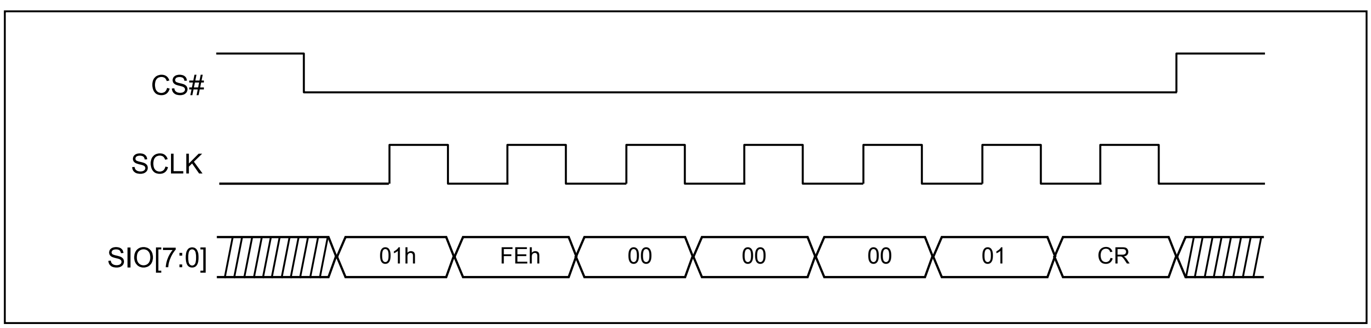
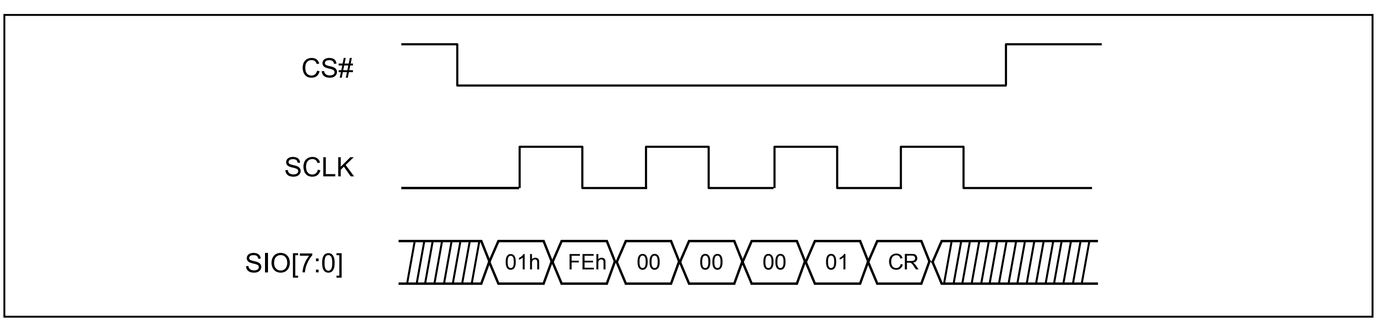
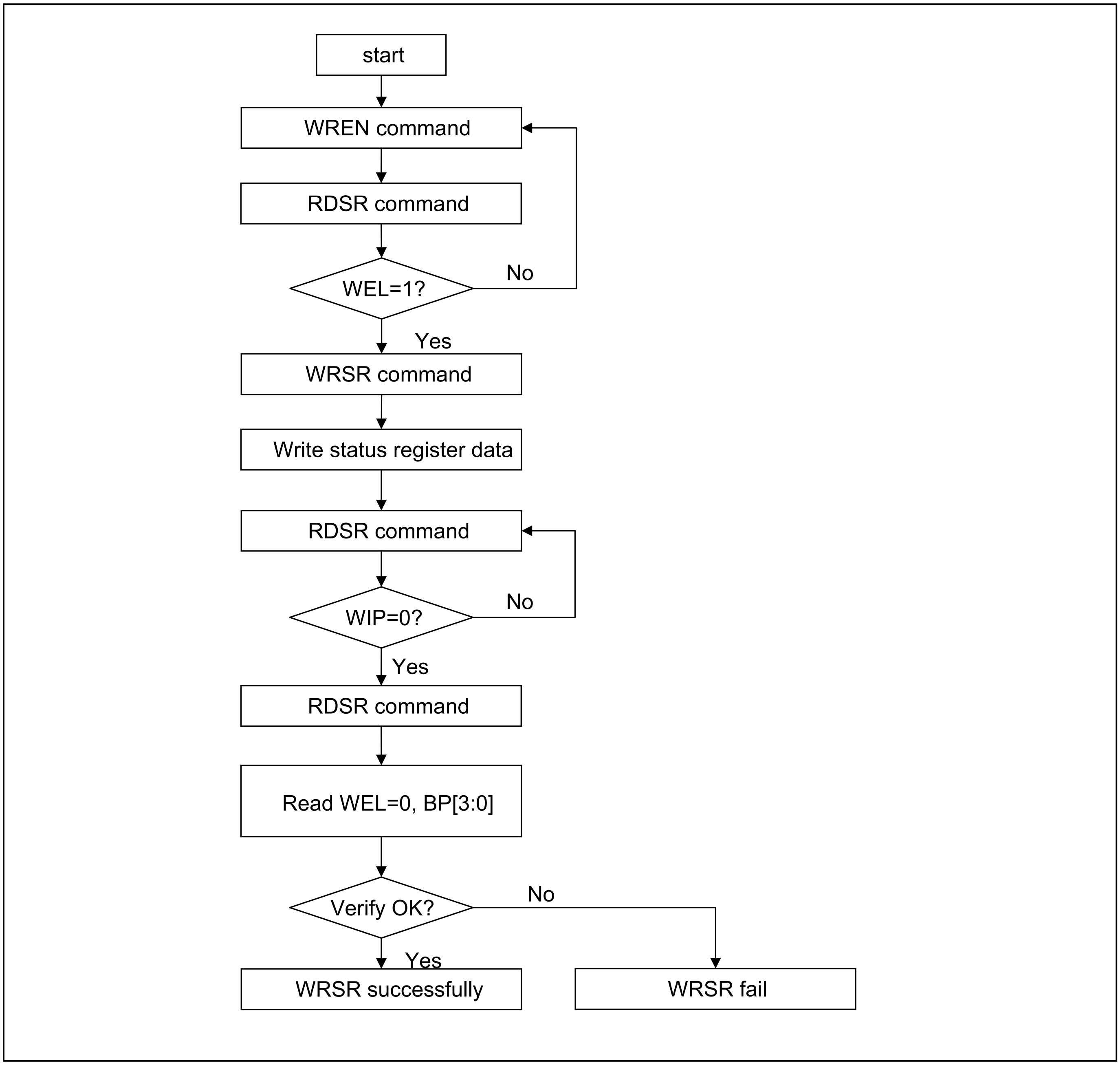


Figure 26. Write Configuration Register (WRCR) Sequence (DTR-OPI Mode)



Note: CS# must go high while SCLK is low.

Figure 27. WRSR flow

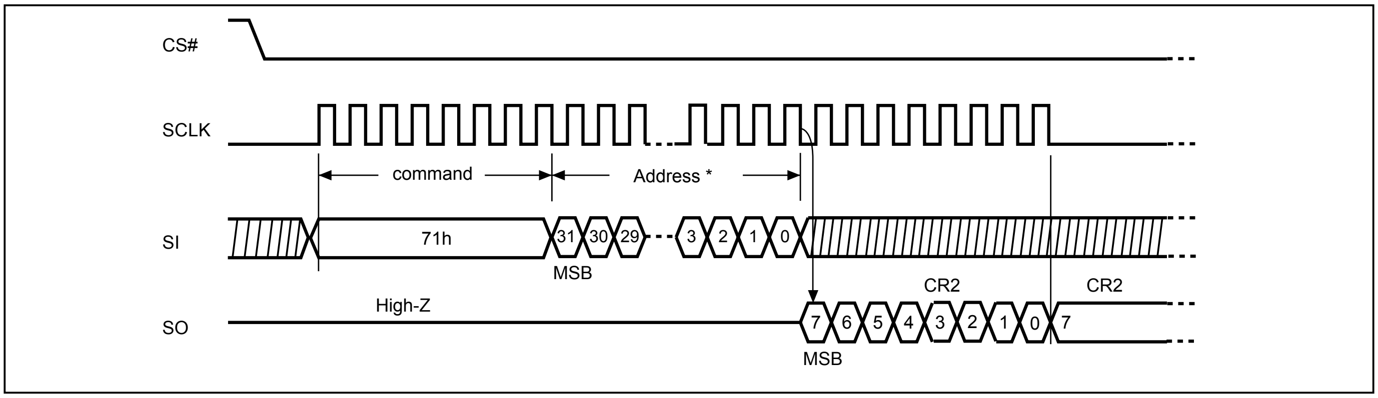


10-7. Read Configuration Register 2 (RDCR2)

The RDCR2 instruction is for reading Configuration Register 2. The Read Configuration Register 2 command would be rejected while Internal write operation is in progress (WIP=1).

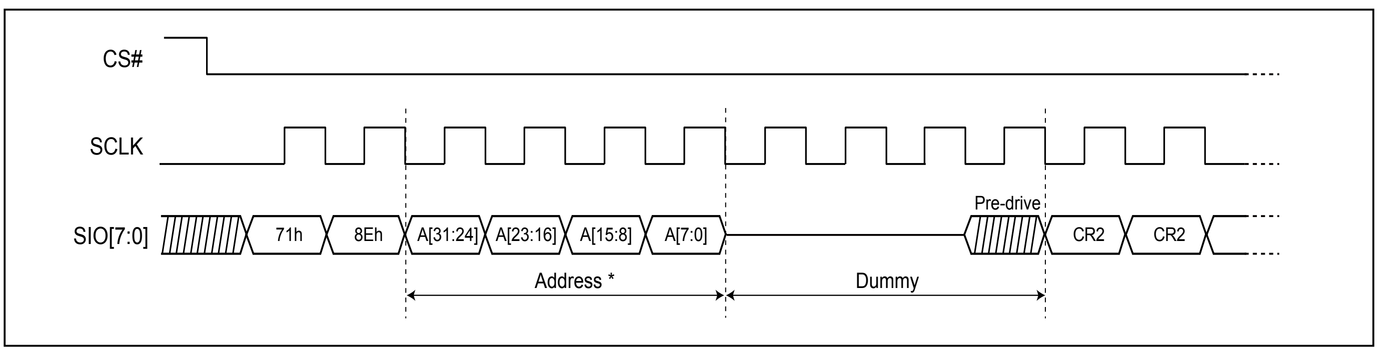
The sequence of issuing RDCR2 instruction is: CS# goes low→ sending RDCR2 instruction code→ Sending 4 byte address → Configuration Register 2 data out on SO.

Figure 28. Read Configuration Register 2 (RDCR2) Sequence (SPI Mode)



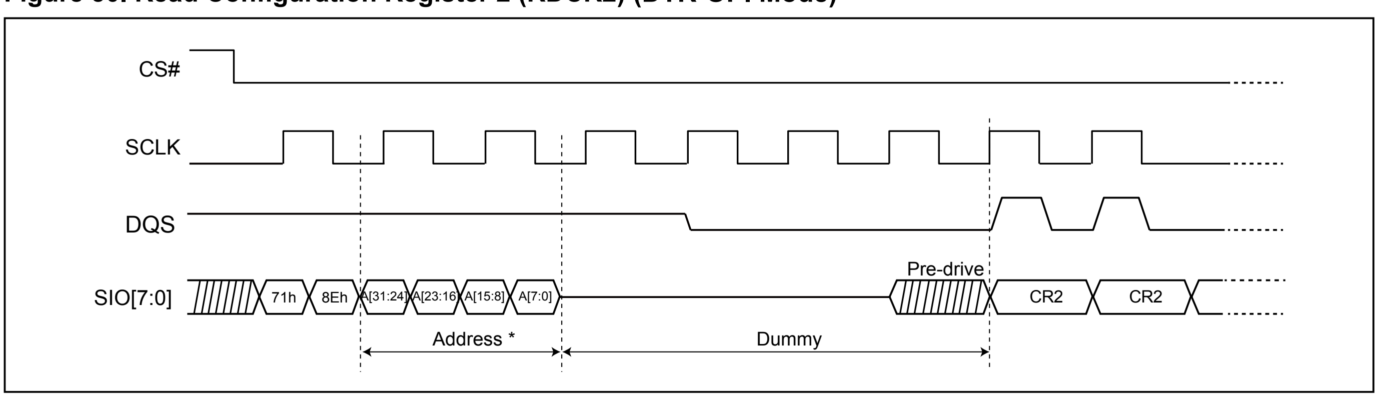
Note: * See "9-3. Configuration Register 2" for defining address .

Figure 29. Read Configuration Register 2 (RDCR2) Sequence (STR-OPI Mode)



Note: * See "9-3. Configuration Register 2" for defining address .

Figure 30. Read Configuration Register 2 (RDCR2) (DTR-OPI Mode)



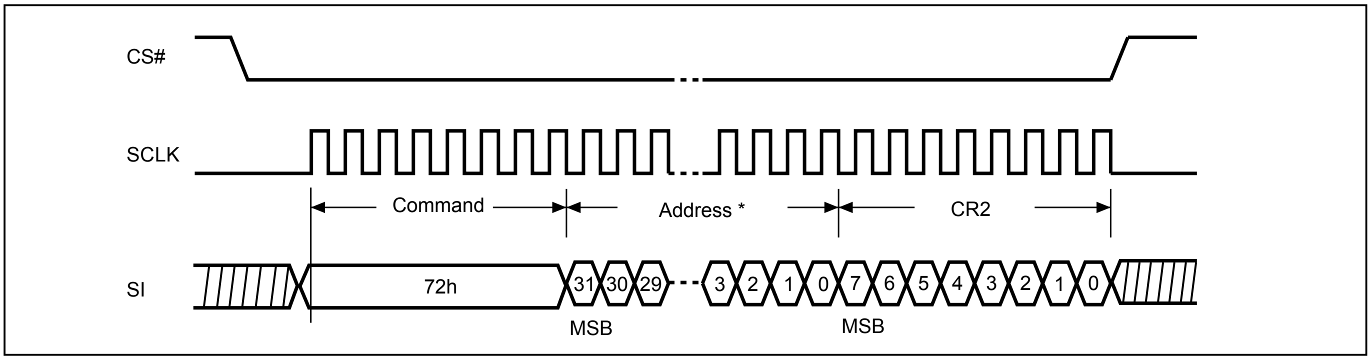
Note: * See "9-3. Configuration Register 2" for defining address .

10-8. Write Configuration Register 2 (WRCR2)

The WRCR2 instruction is for changing the values of Configuration Register 2. Before sending WRCR2 instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance.

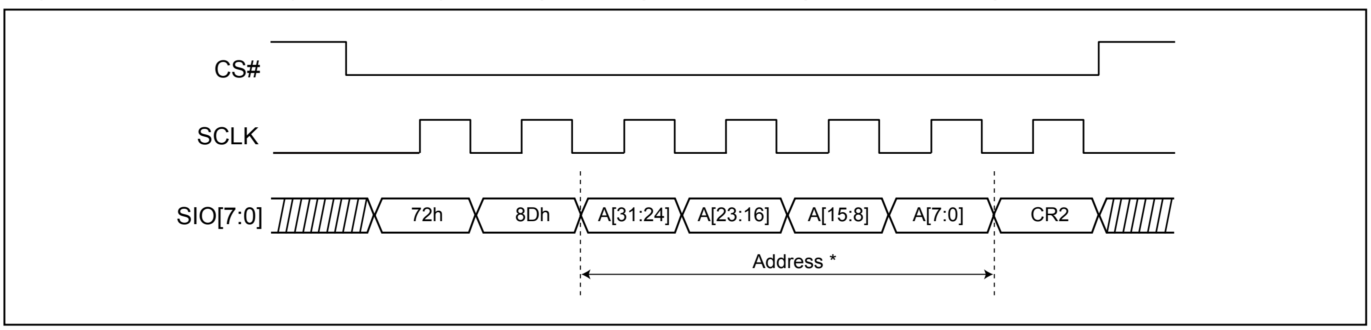
In SPI, CS# must go high exactly at the 8 bits data boundary; In DOPI, CS# must go high while clock is low; otherwise, the instruction will be rejected and not executed, and the Write Enable Latch (WEL) bit is reset.

Figure 31. Write Configuration Register 2 (WRCR2) Sequence (SPI Mode)



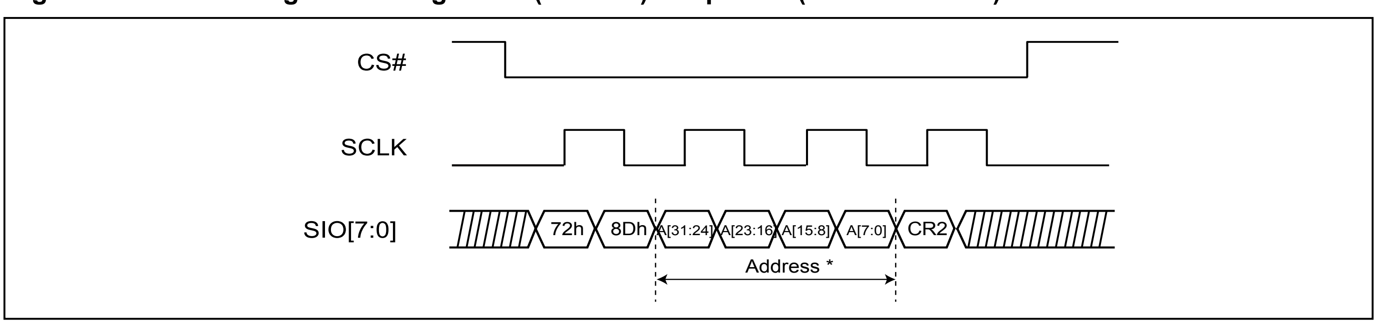
Note 1: * See *"9-3. Configuration Register 2"* for defining address .

Figure 32. Write Configuration Register 2 (WRCR2) Sequence (STR-OPI Mode)



Note 1: * See *"9-3. Configuration Register 2"* for defining address .

Figure 33. Write Configuration Register 2 (WRCR2) Sequence (DTR-OPI Mode)



Note 1 : * See *"9-3. Configuration Register 2"* for defining address.
Note 2 : CS# must go high while SCLK is low

10-9. Read Security Register (RDSCUR)

The RDSCUR instruction is for reading the value of Security Register bits. The Read Security Register can be read at any time (even in program/erase/write status register/write security register condition) and continuously.

The sequence of issuing RDSCUR instruction is : CS# goes low→sending RDSCUR instruction→Security Register data out on SO→ CS# goes high.

Figure 34. Read Security Register (RDSCUR) Sequence (SPI Mode)

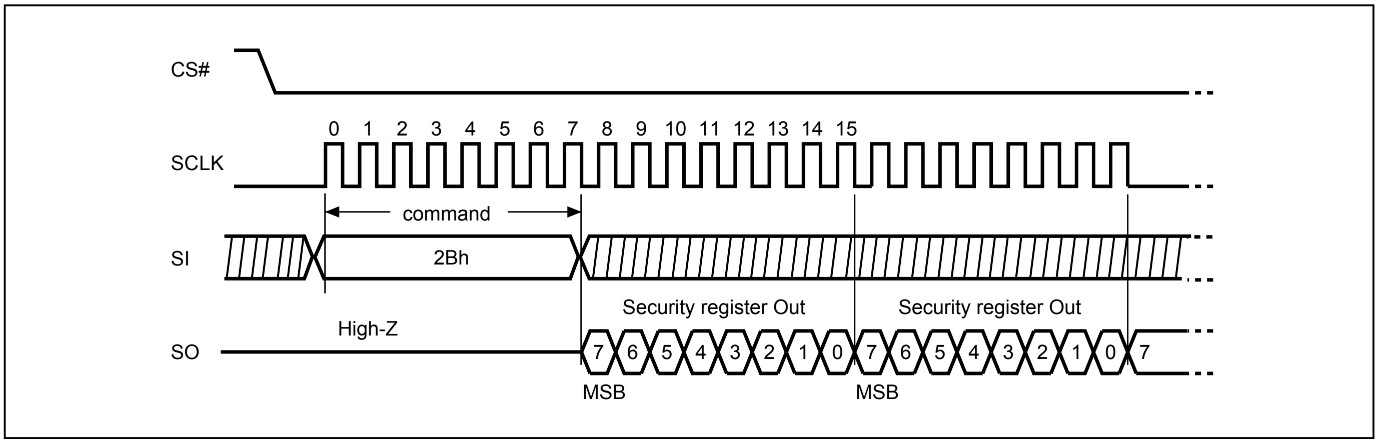


Figure 35. Read Security Register (RDSCUR) Sequence (STR-OPI Mode)

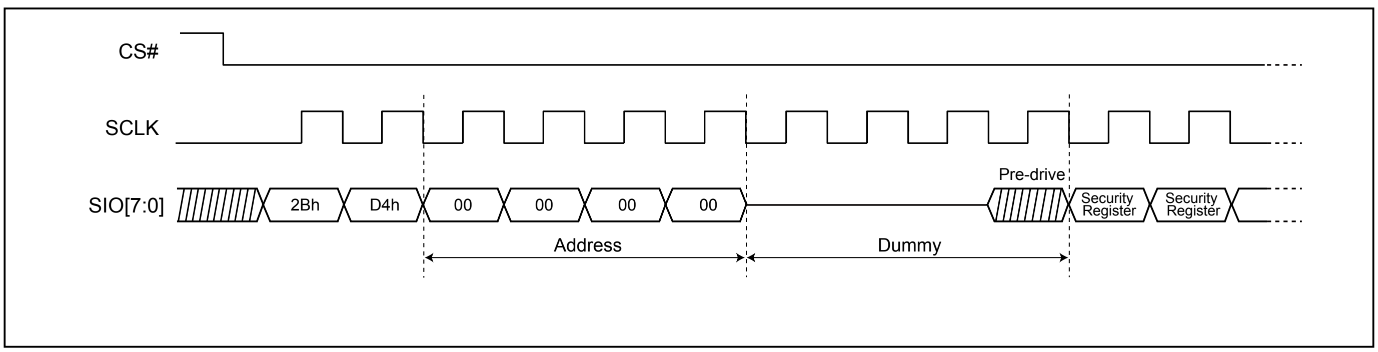
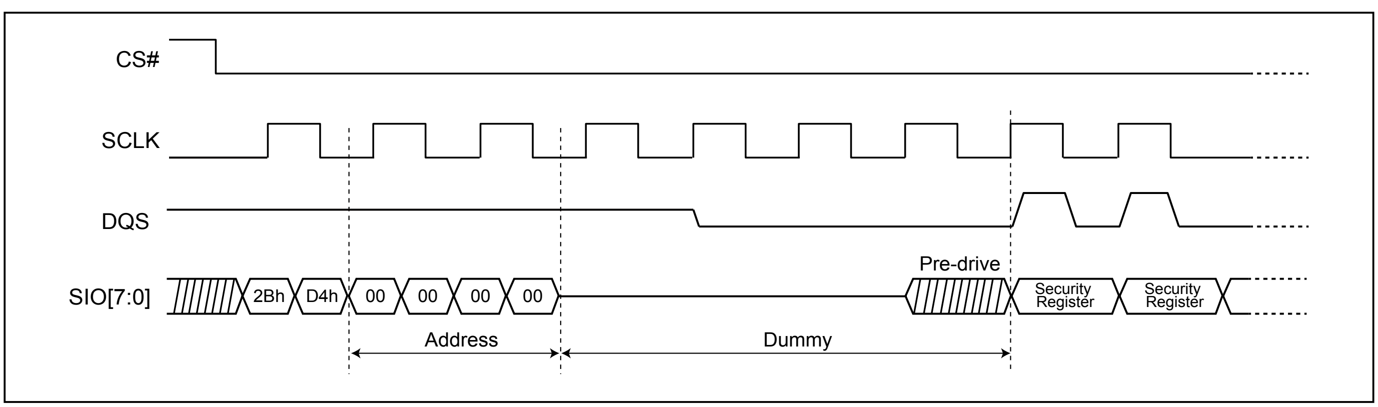


Figure 36. Read Security Register (RDSCUR) Sequence (DTR-OPI Mode)



10-10. Write Security Register (WRSCUR)

The WRSCUR instruction sets the LDSO bit of the Security Register. The WREN (Write Enable) instruction is required before issuing WRSCUR instruction. The WRSCUR instruction may change the values of bit1 (LDSO bit) for customer to lock-down the 8K-bit Secured OTP area. Once the LDSO bit is set to "1", the Secured OTP area cannot be updated any more.

The sequence of issuing WRSCUR instruction is :CS# goes low→ sending WRSCUR instruction → CS# goes high.

The CS# must go high exactly at the boundary; otherwise, the instruction will be rejected and not executed.

Figure 37. Write Security Register (WRSCUR) Sequence (SPI Mode)

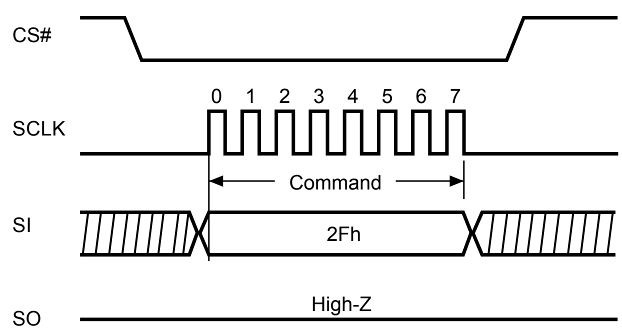


Figure 38. Write Security Register (WRSCUR) Sequence (STR-OPI Mode)

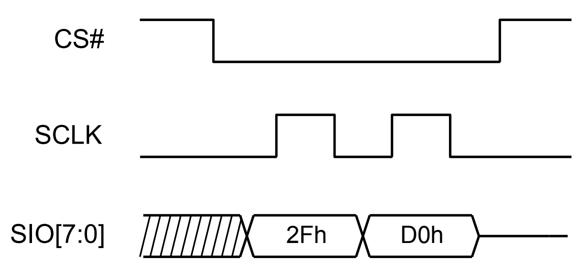
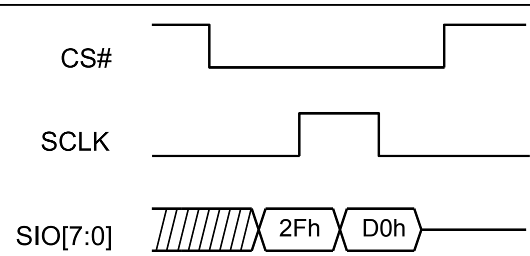


Figure 39. Write Security Register (WRSCUR) Sequence (DTR-OPI Mode)

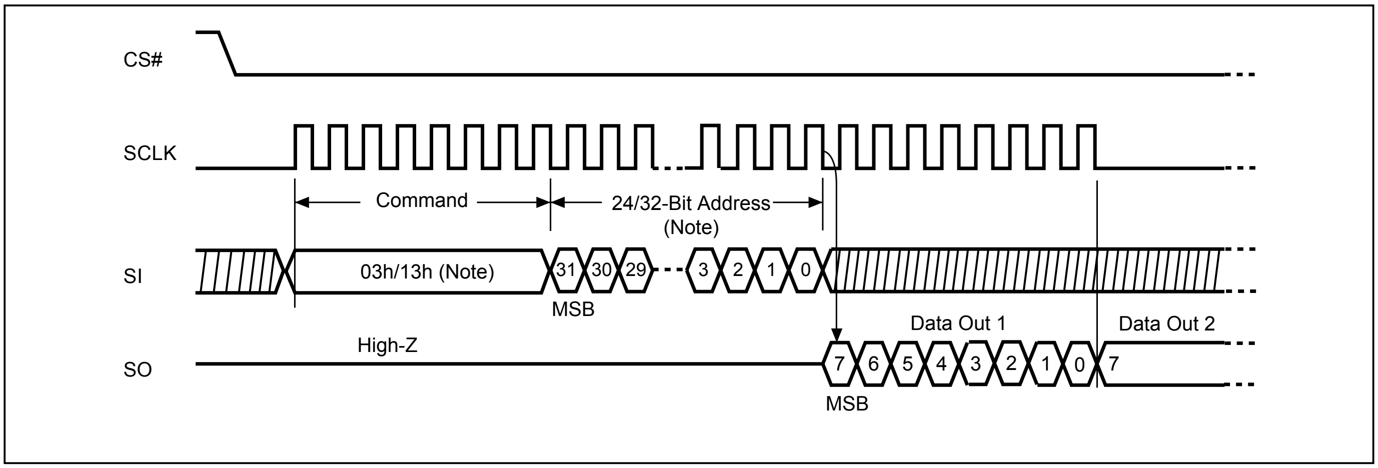


10-11.Read Data Bytes (READ/READ3B/READ4B)

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency fR. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ/READ3B/READ4B instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing READ/READ3B/READ4B instruction is: CS# goes low→sending READ/READ3B/READ4B instruction code→ 3-byte or 4-byte address on SI→ data out on SO→to end READ/READ3B/READ4B operation can use CS# to high at any time during data out.

Figure 40. Read Data Bytes (READ/READ3B/READ4B) Sequence (SPI Mode only)



Note: The number of address cycles are based on different address mode. In 3-Byte command operation, it is 24-bit. In 4-Byte command operation, it is 32-bit.

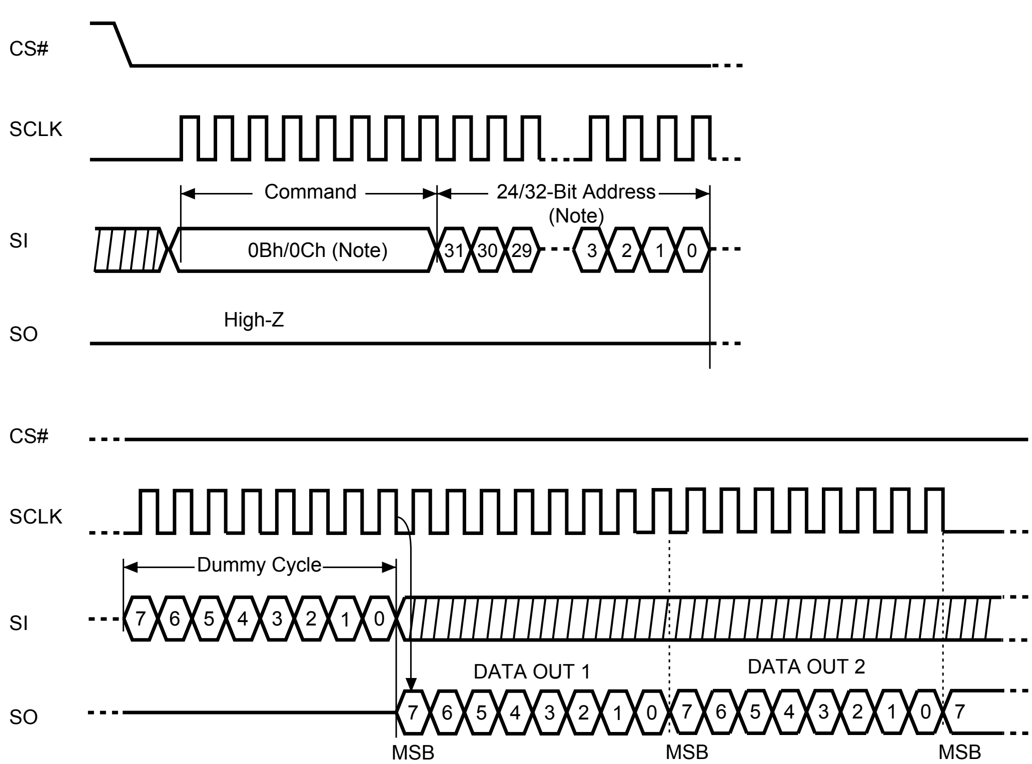
10-12. Read Data Bytes at Higher Speed (FAST_READ/FAST_READ3B/FAST_READ4B)

The FAST_READ/FAST_READ3B/FAST_READ4B instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency fC. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST_READ/FAST_READ3B/FAST_READ4B instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing FAST_READ/FAST_READ3B/FAST_READ4B instruction is: CS# goes low→ sending FAST_READ/FAST_READ3B/FAST_READ4B instruction code→ 3-byte or 4-byte address on SI→ 8 dummy cycles → data out on SO→ to end FAST_READ/FAST_READ3B/FAST_READ4B operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, FAST_READ/FAST_READ3B/FAST_READ4B instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 41. Read at Higher Speed (FAST_READ/FAST_READ3B/FAST_READ4B) Sequence (SPI Mode only)



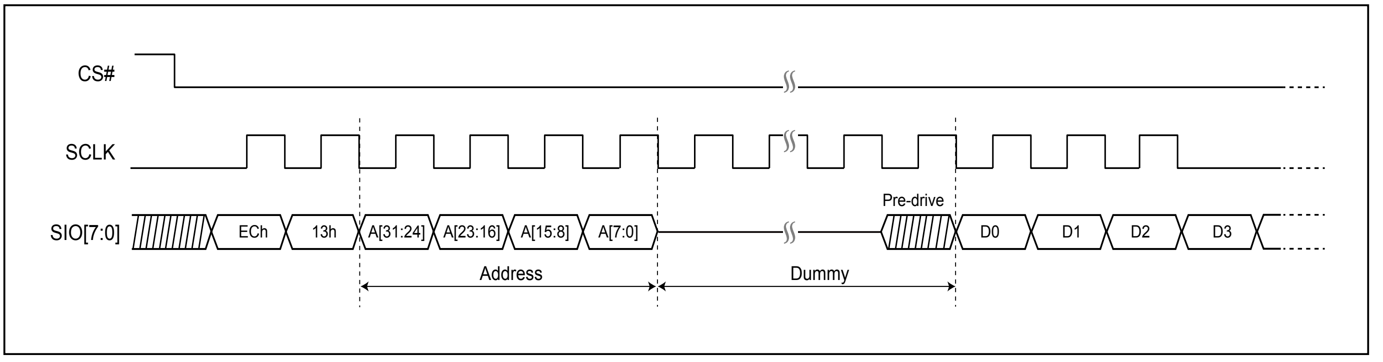
Note: The number of address cycles are based on different address mode. In 3-Byte command operation, it is 24-bit. In 4-Byte command operation, it is 32-bit.

10-13. OCTA Read Mode (8READ)

The 8READ instruction enable Octa throughput of Serial NOR Flash in read mode. An OPI Enable bit of Configuration Register 2 must be set to "1" before sending the STR Octa READ instruction.

While Program/Erase/Write Status Register cycle is in progress, 8READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 42. OCTA Read Mode Sequence (STR-OPI Mode)



10-14. OCTA DTR Read Mode (8DTRD)

The 8DTRD instruction enable DTR Octa throughput of Serial NOR Flash in read mode. An DOPI Enable bit of Configuration Register 2 must be set to "1" before sending the DTR Octa READ instruction.

While Program/Erase/Write Status Register cycle is in progress, 8DTRD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

In DTR Octa READ mode, the starting address must be even byte (A0=0).

Figure 43. OCTA Read Mode Sequence (DTR-OPI Mode)

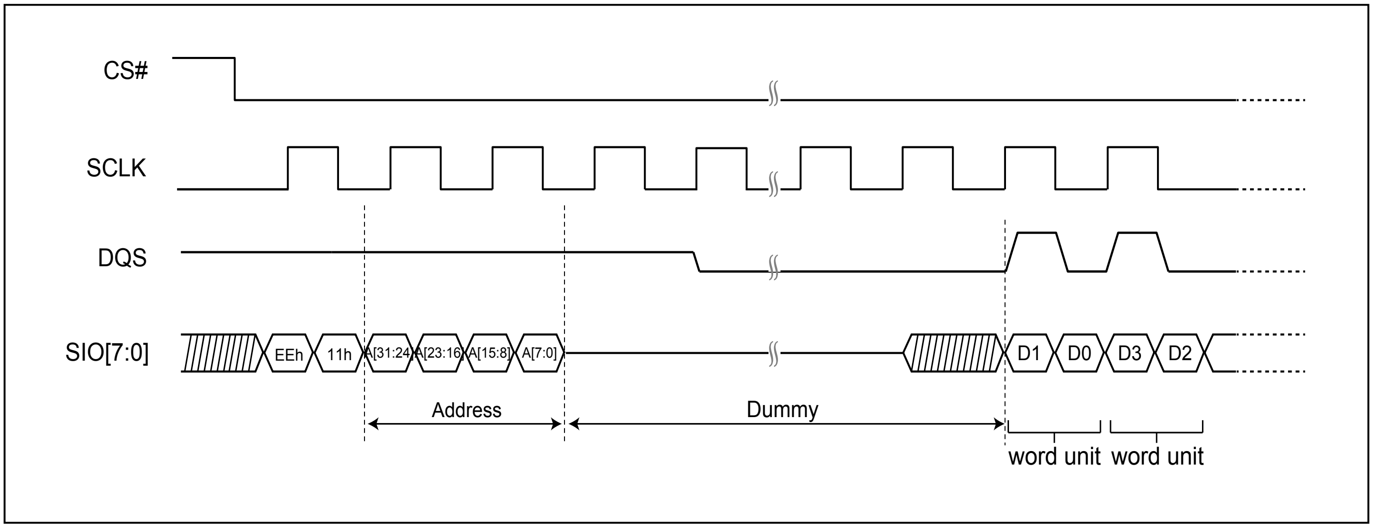
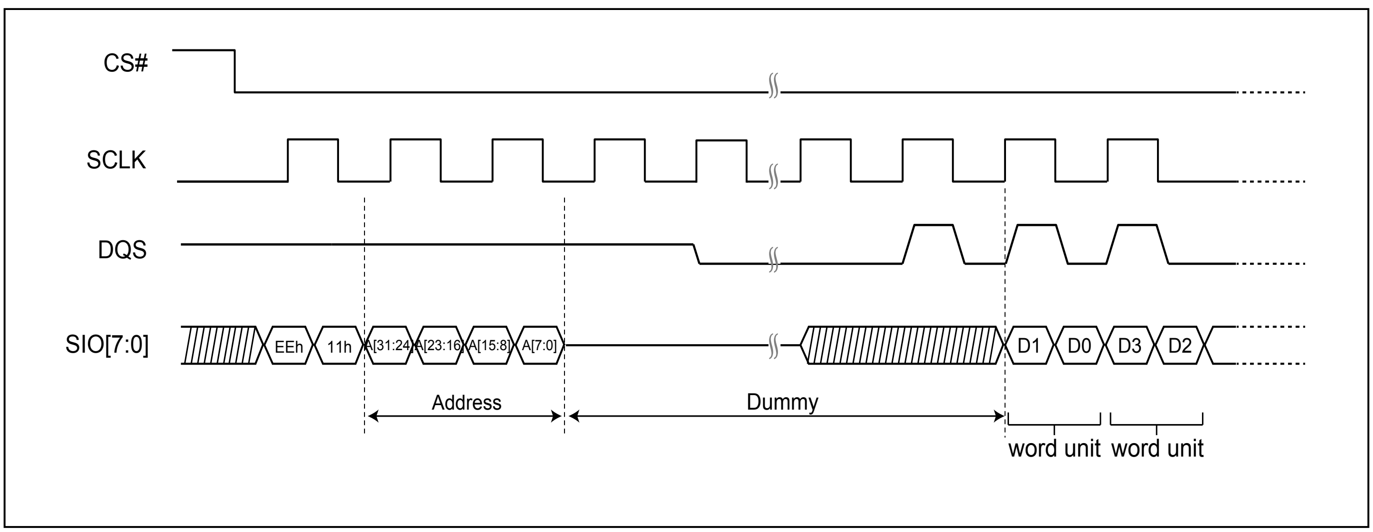


Figure 44. OCTA Read Mode Sequence (DTR-OPI Mode) with DQS pre-cycle enabled (CR2 DQSPRC=1)



10-15. Preamble Bit

The Preamble Bit data pattern supports system/memory controller to determine the valid windows of data output more easily and improve data capture reliability while the flash memory is running in high frequency.

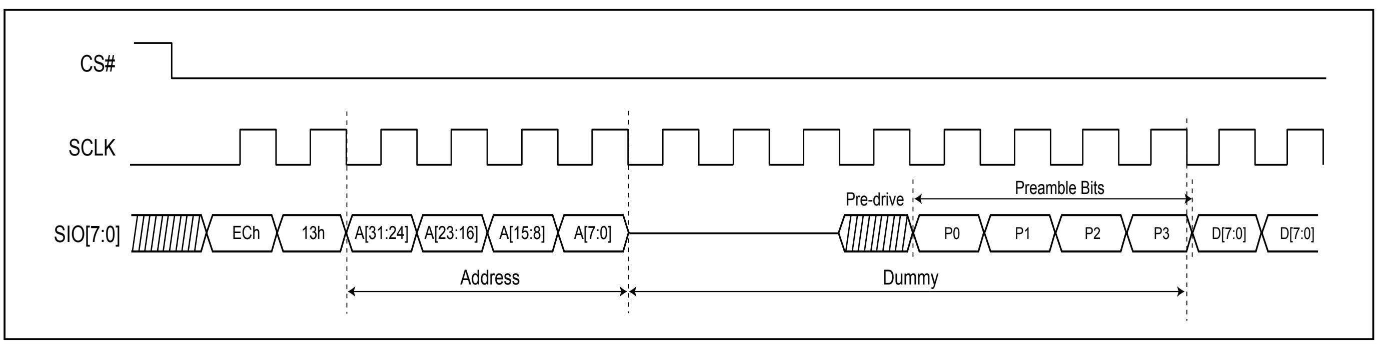
The preamble bit is designed as a 16-bit data pattern, which can be enabled or disabled by setting the bit4 of Configuration register (Preamble bit Enable bit). Once CR<4> is set, the preamble bit is inputted into dummy cycles. Two different patterns are selectable by setting CR<2> PSB (Pattern Select Bit), and please refer to *"9-3. Configuration Register 2"* for details.

Once Preamble Bit feature is enabled, the preamble bit pattern will be output after a pre-driven signal. When the device is under OPI mode, all SIO pins except SIO3 will output the same learning pattern. The signal on SIO3 will be different from other I/O pins in case PSB=0.

In OPI, when dummy cycle number reaches 20, the complete 16 bits will start to output right after the pre-driven signal. When dummy cycle number is not sufficient of 16 cycles, the rest of the preamble bits will be cut off.

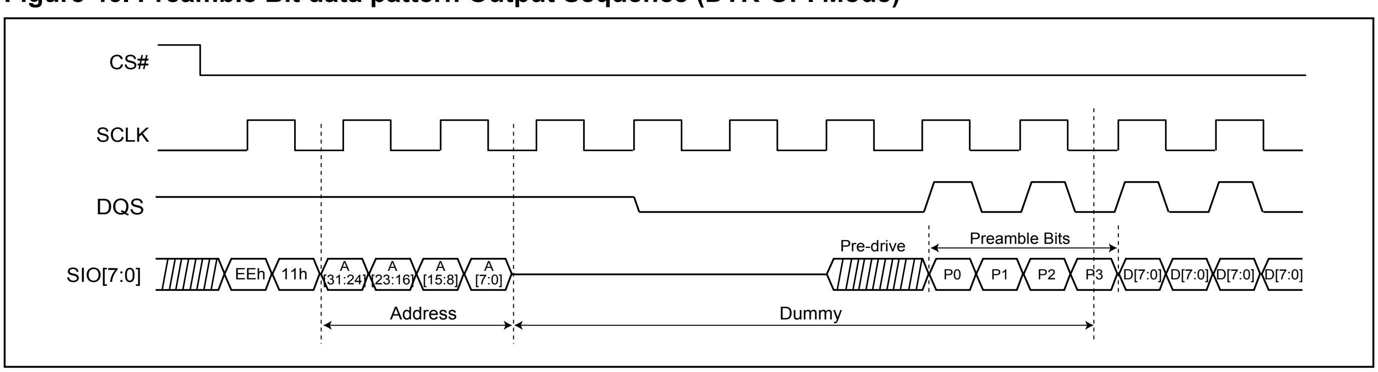
In DOPI, when dummy cycles number reaches 12, the complete 16 bits will start to output right after the pre-driven signal.

Figure 45. Preamble Bit data pattern Output Sequence (STR-OPI Mode)



Note: 8 dummy cycle example.

Figure 46. Preamble Bit data pattern Output Sequence (DTR-OPI Mode)



Note: 6 dummy cycle example.

10-16. Burst Read

To set the Burst length, following command operation is required to issue command: "C0h" in the first Byte, following clock defining wrap around register value.

Their definitions are as the following table:

Data	Wrap Around	Wrap Depth
00h	Reserved	Reserved
01h	Yes	16-byte
02h	Yes	32-byte
03h	Yes	64-byte
1xh	No	X

The wrap around unit is defined within the 256Byte page, with random initial address. It is defined as "wrap-around mode disable" for the default state of the device. To exit wrap around, it is required to issue another "C0h" command in which data='1xh". Otherwise, wrap around status will be retained until power down or reset command. To change wrap around depth, it is requried to issue another "C0h" command in which data="0xh". Burst read is supported only in OPI mode after wrap around is enable. Burst read does not support DOPI. The device is default without Burst read.

Figure 47. Set Burst Length (SPI Mode)

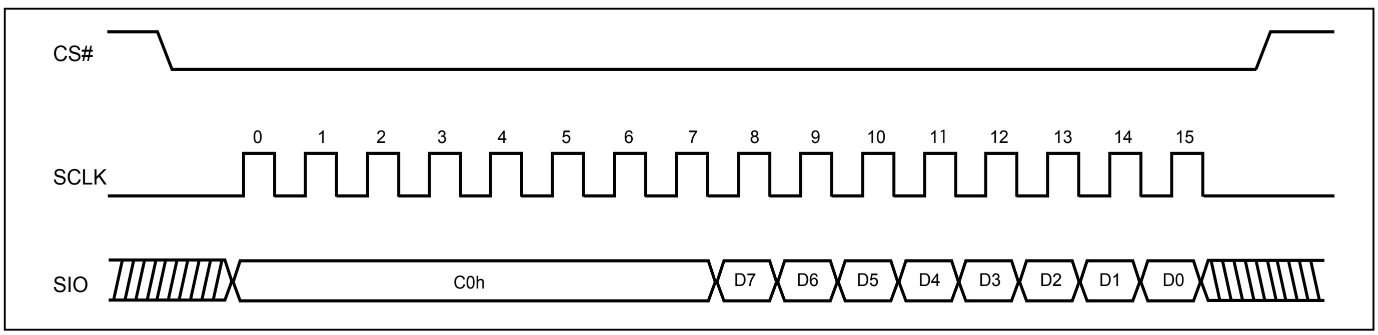
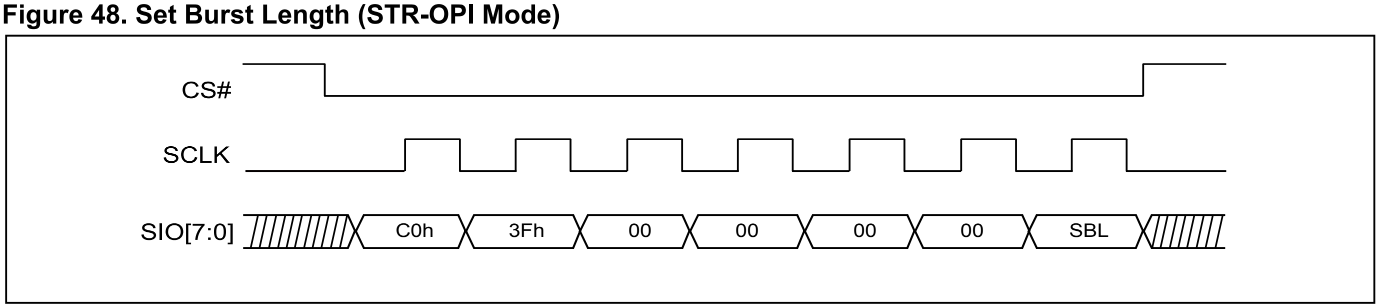


Figure 48. Set Burst Length (STR-OPI Mode)



10-17. Fast Boot

The Fast Boot Feature provides the ability to automatically execute read operation after power on cycle or reset without any read instruction.

A Fast Boot Register is provided on this device. It can enable the Fast Boot function and also define the number of delay cycles and start address (where boot code being transferred). Instruction WRFBR (write fast boot register) and ESFBR (erase fast boot register) can be used for the status configuration or alternation of the Fast Boot Register bit. RDFBR (read fast boot register) can be used to verify the program state of the Fast Boot Register. The default number of delay cycles is 21 cycles in OPI/DOPI; while the number of delay cycles is 13 in SPI and there is a 16bytes boundary address for the start of boot code access.

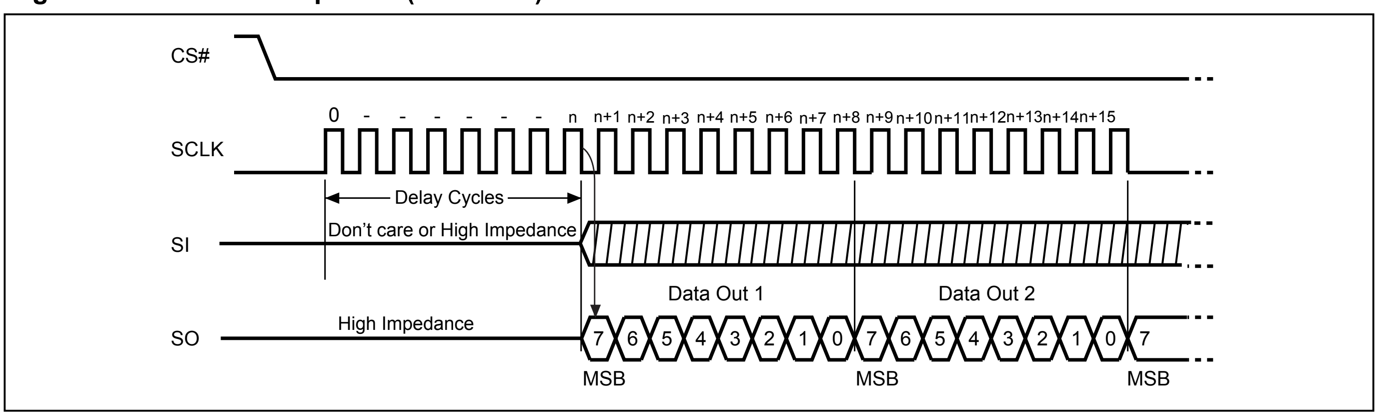
When CS# starts to go low, data begins to output from default address after the delay cycles. After CS# returns to go high, the device will go back to standard SPI/OPI/DOPI mode and user can start to input command. In the fast boot data out process from CS# goes low to CS# goes high, a minimum of one byte must be output.

Once Fast Boot feature has been enabled, the device will automatically start a read operation after power on cycle, reset command, or hardware reset operation.

Fast Boot Register (FBR)

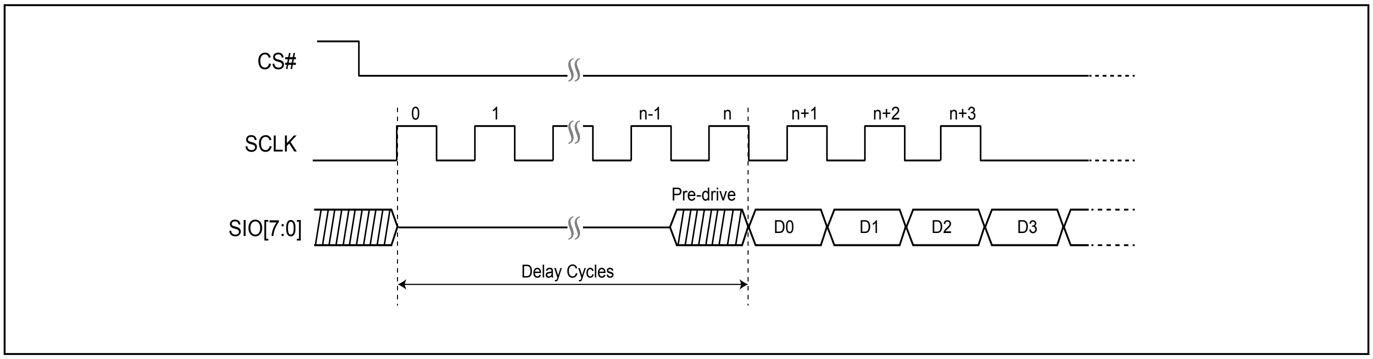
Bits	Description	Bit Status	Default State	Type
31 to 4	FBSA (FastBoot Start Address)	16 bytes boundary address for the start of boot code access.	FFFFFFF	Non-Volatile
3	Reserved		1	Non-Volatile
2 to 1	FBSD (FastBoot Start Delay Cycle)	00: 11 delay cycles 01: 15 delay cycles 10: 17 delay cycles 11: 21 delay cycles	11	Non-Volatile
0	FBE (FastBoot Enable)	0=FastBoot is enabled. 1=FastBoot is not enabled.	1	Non-Volatile

Figure 49. Fast Boot Sequence (SPI Mode)



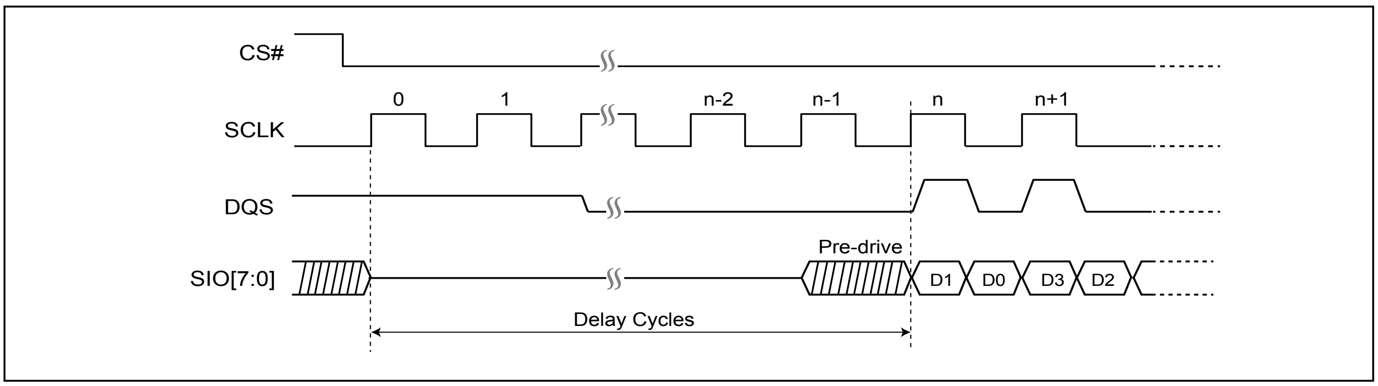
Note: The delay cycle is always 13 in SPI mode.

Figure 50. Fast Boot Sequence (STR-OPI Mode)



Note: If FBSD = 11, delay cycles is 21 and n is 20.
If FBSD = 10, delay cycles is 17 and n is 16.
If FBSD = 01, delay cycles is 15 and n is 14.
If FBSD = 00, delay cycles is 11 and n is 10.

Figure 51. Fast Boot Sequence (DTR-OPI Mode)



Note: If FBSD = 11, delay cycles is 21 and n is 21.
If FBSD = 10, delay cycles is 17 and n is 17.
If FBSD = 01, delay cycles is 15 and n is 15.
If FBSD = 00, delay cycles is 11 and n is 11.

Figure 52. Read Fast Boot Register (RDFBR) Sequence

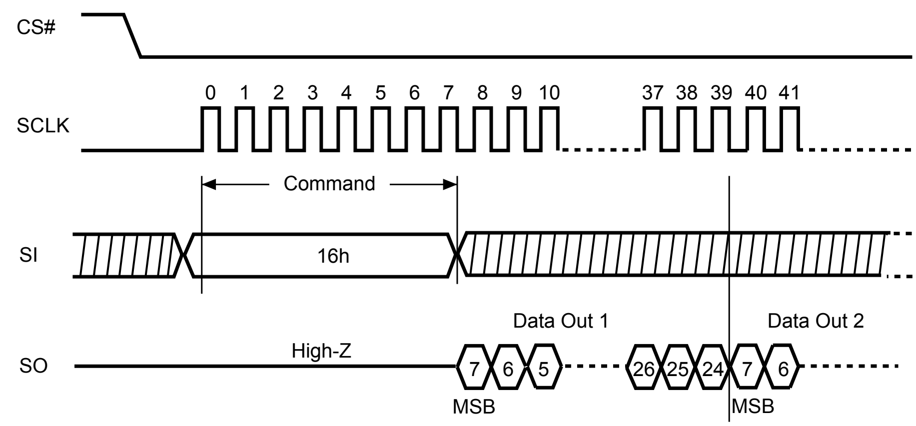


Figure 53. Read Fast Boot Register (RDFBR) Sequence (STR-OPI Mode)

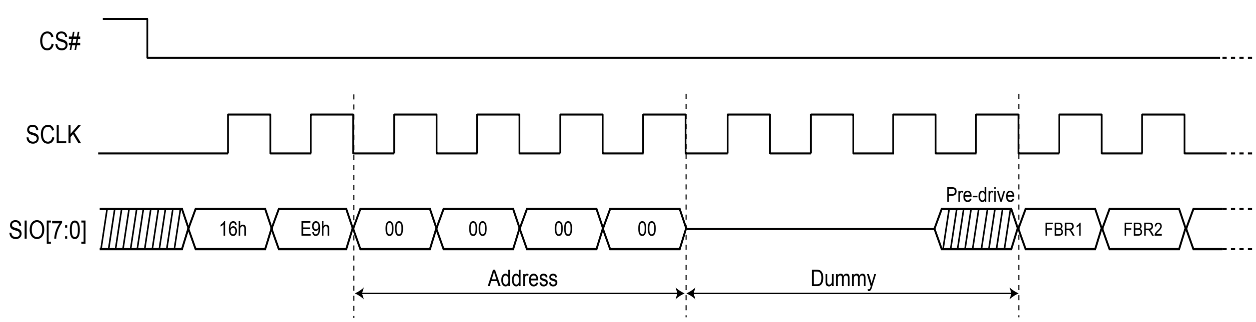


Figure 54. Read Fast Boot Register (RDFBR) Sequence (DTR-OPI Mode)

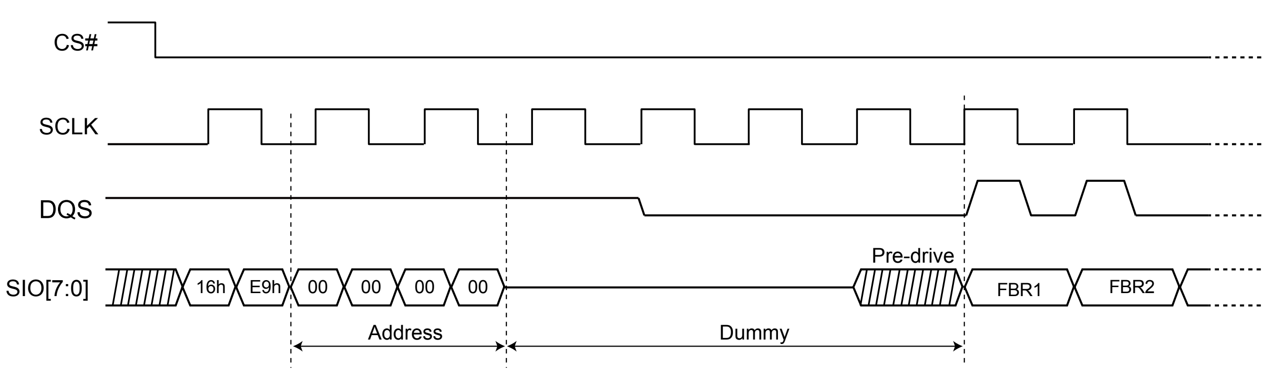


Figure 55. Write Fast Boot Register (WRFBR) Sequence

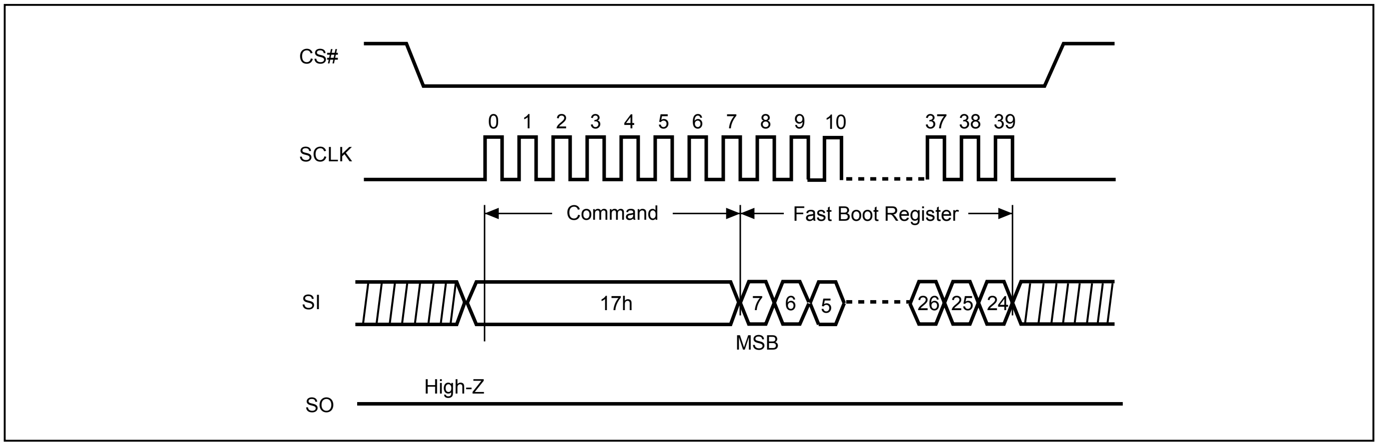


Figure 56. Write Fast Boot Register (WRFBR) Sequence (STR-OPI Mode)

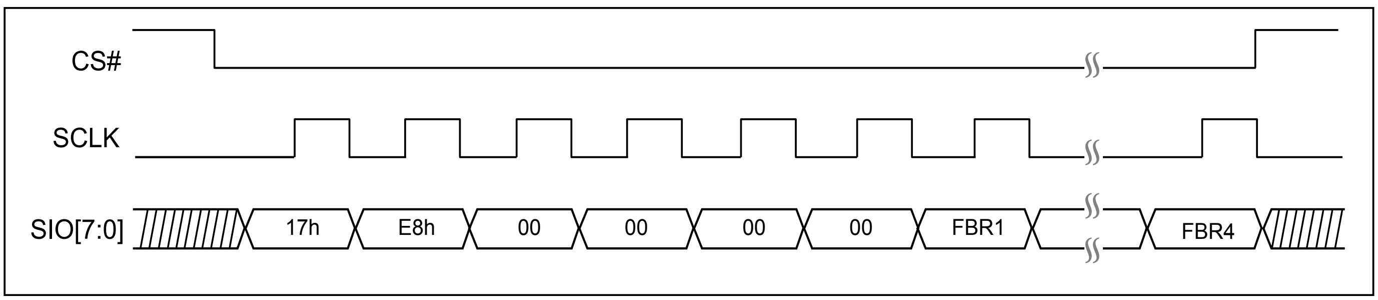


Figure 57. Write Fast Boot Register (WRFBR) Sequence (DTR-OPI Mode)

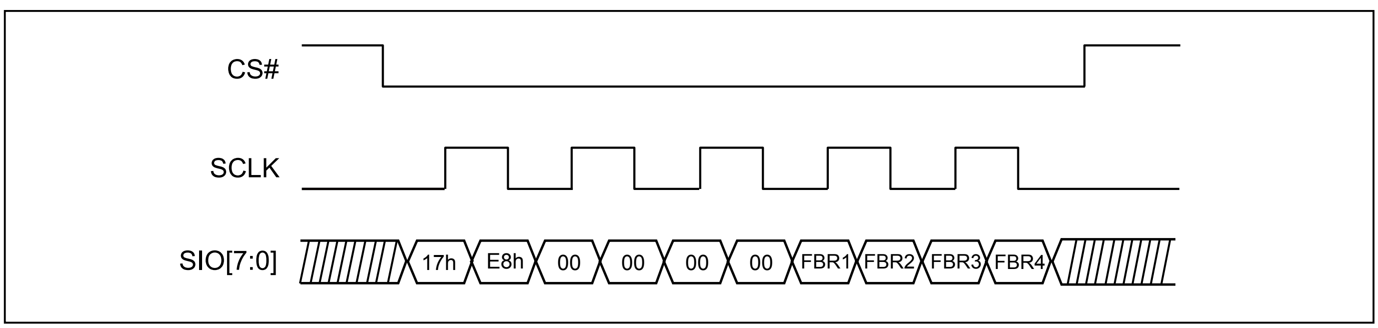


Figure 58. Erase Fast Boot Register (ESFBR) Sequence

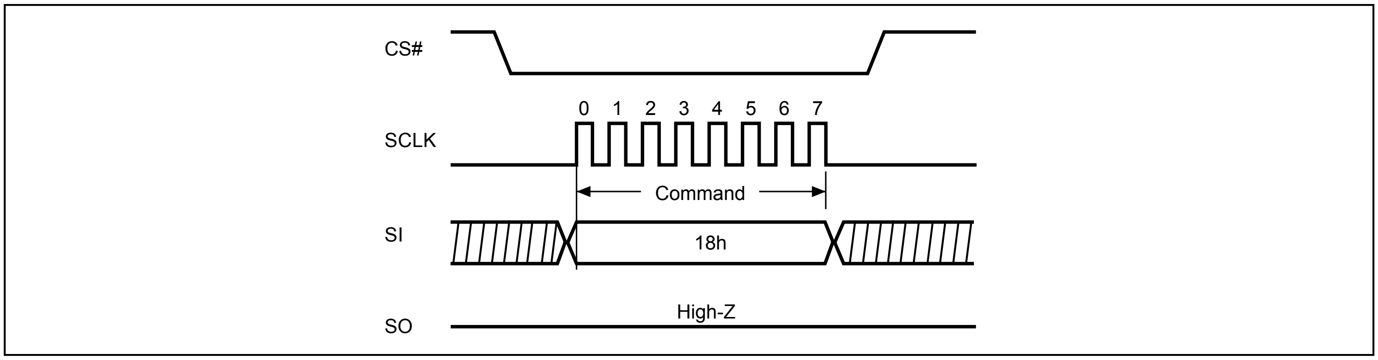


Figure 59. Erase Fast Boot Register (ESFBR) Sequence (STR-OPI Mode)

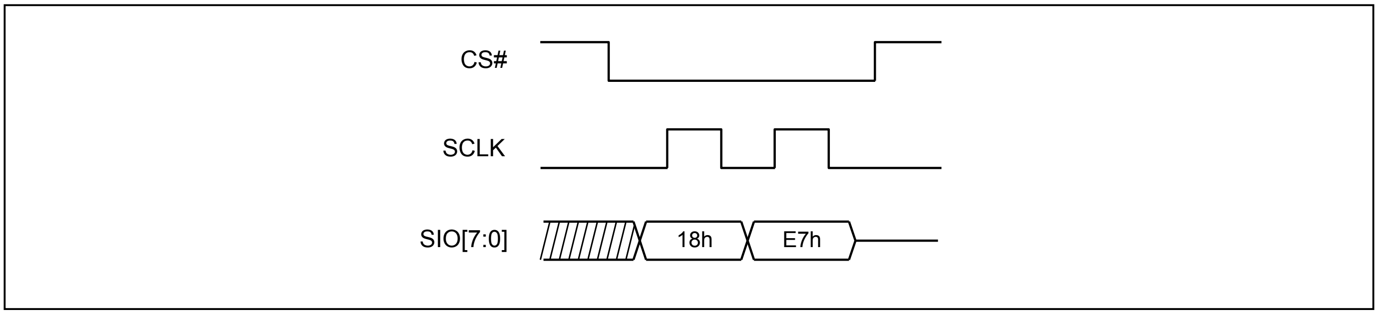
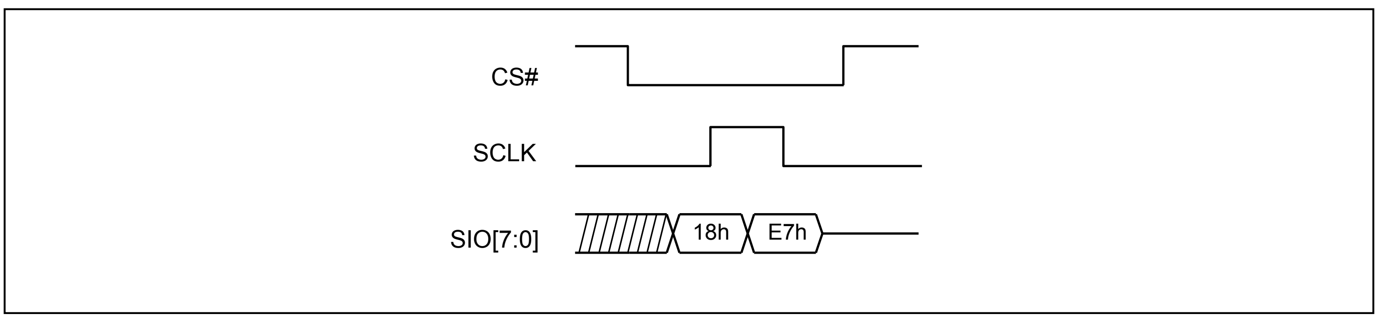


Figure 60. Erase Fast Boot Register (ESFBR) Sequence (DTR-OPI Mode)



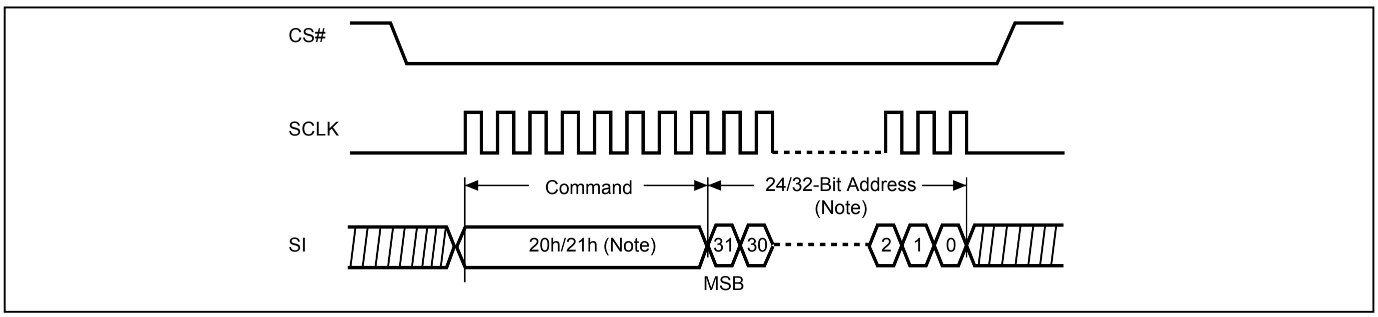
10-18. Sector Erase (SE/SE3B/SE4B)

The Sector Erase (SE/SE3B/SE4B) instruction is for erasing the data of the chosen sector to be "1". The instruction is used for any 4K-byte sector. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE/SE3B/SE4B). Any address of the sector (Please refer to *"5. MEMORY ORGANIZATION"*) is a valid address for Sector Erase (SE/SE3B/SE4B) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of the address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing SE/SE3B/SE4B instruction is: CS# goes low→ sending SE/SE3B/SE4B instruction code→ 3-byte or 4-byte address → CS# goes high.

The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Sector Erase cycle is in progress. The WIP sets 1 during the tSE timing, and clears when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the Block is protected by BP bits (Block Protect Mode), the Sector Erase (SE/SE3B/SE4B) instruction will not be executed on the block.

Figure 61. Sector Erase (SE/SE3B/SE4B) Sequence (SPI Mode)



Note: The number of address cycles are based on different address mode. In 3-Byte command operation, it is 24-bit. In 4-Byte command operation, it is 32-bit.

Figure 62. Sector Erase (SE) Sequence (STR-OPI Mode)

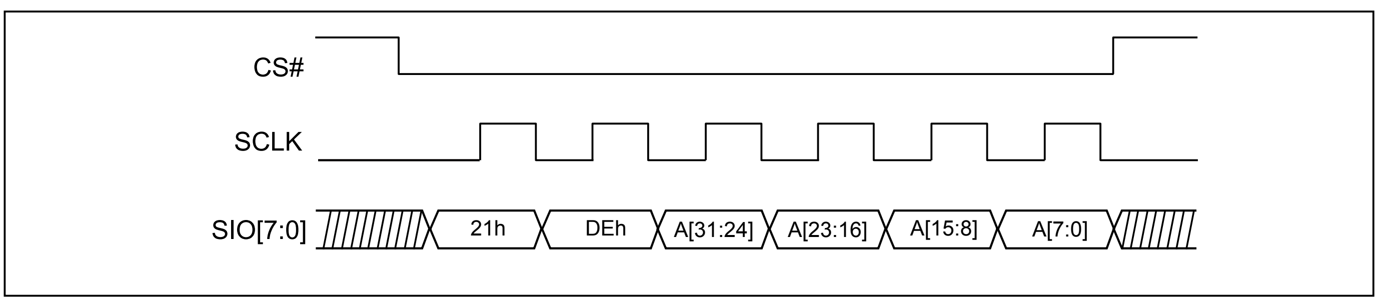
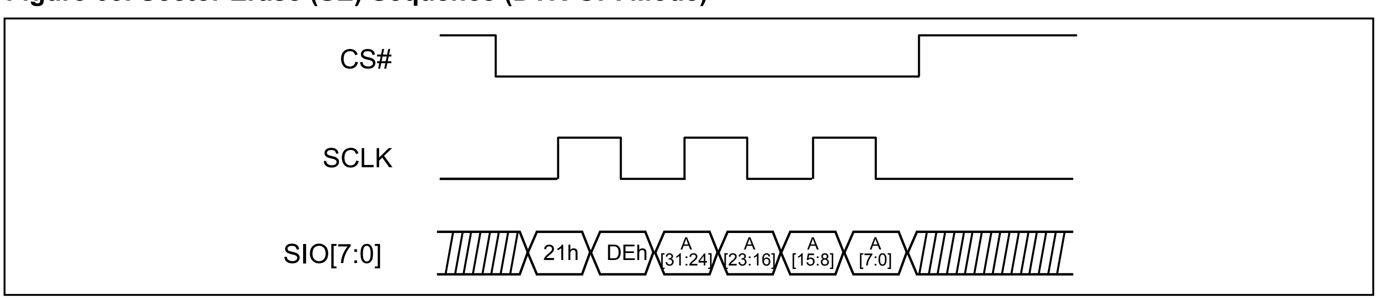


Figure 63. Sector Erase (SE) Sequence (DTR-OPI Mode)



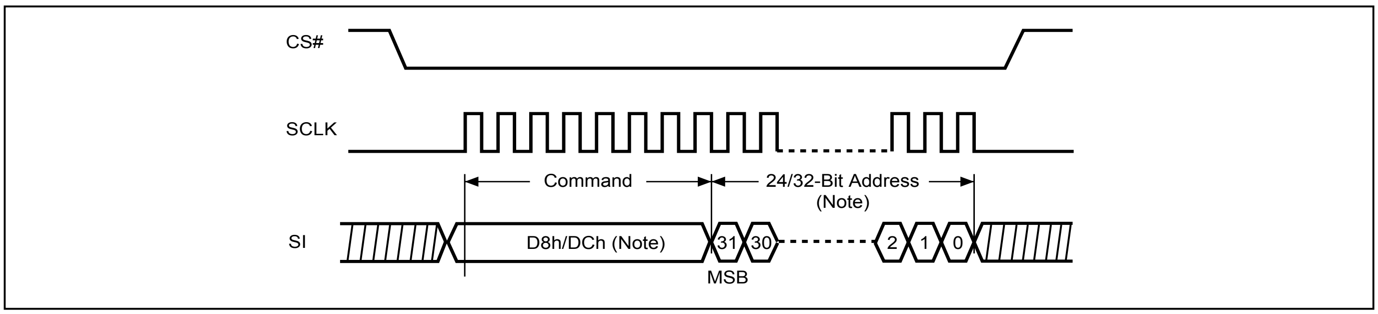
10-19. Block Erase (BE/BE3B/BE4B)

The Block Erase (BE/BE3B/BE4B) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 64K-byte block erase operation. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE/BE3B/BE4B). Any address of the block (Please refer to *"5. MEMORY ORGANIZATION"*) is a valid address for Block Erase (BE/BE3B/BE4B) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE/BE3B/BE4B instruction is: CS# goes low→ sending BE/BE3B/BE4B instruction code→ 3-byte or 4-byte address → CS# goes high.

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Block Erase cycle is in progress. The WIP sets during the tBE timing, and clears when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the Block is protected by BP bits (Block Protect Mode), the Block Erase (BE/BE3B/BE4B) instruction will not be executed on the block.

Figure 64. Block Erase (BE/BE3B/BE4B) Sequence (SPI Mode)



Note: The number of address cycles are based on different address mode. In 3-Byte command operation, it is 24-bit. In 4-Byte command operation, it is 32-bit.

Figure 65. Block Erase (BE) Sequence (STR-OPI Mode)

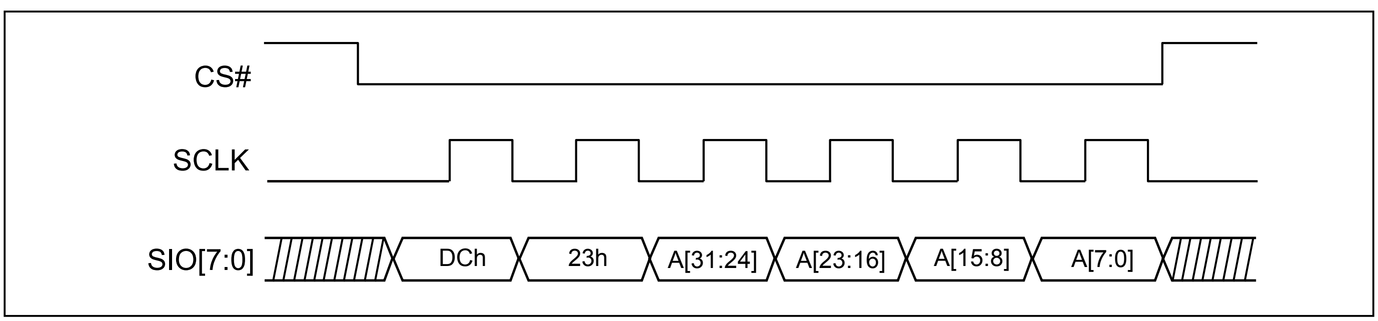
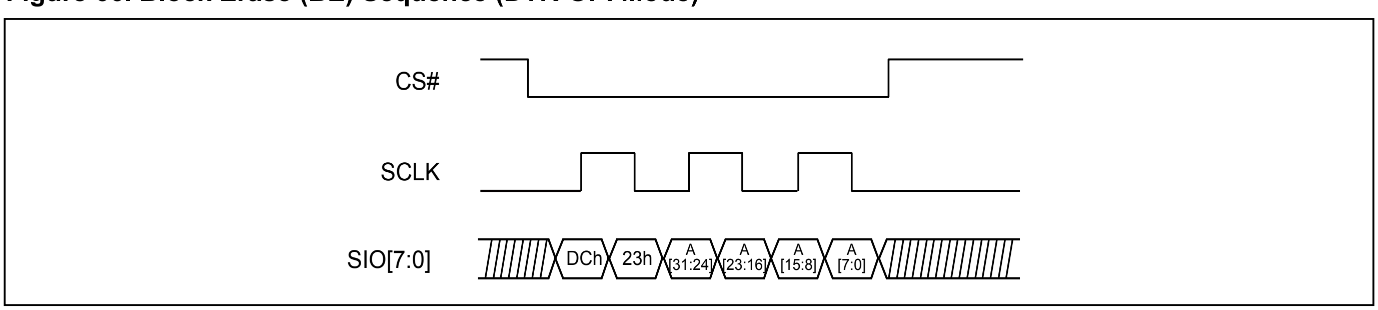


Figure 66. Block Erase (BE) Sequence (DTR-OPI Mode)



10-20. Chip Erase (CE)

The Chip Erase (CE) instruction is for erasing the data of the whole chip to be "1". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). The CS# must go high exactly at the byte boundary, otherwise the instruction will be rejected and not executed.

The sequence of issuing CE instruction is: CS# goes low→sending CE instruction code→CS# goes high.

The self-timed Chip Erase Cycle time (tCE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Chip Erase cycle is in progress. The WIP sets during the tCE timing, and clears when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared.

When the chip is under "Block protect (BP) Mode". The Chip Erase (CE) instruction will not be executed, if one (or more) sector is protected by BP3-BP0 bits. It will be only executed when BP3-BP0 all set to "0".

Figure 67. Chip Erase (CE) Sequence (SPI Mode)

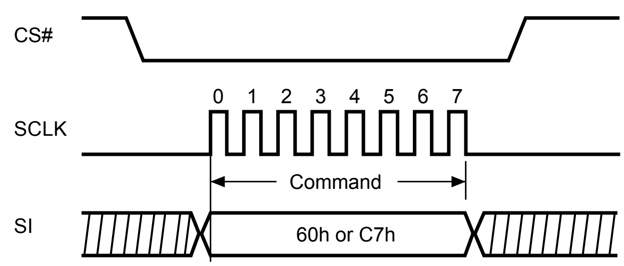


Figure 68. Chip Erase (CE) Sequence (STR-OPI Mode)

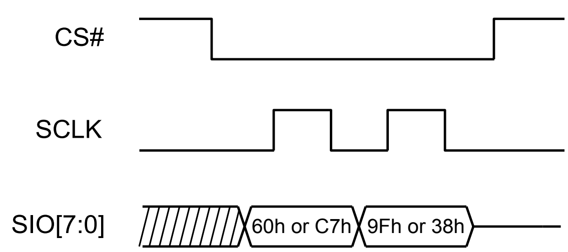
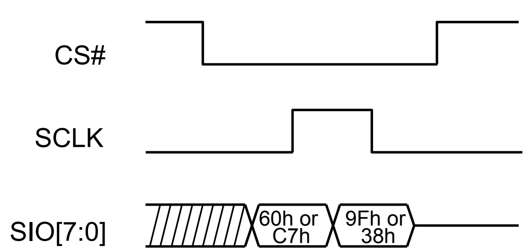


Figure 69. Chip Erase (CE) Sequence (DTR-OPI Mode)



10-21. Page Program (PP/PP3B/PP4B)

The Page Program (PP/PP3B/PP4B) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending each Page Program (PP/PP3B/PP4B) command. The device programs only the last 256 data bytes sent to the device. The last address byte (the 8 least significant address bits, A7-A0) should be set to 0 for 256 bytes page program. If A7-A0 are not all zero, transmitted data that exceed page length are programmed from the starting address (32-bit address that last 8 bit are all 0) of currently selected page. If the data bytes sent to the device exceeds 256, the last 256 data byte is programmed at the request page and previous data will be disregarded. If the data bytes sent to the device has not exceeded 256, the data will be programmed at the request address of the page. There will be no effort on the other data bytes of the same page.

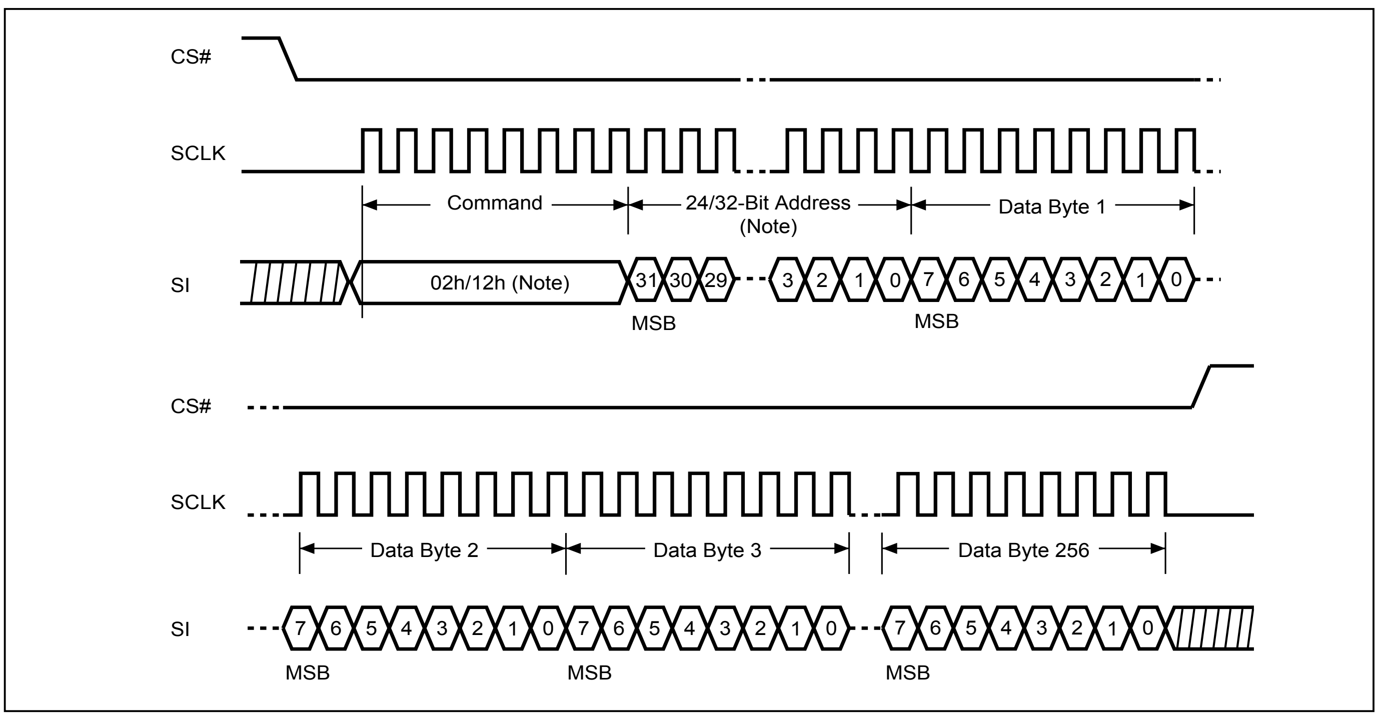
In DTR OPI, the starting address given must be even address (A0=0) and data byte number must be even.

The sequence of issuing PP/PP3B/PP4B instruction is: CS# goes low→ sending PP/PP3B/PP4B instruction code→ 3-byte or 4-byte address → at least 1-byte on data in SPI and STR OPI; at least two bytes in DOPI→ CS# goes high.

The CS# must be kept to low during the whole Page Program cycle; The CS# must go high exactly at the byte boundary in SPI (the latest eighth bit of data being latched in), CS# must go high while SCLK is low in DOPI, otherwise the instruction will be rejected and will not be executed.

The self-timed Page Program Cycle time (tPP) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Page Program cycle is in progress. The WIP sets during the tPP timing, and clears when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the page is protected by BP bits (Block Protect Mode), the Page Program (PP/PP3B/PP4B) instruction will not be executed.

Figure 70. Page Program (PP/PP3B/PP4B) Sequence (SPI Mode)



Note: The number of address cycles are based on different address mode. In 3-Byte command operation, it is 24-bit. In 4-Byte command operation, it is 32-bit.

Figure 71. Page Program (PP) Sequence (STR-OPI Mode)

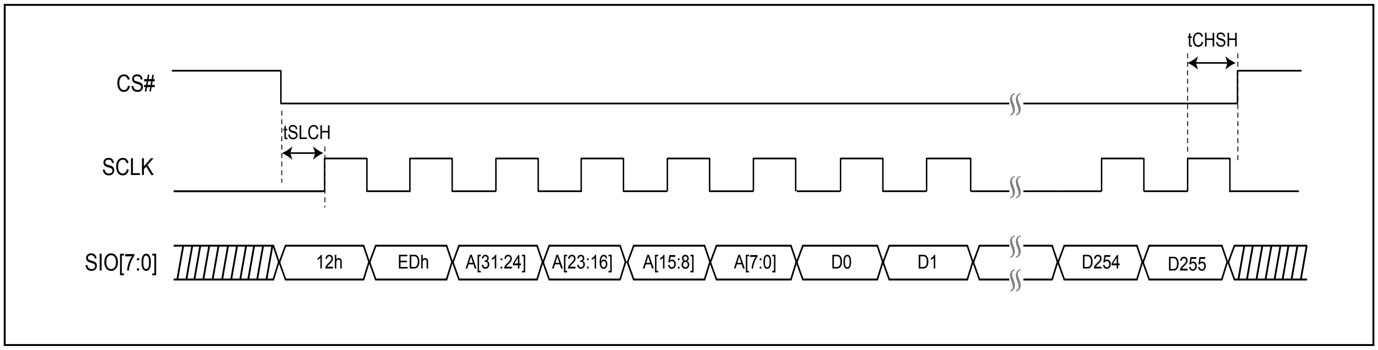
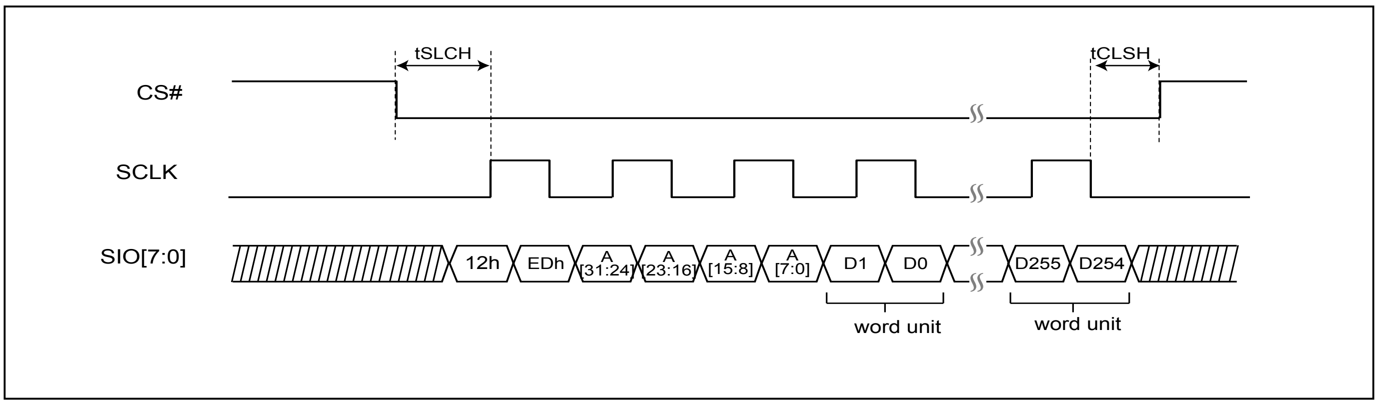


Figure 72. Page Program (PP) Sequence (DTR-OPI Mode)



Note: CS# must go high while SCLK is low.

10-22. Deep Power-down (DP)

The Deep Power-down (DP) instruction is for setting the device to minimum power consumption (the standby current is reduced from ISB1 to ISB2). The Deep Power-down mode requires the Deep Power-down (DP) instruction to enter, during the Deep Power-down mode, the device is not active and all Write/Program/Erase instruction are ignored. When CS# goes high, it's only in deep power-down mode not standby mode. It's different from Standby mode.

The sequence of issuing DP instruction is: CS# goes low→sending DP instruction code→CS# goes high.

Once the DP instruction is set, all instruction will be ignored except the Release from Deep Power-down mode (RDP) and Read Electronic Signature (RES) instruction and softreset command. (those instructions allow the ID being reading out). When Power-down, or software reset command the deep power-down mode automatically stops, and when power-up, the device automatically is in standby mode. For DP instruction the CS# must go high exactly at the byte boundary (the latest eighth bit of instruction code been latched-in); otherwise, the instruction will not executed. As soon as Chip Select (CS#) goes high, a delay of tDP is required before entering the Deep Power-down mode.

The device exits Deep Power-down mode and returns to Stand-by mode if CS# pulses low for tCRDP or if the device is power-cycled or hardware reset. After CS# goes high, there is a delay of tRES1 before the device transitions from Deep Power-down mode back to Stand-by mode.

Figure 73. Deep Power-down (DP) Sequence (SPI Mode)

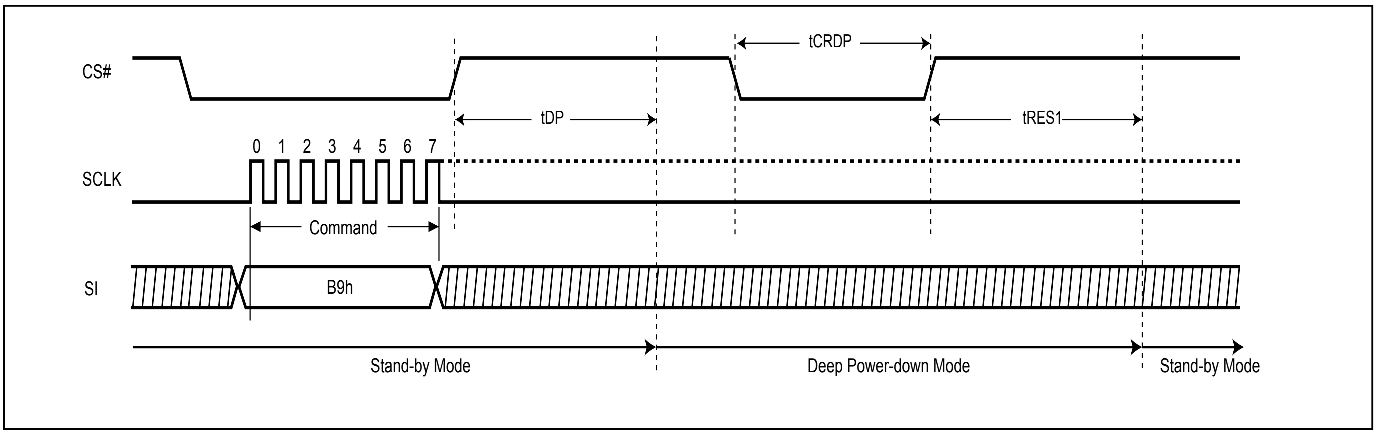


Figure 74. Deep Power-down (DP) Sequence (STR-OPI Mode)

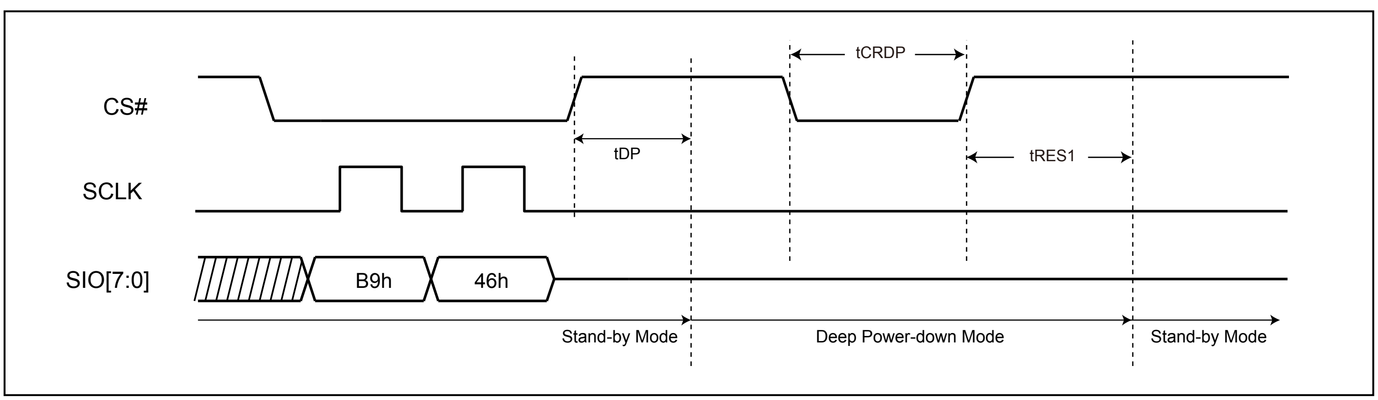
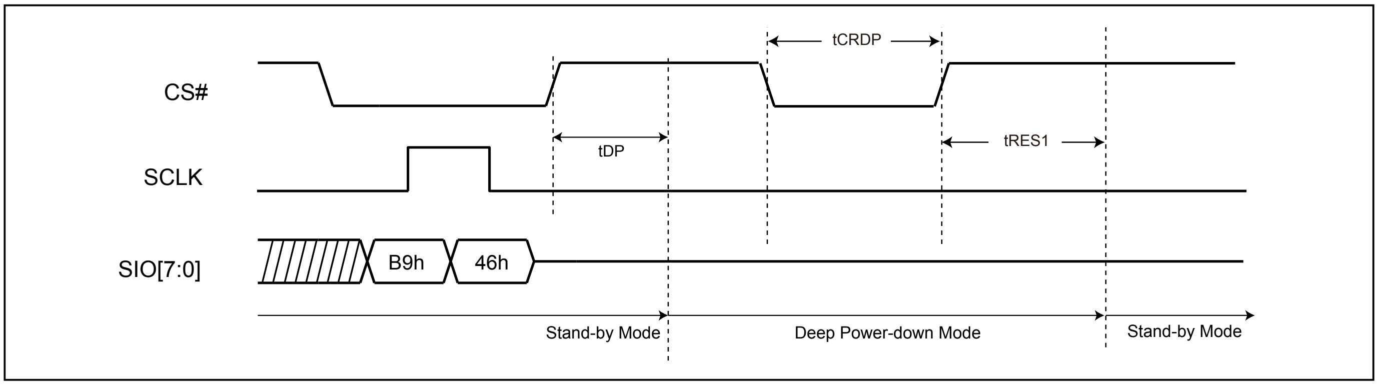


Figure 75. Deep Power-down (DP) Sequence (DTR-OPI Mode)



10-23. Enter Secured OTP (ENSO)

The ENSO instruction is for entering the additional 8K-bit secured OTP mode. While device is in 8K-bit secured OTP mode, main array access is not available. The additional 8K-bit secured OTP is independent from main array and may be used to store unique serial number for system identifier. After entering the Secured OTP mode, follow standard read or program procedure to read out the data or update data. The Secured OTP data cannot be updated again once it is lock-down.

The sequence of issuing ENSO instruction is: CS# goes low→ sending ENSO instruction to enter Secured OTP mode→ CS# goes high.

Please note that after issuing ENSO command user can only access secure OTP region with standard read or program procedure. Furthermore, once security OTP is lock down, only read related commands are valid.

10-24. Exit Secured OTP (EXSO)

The EXSO instruction is for exiting the additional 8K-bit secured OTP mode.

The sequence of issuing EXSO instruction is: CS# goes low→ sending EXSO instruction to exit Secured OTP mode→ CS# goes high.

10-25. Write Protection Selection (WPSEL)

There are two write protection methods provided on this device, (1) Block Lock (BP) protection mode (2) Advanced Sector protection mode. If WPSEL=0, flash is under BP protection mode. If WPSEL=1, flash is under Advanced Sector protection mode. The default value of WPSEL is “0”. WPSEL command can be used to set WPSEL=1. **Please note that WPSEL is an OTP bit. Once WPSEL is set to 1, there is no chance to recovery WPSEL back to “0”.** If the flash is put on BP mode, the Advanced Sector protection mode is disabled. Contrarily, if flash is on the Advanced Sector protection mode, the BP mode is disabled.

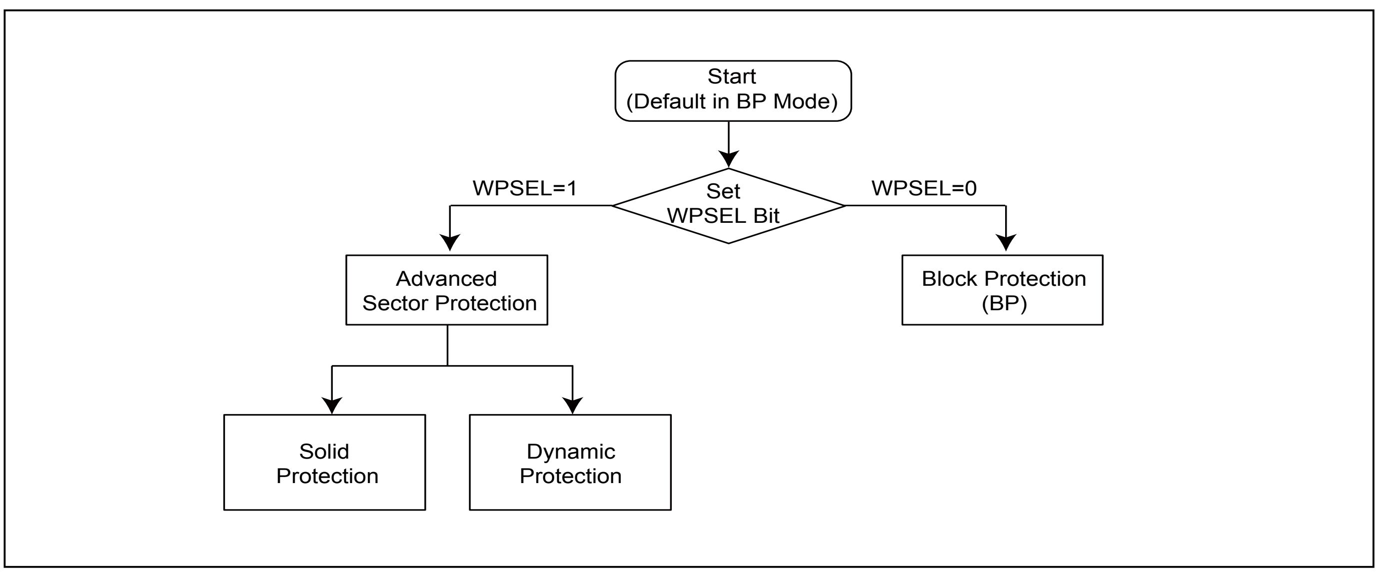
Every time after the system is powered-on, and the Security Register bit 7 is checked to be WPSEL=1, all the blocks or sectors will be write protected by Dynamic Protected Bit (DPB) in default. User may only unlock the blocks or sectors via GBULK instruction. Program or erase functions can only be operated after the Unlock instruction is conducted.

When WPSEL = 0: Block Lock (BP) protection mode,
Array is protected by BP3~BP0 and BP bits are protected by “SRWD=1 and WP#=0”, where SRWD is bit 7 of status register that can be set by WRSR command.

When WPSEL =1: Advanced Sector protection mode,
Blocks are individually protected by their own SPB or DPB lock bits which are set to “1” after power up. When the system accepts and executes WPSEL instruction, the bit 7 in security register will be set. It will activate WRLR, RDLR, WRSPB, ESSPB, WRDPB, RDDPB, GBLK, GBULK etc instructions to conduct block lock protection and replace the original Software Protect Mode (SPM) use (BP3~BP0) indicated block methods. Under the Advanced Sector protection mode (WPSEL=1), hardware protection is performed by driving WP#=0. Once WP#=0 all array blocks/sectors are protected regardless of the contents of SPB or DPB lock bits.

The sequence of issuing WPSEL instruction is: CS# goes low → sending WPSEL instruction to enter the individual block protect mode → CS# goes high.

Write Protection Selection

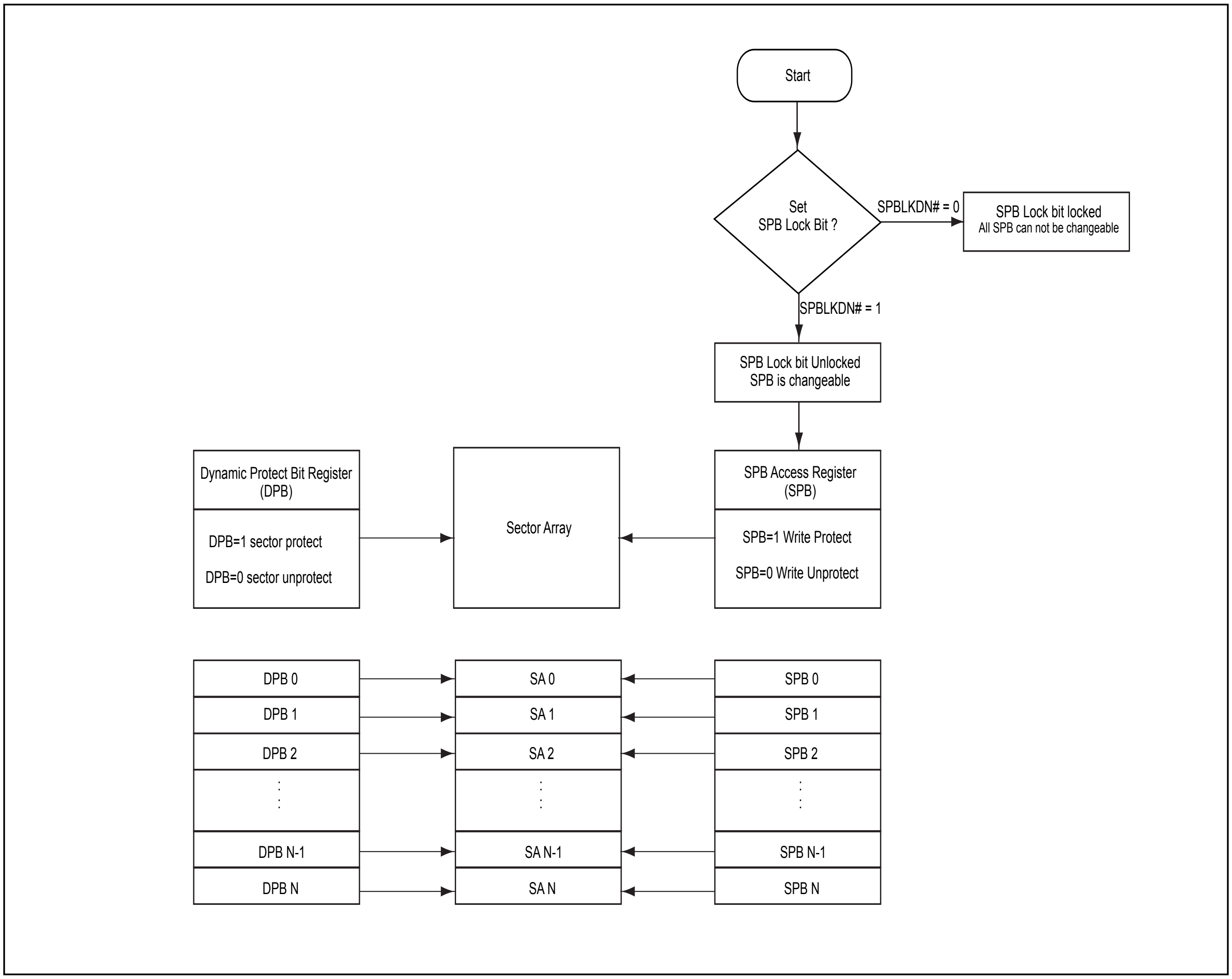


10-26. Individual Sector Protection

There is a non-volatile (SPB) protection bit related to the single sector in main flash array. Each of the sectors is protected from programming or erasing operation when the bit is set.

The figure below helps describing an overview of these methods. The device is default to the Solid mode when shipped from factory. The detail algorithm of advanced sector protection is shown as follows:

Figure 76. Individual Sector Protection Overview



10-26-1. Lock Register

The Lock Register is a 8-bit one-time programmable register. Lock Register bit [6] is SPB Lock Down Bit (SPBLKDN) which is an unique bit assigned to control all SPB bit status.

When SPBLKDN is 1, SPB can be changed. When it is locked as 0, all SPB can not be changed anymore, and SPBLKDN bit itself can not be altered anymore, either.

The Lock Register is programmed using the WRLR (Write Lock Register) command. A WREN command must be executed to set the WEL bit before sending the WRLR command.

Lock Register

Bits	Field Name	Function	Type	Default State	Description
7	RFU	Reserved	OTP	1	Reserved for Future Use
6	SPBLKDN#	SPB Lock Down	OTP	1	1 = SPB changeable 0 = freeze SPB
5 to 0	RFU	Reserved	OTP	1	Reserved for Future Use

Figure 77. Read Lock Register (RDLR) Sequence

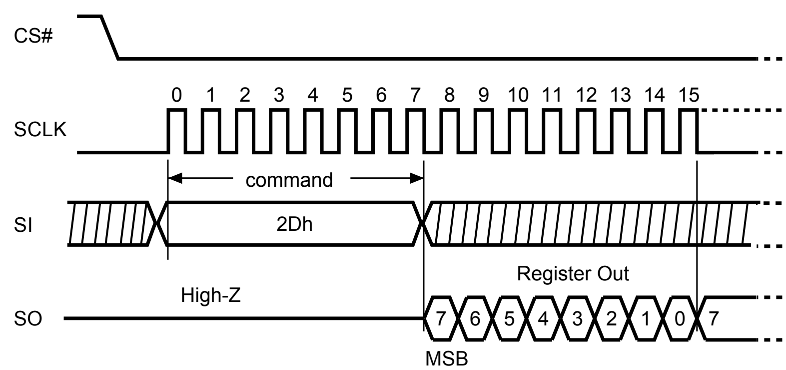


Figure 78. Read Lock Register (RDLR) Sequence (STR-OPI Mode)

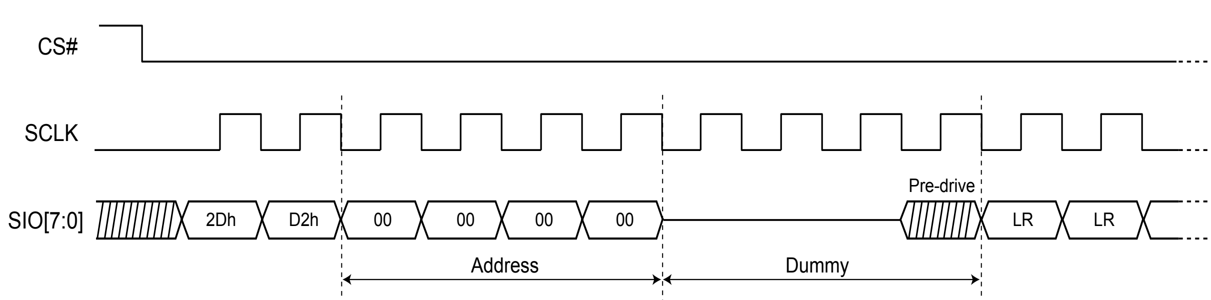


Figure 79. Read Lock Register (RDLR) Sequence (DTR-OPI Mode)

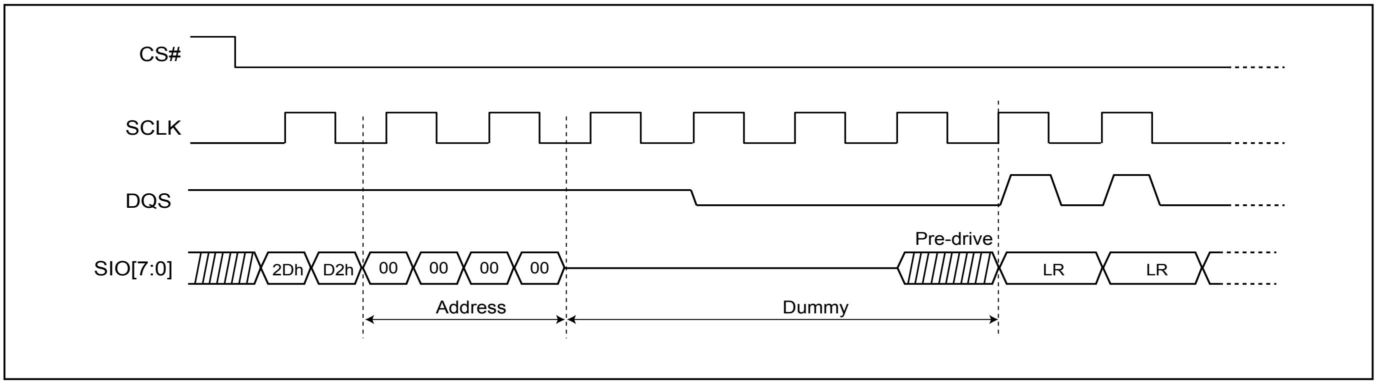


Figure 80. Write Lock Register (WRLR) Sequence

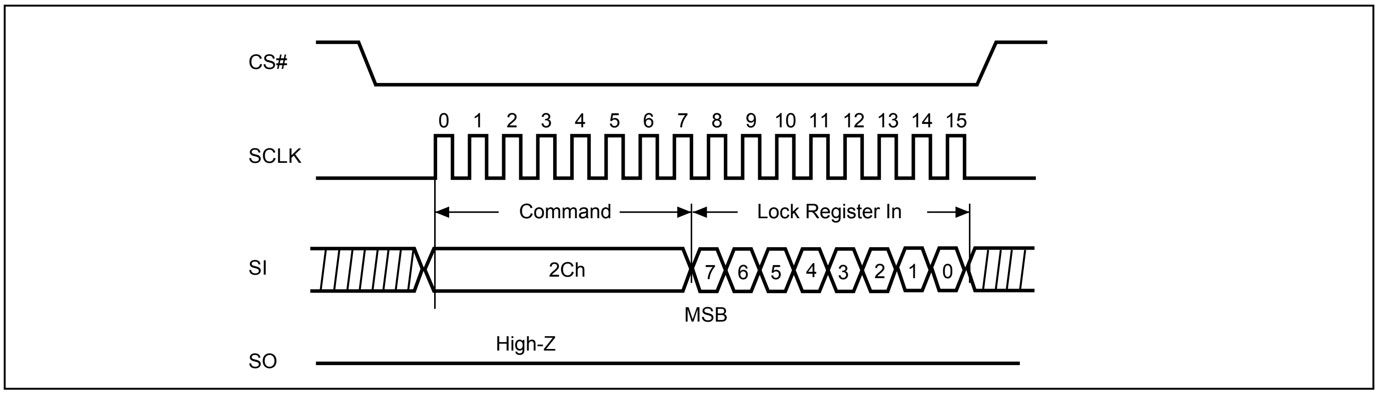


Figure 81. Write Lock Register (WRLR) Sequence (STR-OPI Mode)

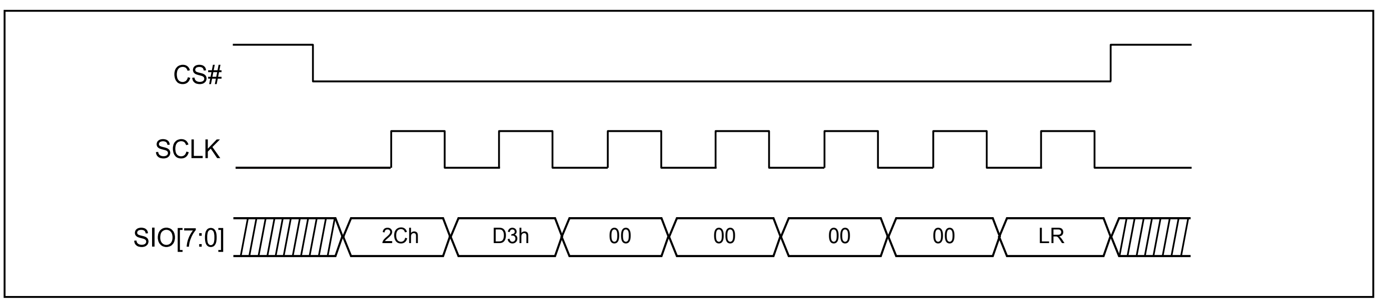
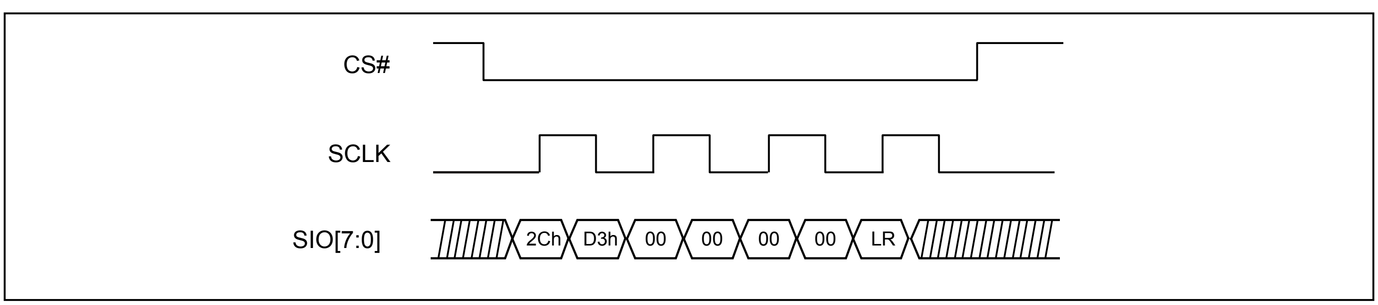


Figure 82. Write Lock Register (WRLR) Sequence (DTR-OPI Mode)



Note: CS# must go high while SCLK is low.

10-26-2. Solid Protection Bits

The Solid Protection Bits (SPBs) are nonvolatile bits for enabling or disabling write-protection to sectors and blocks. The SPB bits have the same endurance as the Flash memory. An SPB is assigned to each 4KB sector in the bottom and top 64KB of memory and to each 64KB block in the remaining memory. The factory default state of the SPB bits is “0”, which has the sector/block write-protection disabled.

When an SPB is set to “1”, the associated sector or block is write-protected. Program and erase operations on the sector or block will be inhibited. SPBs can be individually set to “1” by the WRSPB command. However, the SPBs cannot be individually cleared to “0”. Issuing the ESSPB command clears all SPBs to “0”. A WREN command must be executed to set the WEL bit before sending the WRSPB or ESSPB command.

The RDSPB command reads the status of the SPB of a sector or block. The RDSPB command returns 00h if the SPB is “0”, indicating write-protection is disabled. The RDSPB command returns FFh if the SPB is “1”, indicating write-protection is enabled.

Note: If SPBLKDN=0, commands to set or clear the SPB bits will be ignored.

SPB Register

Bit	Description	Bit Status	Default	Type
7 to 0	SPB (Solid Protection Bit)	00h = Unprotect Sector / Block FFh = Protect Sector / Block	00h	Non-volatile

Figure 83. Read SPB Status (RDSPB) Sequence

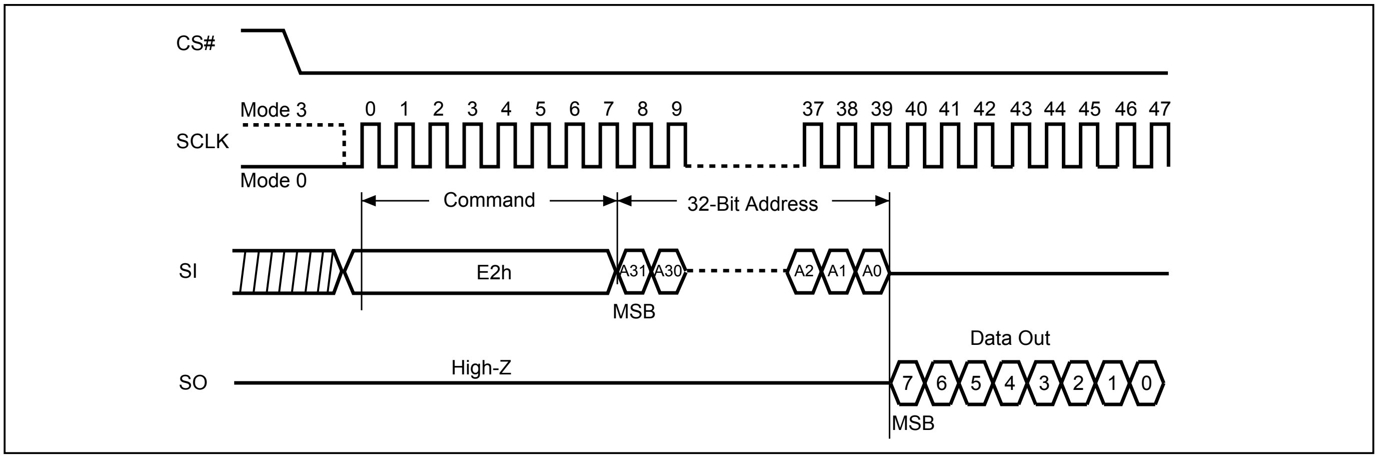


Figure 84. Read SPB Status (RDSPB) Sequence (STR-OPI Mode)

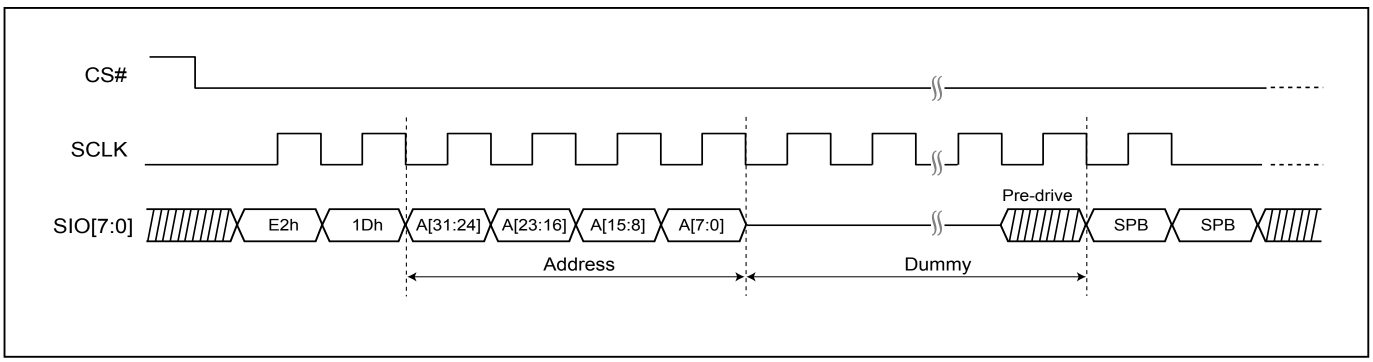


Figure 85. Read SPB Status (RDSPB) Sequence (DTR-OPI Mode)

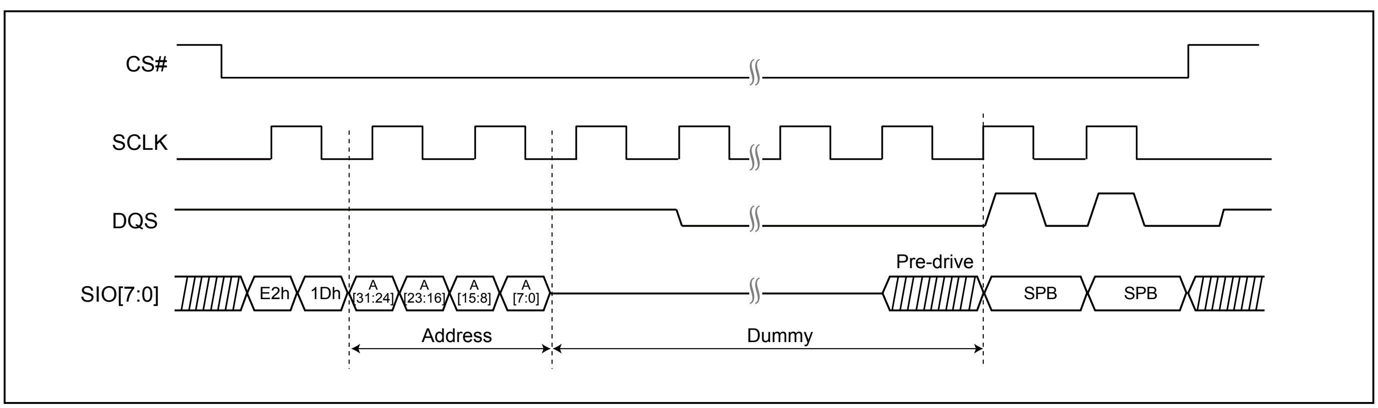


Figure 86. SPB Erase (ESSPB) Sequence

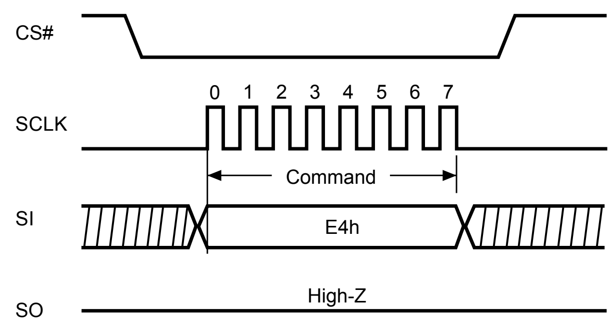


Figure 87. SPB Erase (ESSPB) Sequence (STR-OPI Mode)

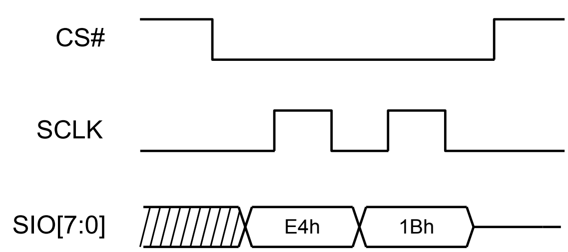


Figure 88. SPB Erase (ESSPB) Sequence (DTR-OPI Mode)

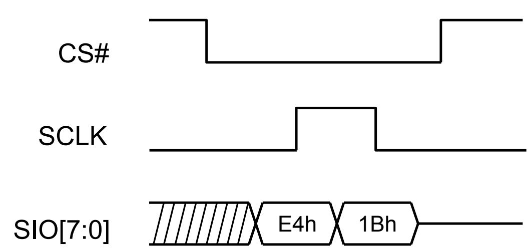


Figure 89. SPB Program (WRSPB) Sequence

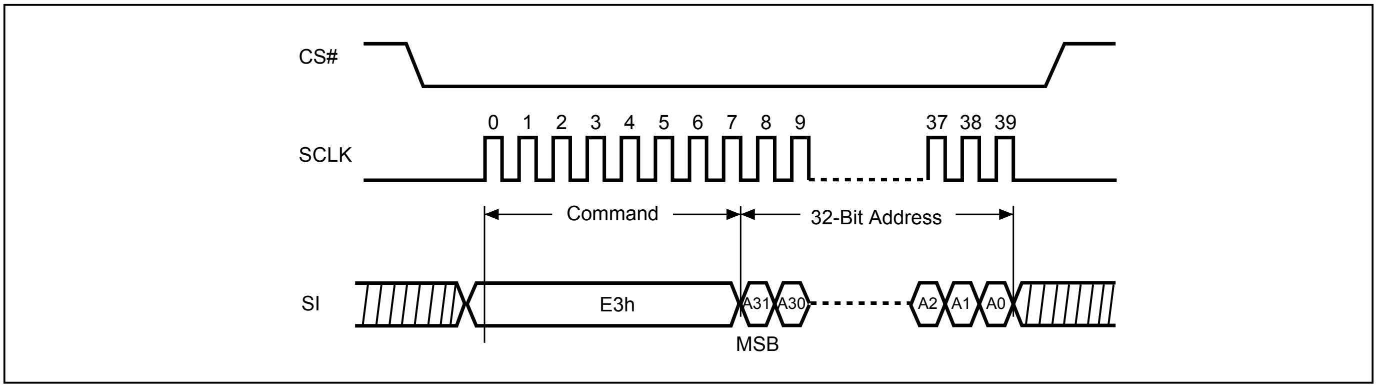


Figure 90. SPB Program (WRSPB) Sequence (STR-OPI Mode)

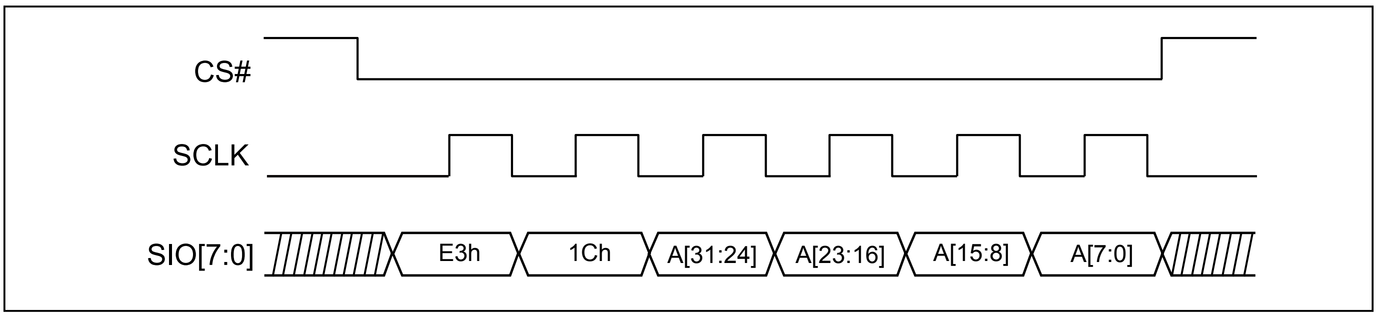
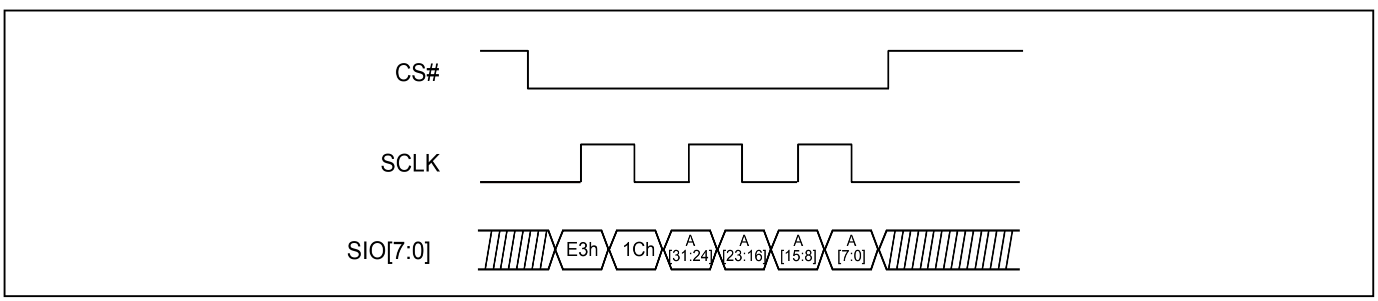


Figure 91. SPB Program (WRSPB) Sequence (DTR-OPI Mode)



10-26-3. Dynamic Write Protection Bits

The Dynamic Protection features a volatile type protection to each individual sector. It can protect sectors from unintentional change, and is easy to disable when there are necessary changes.

All DPBs are default as protected (FFh) after reset or upon power up cycle. Via setting up Dynamic Protection bit (DPB) by write DPB command (WRDPB), user can cancel the Dynamic Protection of associated sector.

The Dynamic Protection only works on those unprotected sectors whose SPBs are cleared. After the DPB state is cleared to “0”, the sector can be modified if the SPB state is unprotected state.

DPB Register

Bit	Description	Bit Status	Default	Type
7 to 0	DPB (Dynamic protected Bit)	00h= DPB for the sector address unprotected FFh= DPB for the sector address protected	FFh	Volatile

Figure 92. Read DPB Register (RDDPB) Sequence

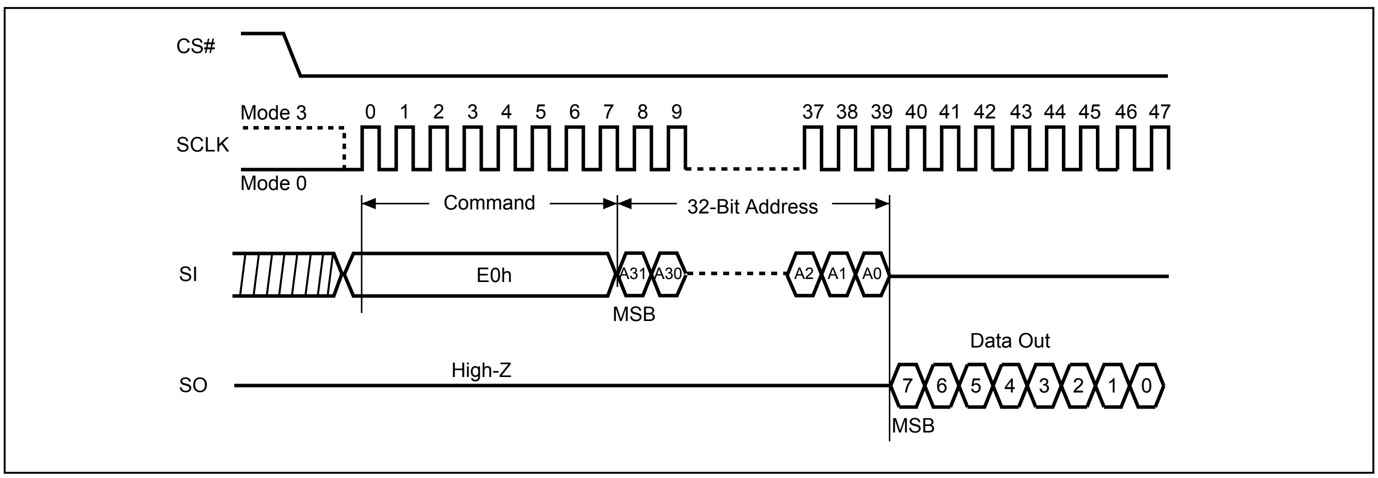


Figure 93. Read DPB Register (RDDPB) Sequence (STR-OPI Mode)

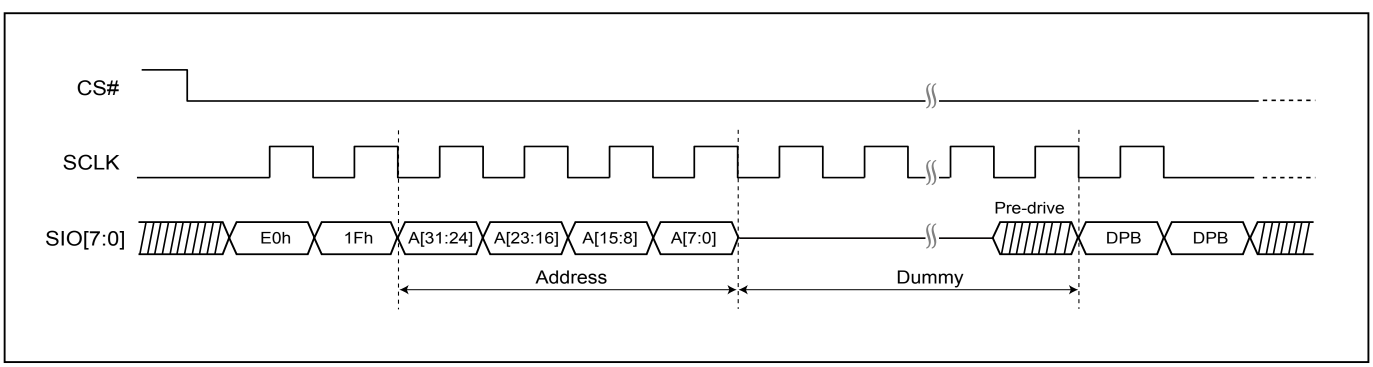


Figure 96. Read DPB Register (RDDPB) Sequence (DTR-OPI Mode)

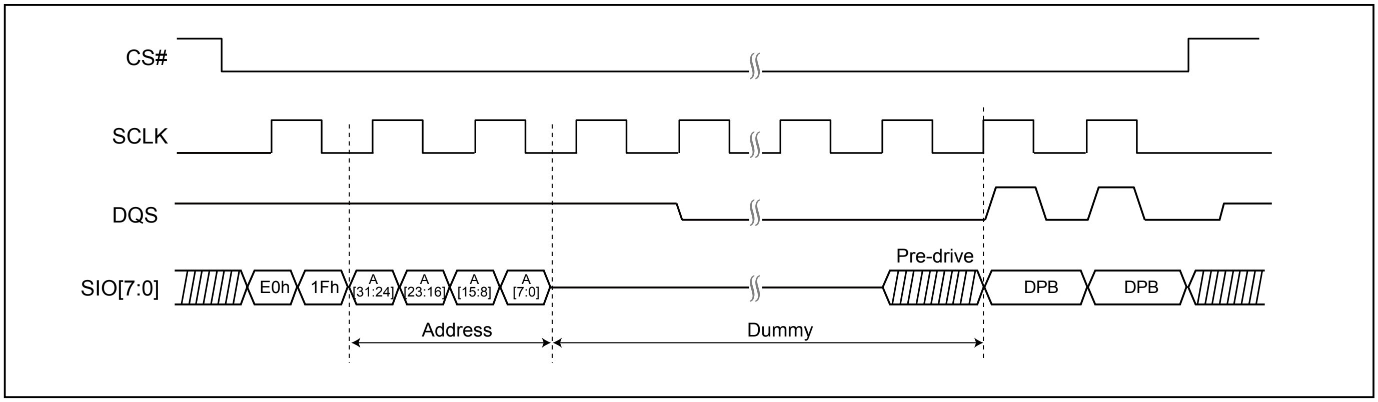


Figure 94. Write DPB Register (WRDPB) Sequence

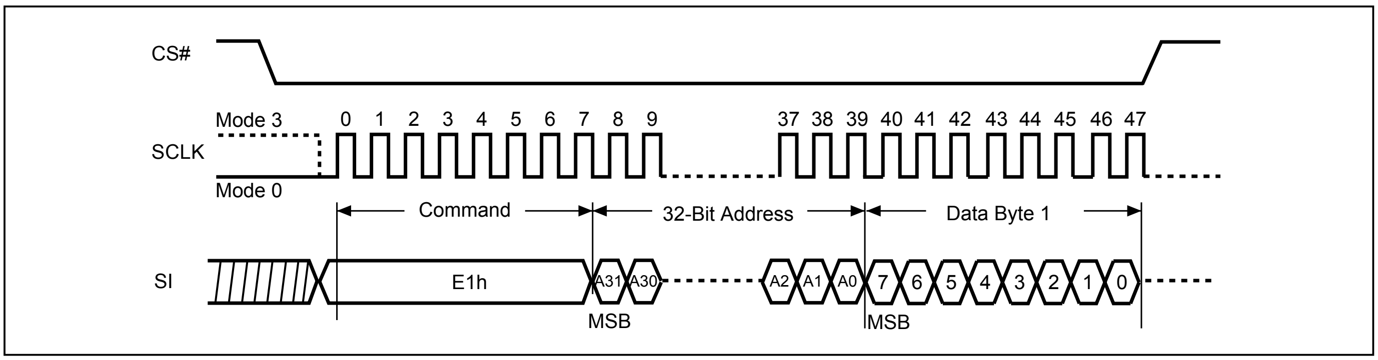


Figure 95. Write DPB Register (WRDPB) Sequence (STR-OPI Mode)

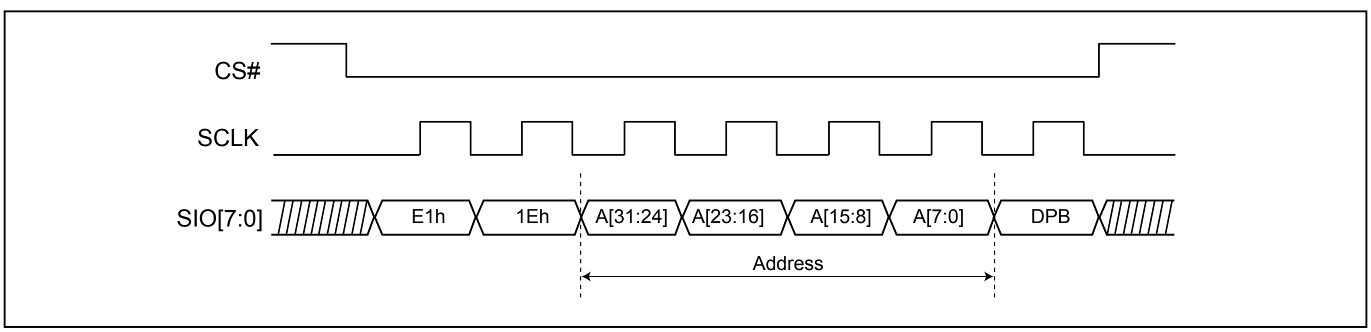
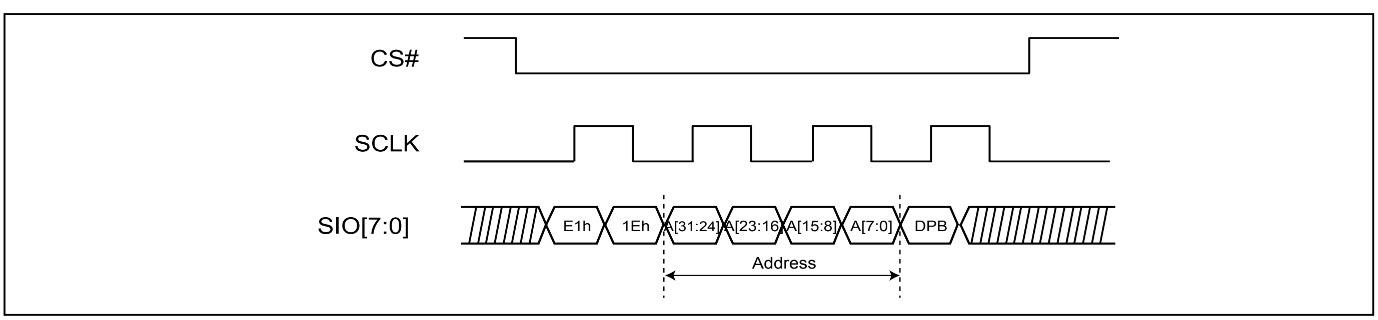


Figure 97. Write DPB Register (WRDPB) Sequence (DTR-OPI Mode)



10-26-4. Gang Block Lock/Unlock (GBLK/GBULK)

These instructions are only effective after WPSEL was executed. The GBLK/GBULK instruction is a chip-based protected or unprotected operation. It can enable or disable all DPB.

The WREN (Write Enable) instruction is required before issuing GBLK/GBULK instruction.
The sequence of issuing GBLK/GBULK instruction is: CS# goes low → send GBLK/GBULK (7Eh/98h) instruction →CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

The CS# must go high exactly at the byte boundary, otherwise, the instruction will be rejected and not be executed.

10-26-5. Sector Protection States Summary Table

Protection Status		Sector State
DPB bit	SPB bit	
0	0	Unprotect
0	1	Protect
1	0	Protect
1	1	Protect

10-27. Program Suspend and Erase Suspend

The Suspend instruction interrupts a Program or Erase operation to allow the device conduct other operations.

After the device has entered the suspended state, the memory array can be read except for the page being programmed or the sector being erased.

Security Register bit 2 (PSB) and bit 3 (ESB) can be read to check the suspend status. The PSB (Program Suspend Bit) sets to “1” when a program operation is suspended. The ESB (Erase Suspend Bit) sets to “1” when an erase operation is suspended. The PSB or ESB clears to “0” when the program or erase operation is resumed.

When the Serial NOR Flash receives the Suspend instruction, Program Suspend Latency(tPSL) or Erase Suspend latency(tESL) is required to complete suspend operation. (Refer to *"Table 23. AC CHARACTERISTICS"*) After the device has entered the suspended state, the WEL bit is clears to “0” and the PSB or ESB in security register is set to “1”, then the device is ready to acceptanother command.

However, some commands can be executed without tPSL or tESL latency during the program/erase suspend, and can be issued at any time during the Suspend.

Please refer to *"Table 16. Acceptable Commands During Suspend".*

Figure 98. Suspend to Read Latency

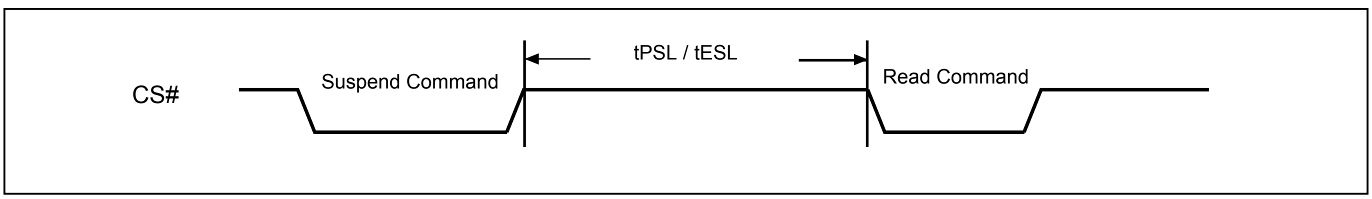


Table 16. Acceptable Commands During Suspend

Command Name	Command Code	Suspend Type	
		Program Suspend	Erase Suspend
Commands which require tPSL/tESL delay			
READ	03h/13h	•	•
FAST_READ	0Bh/0Ch	•	•
8READ	ECh	•	•
8DTRD	EEh	•	•
RDSFDP	5Ah	•	•
RDID	9Fh	•	•
SBL	C0h	•	•
ENSO	B1h	•	•
EXSO	C1h	•	•
WREN	06h	•	•
RESUME	30h	•	•
RDLR	2Dh	•	•
RDSPB	E2h	•	•
RDFBR	16h	•	•
RDDPB	E0h	•	•
RDCR2 with A[31:30]=00/01	71h	•	•
WRCR2 with A[31:30]=00	72h	•	•
WRCR2 with A[31:30]=01			
Commands not required tPSL/tESL delay			
WRDI	04h	•	•
RDSR	05h	•	•
RDCR	15h	•	•
RDCR2 with A[31:30]=10	71h	•	•
WRCR2 with A[31:30]=10	72h	•	•
RDSCUR	2Bh	•	•
RES	ABh	•	•
RSTEN	66h	•	•
RST	99h	•	•
NOP	00h	•	•

10-28. Program Resume and Erase Resume

The Resume instruction resumes a suspended Program or Erase operation. After the device receives the Resume instruction, the WEL and WIP bits are set to “1” and the PSB or ESB is cleared to “0”.The program or erase operation will continue until it is completed or until another Suspend instruction is received.

To issue another Suspend instruction, the minimum resume-to-suspend latency (tPRS or tERS) is required. However, in order to finish the program or erase progress, a period equal to or longer than the typical timing is required.

To issue other command except suspend instruction, a latency of the self-timed Page Program Cycle time (tPP) or Sector Erase (tSE) is required. The WEL and WIP bits are cleared to “0” after the Program or Erase operation is completed.

Figure 99. Resume to Read Latency

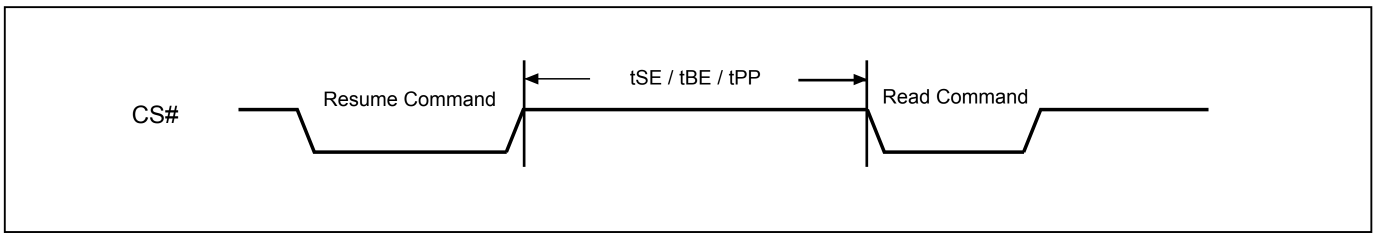
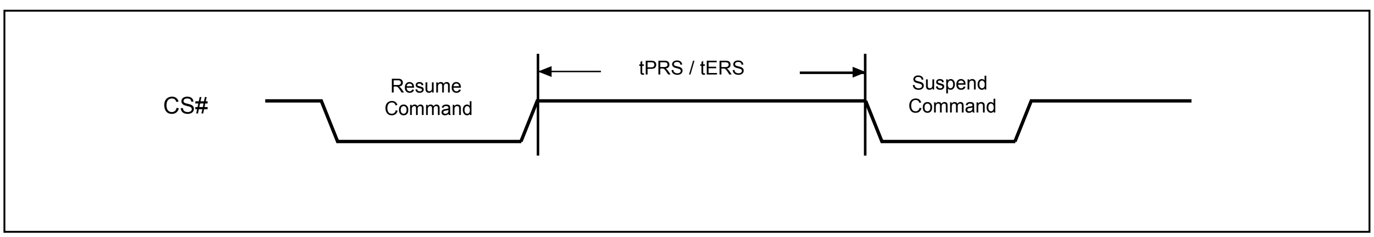


Figure 100. Resume to Suspend Latency



10-29. No Operation (NOP)

The “No Operation” command is only able to terminate the Reset Enable (RSTEN) command and will not affect any other command.

10-30. Software Reset (Reset-Enable (RSTEN) and Reset (RST))

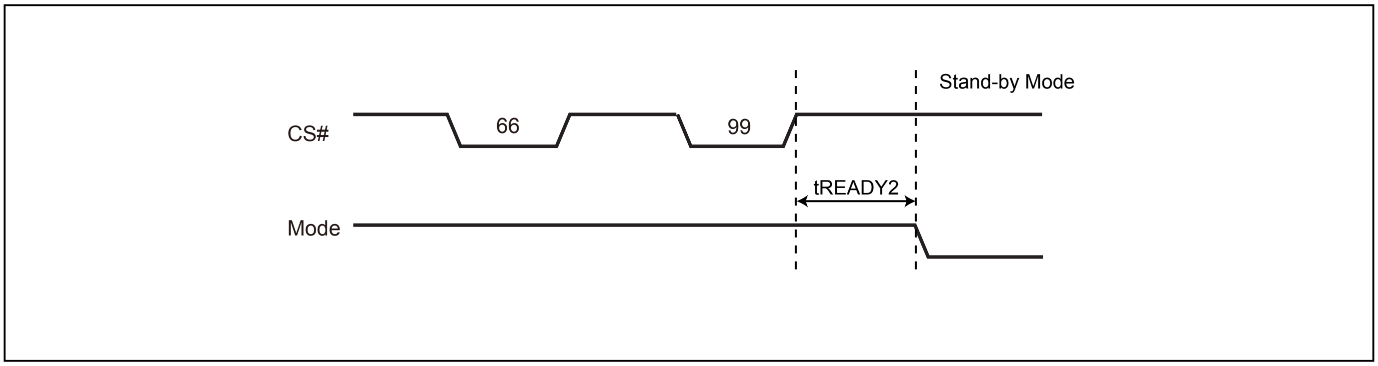
The Software Reset operation combines two instructions: Reset-Enable (RSTEN) command following a Reset (RST) command. It returns the device to a standby mode. All the volatile bits and settings will be cleared then, which makes the device return to the default status as power on.

To execute Reset command (RST), the Reset-Enable (RSTEN) command must be executed first to perform the Reset operation. If there is any other command to interrupt after the Reset-Enable command, the Reset-Enable will be invalid.

If the Reset command is executed during program or erase operation, the operation will be disabled, the data under processing could be damaged or lost.

The reset time is different depending on the last operation. For details, please refer to *"Table 19. Reset Timing-(Other Operation)"* for tREADY2.

Figure 101. Software Reset Recovery



Note: Refer to *"Table 19. Reset Timing-(Other Operation)"* for tREADY2.

Figure 102. Reset Sequence (SPI mode)

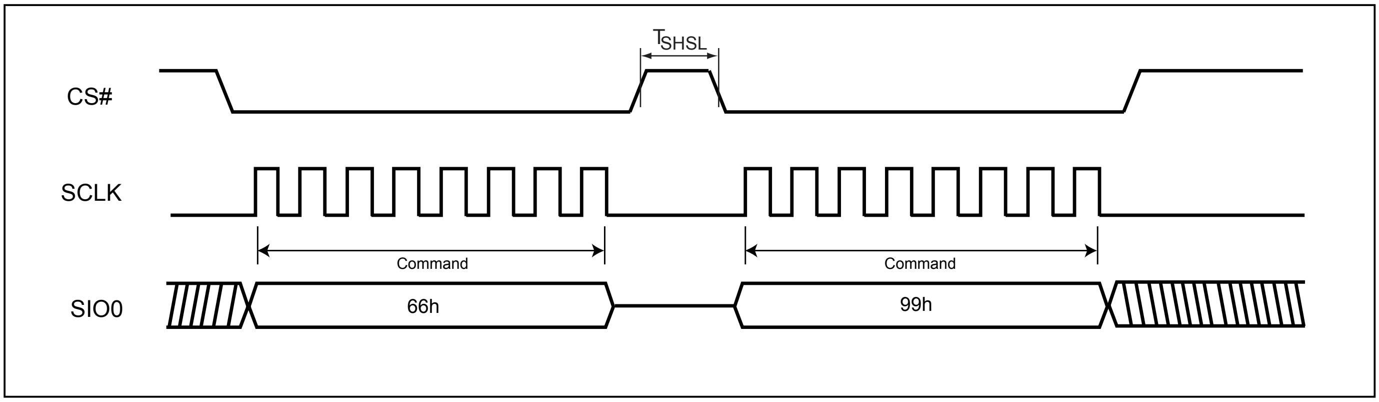


Figure 103. Reset Sequence (STR-OPI mode)

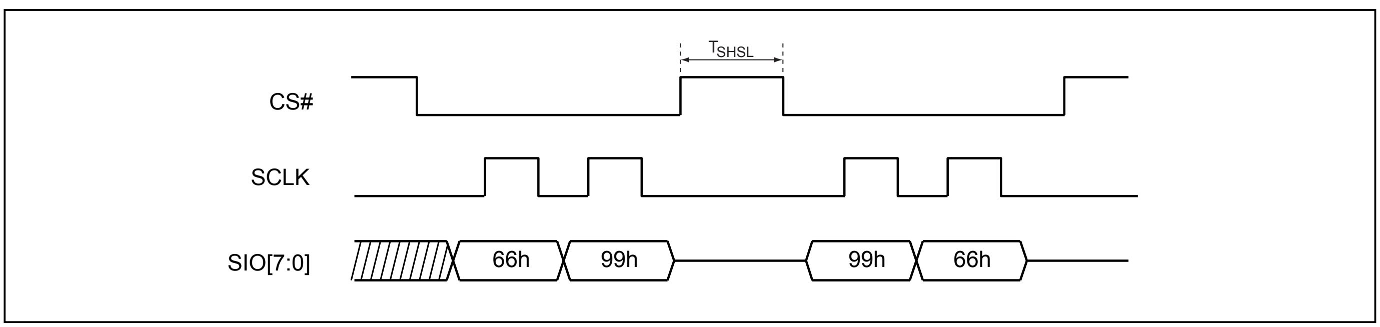
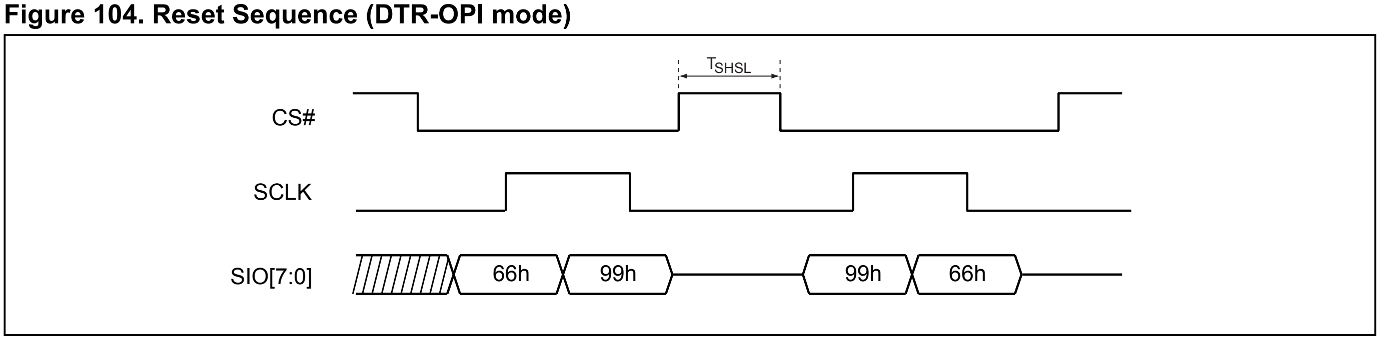


Figure 104. Reset Sequence (DTR-OPI mode)



11. Serial Flash Discoverable Parameter (SFDP)

11-1. Read SFDP Mode (RDSFDP)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI.

The sequence of issuing RDSFDP instruction in SPI is CS# goes low→send RDSFDP instruction (5Ah)→send 3 address bytes on SI pin→ send 8 dummy cycles → read SFDP code on SO→to end RDSFDP operation can use CS# to high at any time during data out.

SFDP in SPI is a JEDEC standard, JESD216.

The sequcn of issuing RDSFDP instruction in OPI/DOPI mode:
CS# low → send RDSFDP instruction (5Ah/A5h) → send 4 address bytes on SIO pin→ send 20 dummy cycles → read SFDP code on SIO[7:0] → to end RDSFDP operation can use CS# to high at any time during data out.

Figure 105. Read Serial Flash Discoverable Parameter (RDSFDP) Sequence

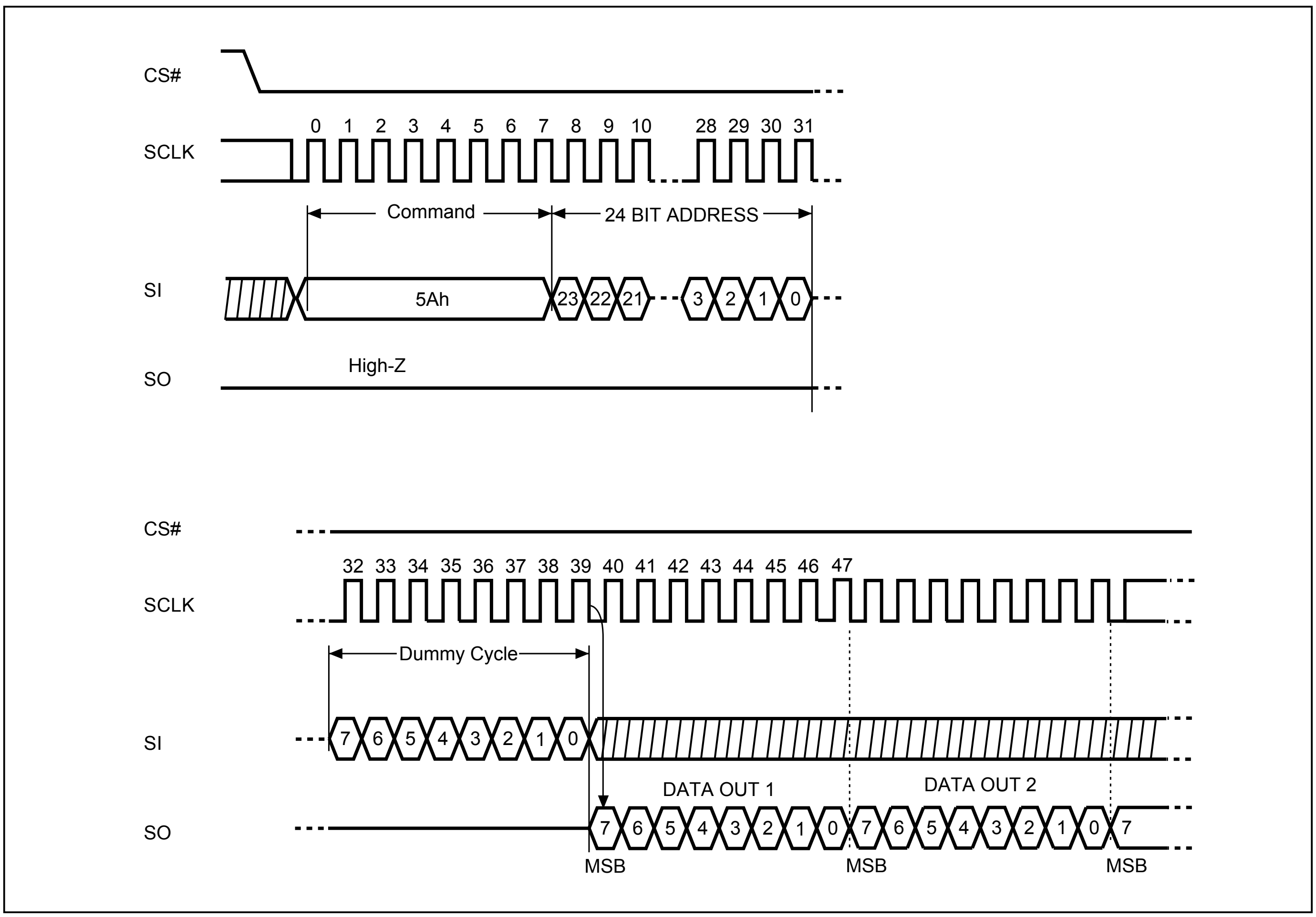


Figure 106. Read Serial Flash Discoverable Parameter (RDSFDP) Sequence (STR-OPI Mode)

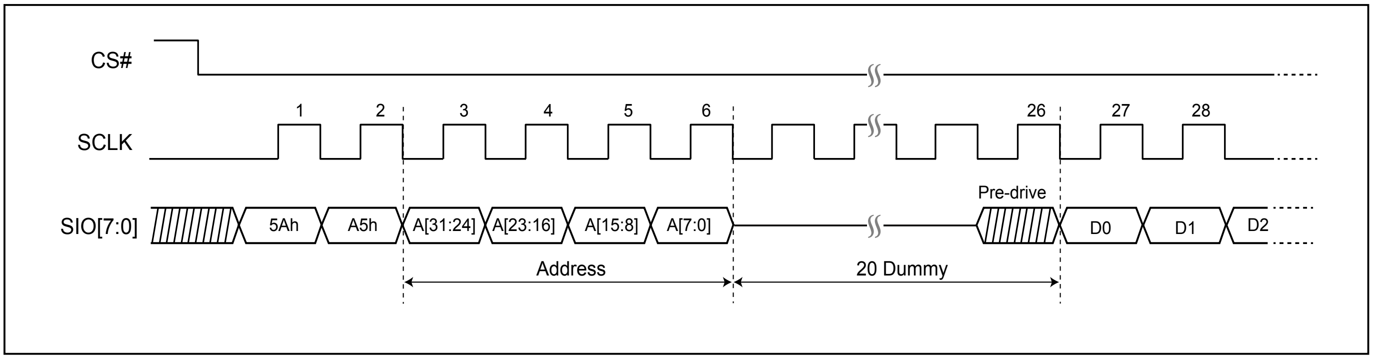
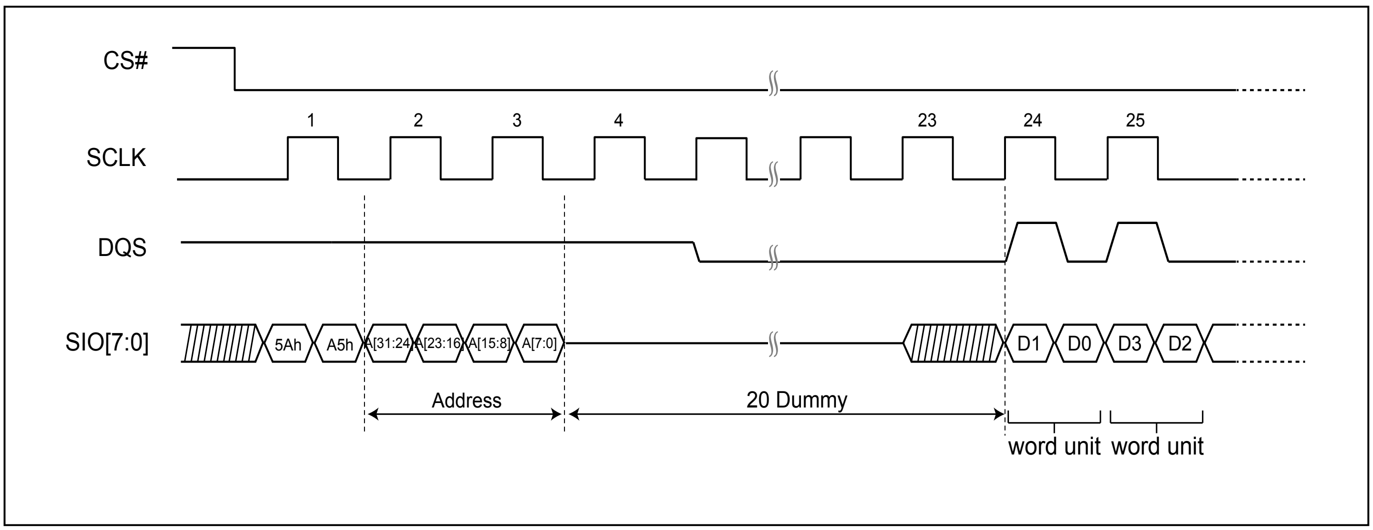


Figure 107. Read Serial Flash Discoverable Parameter (RDSFDP) Sequence (DTR-OPI Mode)



Note: Address must be low byte (A0=0) in DTR OPI.

Table 17. Signature and Parameter Identification Data Values (TBD)

12. RESET

Driving the RESET# pin low for a period of tRLRH or longer will reset the device. After reset cycle, the device is at the following states:
- Standby mode
- All the volatile bits such as WEL/WIP will return to the default status as power on.
- All the volatile bits in CR2 will return to the default status as power on.
- Fastboot read will be executed on first CS# pin goes low

If the device is under programming or erasing, driving the RESET# pin low will also terminate the operation and data could be lost. During the resetting cycle, the SIO data becomes high impedance and the current will be reduced to minimum.

Figure 108. RESET Timing

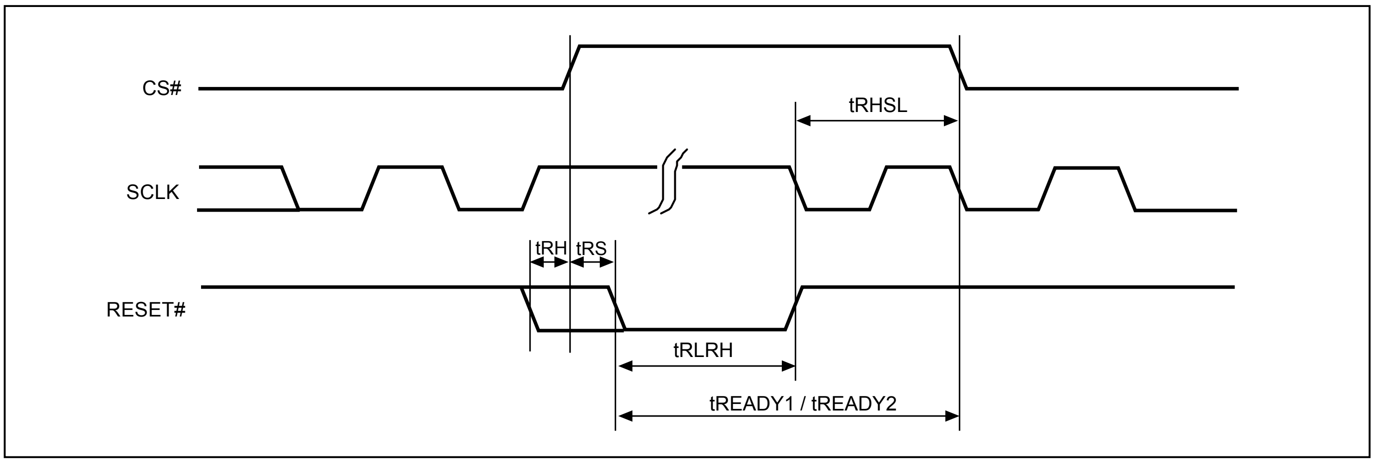


Table 18. Reset Timing-(Standby)

Symbol	Parameter	Min.	Typ.	Max.	Unit
tRHSL	Reset# high before CS# low	10			us
tRS	Reset# setup time	15			ns
tRH	Reset# hold time	15			ns
tRLRH	Reset# low pulse width	10			us
tREADY1	Reset Recovery time	35			us

Table 19. Reset Timing-(Other Operation)

Symbol	Parameter	Min.	Typ.	Max.	Unit
tRHSL	Reset# high before CS# low	10			us
tRS	Reset# setup time	15			ns
tRH	Reset# hold time	15			ns
tRLRH	Reset# low pulse width	10			us
tREADY2	Reset Recovery time (During instruction decoding)	40			us
	Reset Recovery time (for read operation)	40			us
	Reset Recovery time (for program operation)	310			us
	Reset Recovery time(for SE4KB operation)	12			ms
	Reset Recovery time (for BE64K operation)	25			ms
	Reset Recovery time (for Chip Erase operation)	100			ms
	Reset Recovery time (for WRSR operation)	40			ms

13. POWER-ON STATE

The device is at below states when power-up:

- Standby mode (please note it is not deep power-down mode)
- Write Enable Latch (WEL) bit is reset

The device must not be selected during power-up and power-down stage unless the VCC achieves below correct level:

- VCC minimum at power-up stage and then after a delay of tVSL
- GND at power-down

Please note that a pull-up resistor on CS# may ensure a safe and proper power-up/down level.

An internal power-on reset (POR) circuit may protect the device from data corruption and inadvertent data change during power up state. When VCC is lower than VWI (POR threshold voltage value), the internal logic is reset and the flash device has no response to any command.

For further protection on the device, if the VCC does not reach the VCC minimum level, the correct operation is not guaranteed. The write, erase, and program command should be sent after the below time delay:

- tVSL after VCC reached VCC minimum level

The device can accept read command after VCC reached VCC minimum and a time delay of tVSL.
Please refer to the ""Power-up Timing"".

Note:

- To stabilize the VCC level, the VCC rail decoupled by a suitable capacitor close to package pins is recommended. (generally around 0.1uF)
- At power-down stage, the VCC drops below VWI level, all operations are disable and device has no response to any command. The data corruption might occur during the stage while a write, program, erase cycle is in progress.
- To stabilize the VCCQ level, the VCCQ/VSSQ rail decoupled by a suitable capacitor close to package pins is recommended. One VCCQ pin connect to one capacitor.
- It is recommended VCC and VCCQ power are separated system supply with same supply voltage.

14. ELECTRICAL SPECIFICATIONS

Table 20. ABSOLUTE MAXIMUM RATINGS

RATING		VALUE
Ambient Operating Temperature	Industrial grade	-40°C to 85°C
Storage Temperature		-65°C to 150°C
Applied Input Voltage		-0.5V to VCC+0.5V
Applied Output Voltage		-0.5V to VCC+0.5V
VCC to Ground Potential		-0.5V to 2.5V

NOTICE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
2. Specifications contained within the following tables are subject to change.
3. During voltage transitions, all pins may overshoot to VCC+1.0V or -1.0V for period up to 20ns.

Figure 109. Maximum Negative Overshoot Waveform

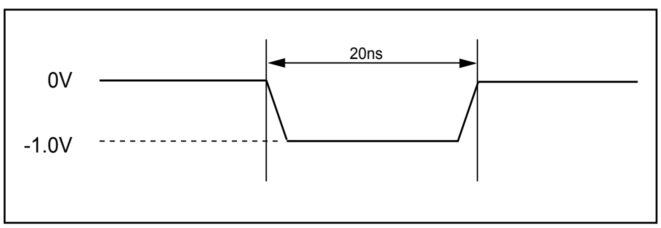


Figure 110. Maximum Positive Overshoot Waveform

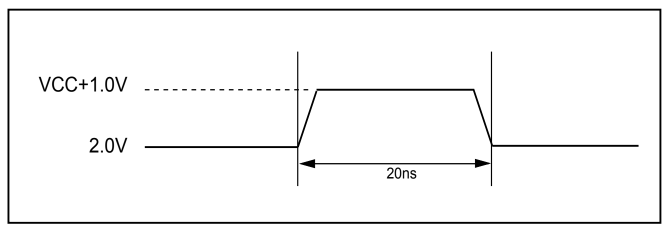


Table 21. CAPACITANCE TA = 25°C, f = 1.0 MHz

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
CIN	Input Capacitance			8	pF	VIN = 0V
COUT	Output Capacitance			8	pF	VOUT = 0V

Figure 111. INPUT TEST WAVEFORMS AND MEASUREMENT LEVEL

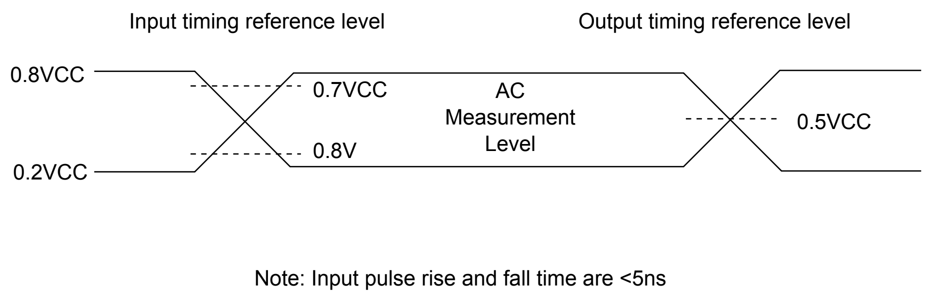


Figure 112. OUTPUT LOADING

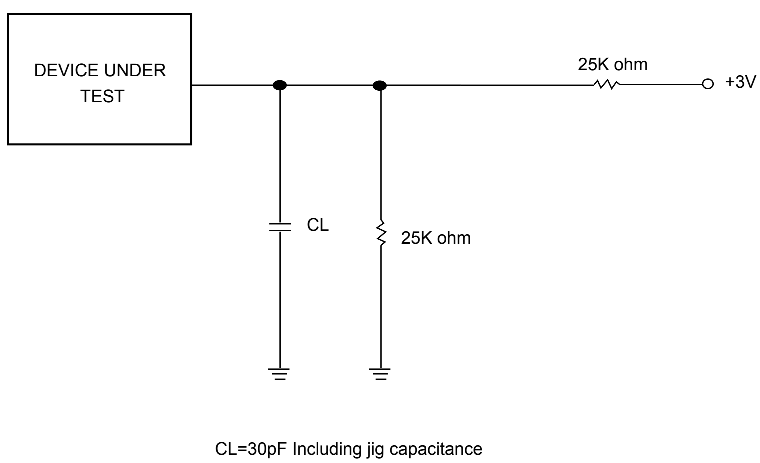


Table 22. DC CHARACTERISTICS

Temperature = -40°C to 85°C, VCC = 2.7V ~ 3.6V

Symbol	Parameter	Notes	Min.	Typ.	Max.	Units	Test Conditions
ILI	Input Load Current	1			±2	uA	VCC = VCC Max, VIN = VCC or GND
ILO	Output Leakage Current	1			±2	uA	VCC = VCC Max, VOUT = VCC or GND
ISB1	VCC Standby Current	1		20	180	uA	VIN = VCC or GND, CS# = VCC
ISB2	Deep Power-down Current			3	50	uA	VIN = VCC or GND, CS# = VCC
ICC1	VCC Read	1,3		20	40	mA	100MHz 8IO STR (SIO floating)
				30	45	mA	100MHz 8IO DTR (SIO floating)
				25	50	mA	133MHz 8IO STR (SIO floating)
				40	60	mA	133MHz 8IO DTR (SIO floating)
ICC2	VCC Program Current	1		30	40	mA	Program in Progress, CS# = VCC
ICC3	VCC Write Status Register (WRSR) Current			20	40	mA	Program status register in progress, CS#=VCC
ICC4	VCC Sector Erase Current (SE)	1		20	40	mA	Erase in Progress, CS#=VCC
ICC4	VCC Block Erase Current (BE)	1		30	40	mA	Erase in Progress, CS#=VCC
ICC5	VCC Chip Erase Current (CE)	1		20	40	mA	Erase in Progress, CS#=VCC
VIL	Input Low Voltage		-0.4		0.3VCC	V	
VIH	Input High Voltage		0.7VCC		VCC+0.4	V	
VOL	Output Low Voltage				0.2	V	IOL=100uA
VOH	Output High Voltage		VCC-0.2			V	IOH=-100uA

Notes :
1. Typical values at VCC = 3.3V, T = 25°C. These currents are valid for all product versions (package and speeds).
2. Typical value is calculated by simulation.
3. VCC current only; not include VCCQ current.

Table 23. AC CHARACTERISTICS

Temperature = -40°C to 85°C, VCC = 2.7V ~ 3.6V

Symbol	Alt.	Parameter		Min.	Typ.	Max.	Unit
fSCLK	fC	Clock frequency for SPI commands (except Read operation)				133	MHz
		Clock frequency for OPI commands				133	MHz
fRSCLK	fR	Clock Frequency for READ instructions				66	MHz
fTSCLK		Clock Frequency for FAST READ				133	MHz
		Clock Frequency for 8READ, 8DTRD		*"9-3-1. Dummy Cycle and Frequency Table (MHz)"*			MHz
tCH[1]	tCLH	Clock High Time		0.45*T			ns
tCL[1]	tCL	Clock Low Time		0.45*T			ns
tCLCH[2]/ tCHCL[2]		Clock Rise Time (peak to peak) / Clock Fall Time (peak to peak)	fSCLK ≤ 100MHz	0.6			V/ns
			fSCLK ≤ 133MHz	0.8			V/ns
tSLCH	tCSS	CS# Active Setup Time (relative to SCLK)		4.5			ns
tCHSL		CS# Not Active Hold Time (relative to SCLK)		3			ns
tSHSL	tCSH	CS# Deselect Time	From Read to next Read	10			ns
			From Write/Erase/Program to Read Status Register	40			ns
tDVCH	tDSU	Data In Setup Time [10]	STR ≤ 133MHz	2			ns
			STR > 133MHz	1			
tDVCH / tDVCL		Data setup time [9] [10]	DTR ≤ 100MHz	1			ns
			DTR ≤ 133MHz	0.8			
tCHDX	tDH	Data In Hold Time [10]	STR ≤ 133MHz	2			ns
			STR > 133MHz	1			
tCHDX / tCLDX		Data hold time [9] [10]	DTR ≤ 100MHz	1			ns
			DTR ≤ 133MHz	0.8			
tCHSH		CS# Active Hold Time (relative to SCLK)	STR	3			ns
tCLSH		CS# active hold time	DTR	3			ns
tSHCH		CS# Not Active Setup Time (relative to SCLK)	STR	3			ns
			DTR	3			ns
tSHQZ[2]	tDIS	Output Disable Time				8	ns
tQSV		DQS Clock transient to DQS valid time				5	ns
tCLQV / tCHQV	tV	Clock transient to Output Valid	Loading: 30pF			5	ns
			Loading: 20pF			5	
			Loading: 15pF			5	
			Loading: 10pF			5	
tCLQX	tHO	Output Hold Time		1			ns
tDQSQ		SIO valid skew related to DQS	Loading: 10pF[10]			0.4	ns
			Loading: 15pF[10]			0.6	
			Loading: 20pF[10]			0.8	
			Loading: 30pF[10]			1	
tQH		SIO hold time related to DQS		min(tCL,tCH)-tQHS			ns

Symbol	Alt.	Parameter		Min.	Typ.	Max.	Unit
tQHS		SIO hold skew factor	Loading: 10pF(10)			0.6	ns
			Loading: 15pF(10)			0.8	
			Loading: 20pF(10)			1	
			Loading: 30pF(10)			1.2	
tDP(2)		CS# High to Deep Power-down Mode				10	us
tRES1(2)		CS# High to Standby Mode				30	us
tCRDP		CS# Toggling Time before Release from Deep Power-Down Mode		20			ns
tW		Write Status/Configuration Register Cycle Time				40	ms
tPP(4)		Page Program Cycle Time			0.15	1.5	ms
tSE		Sector Erase Cycle Time			25	400	ms
tBE		Block Erase (64KB) Cycle Time			220	2000	ms
tCE		Chip Erase Cycle Time			150	300	s
tESL(6)		Erase Suspend Latency				25	us
tPSL(6)		Program Suspend Latency				25	us
tPRS(7)		Latency between Program Resume and next Suspend		0.3	100		us
tERS(8)		Latency between Erase Resume and next Suspend		0.3	400		us

Notes:

1. tCH + tCL must be greater than or equal to 1/ Frequency.
2. Typical values given for TA=25°C. Not 100% tested.
3. Test condition is shown as *Figure 111* and *Figure 112*.
4. While programming consecutive bytes, Page Program instruction provides optimized timings by selecting to program the whole 256 bytes or only a few bytes between 1~256 bytes.
5. By default dummy cycle value. Please refer to the *"Table 1. Operating Frequency Comparison"*.
6. Latency time is required to complete Erase/Program Suspend operation until WIP bit is "0".
7. For tPRS, minimum timing must be observed before issuing the next program suspend command. However, a period equal to or longer than the typical timing is required in order for the program operation to make progress.
8. For tERS, minimum timing must be observed before issuing the next erase suspend command. However, a period equal to or longer than the typical timing is required in order for the erase operation to make progress.
9. tDVCH+tCHDX>1.5ns for each SIO; tDVCL+tCLDX>1.5ns for each SIO.
10. Sampled, not 100% tested.

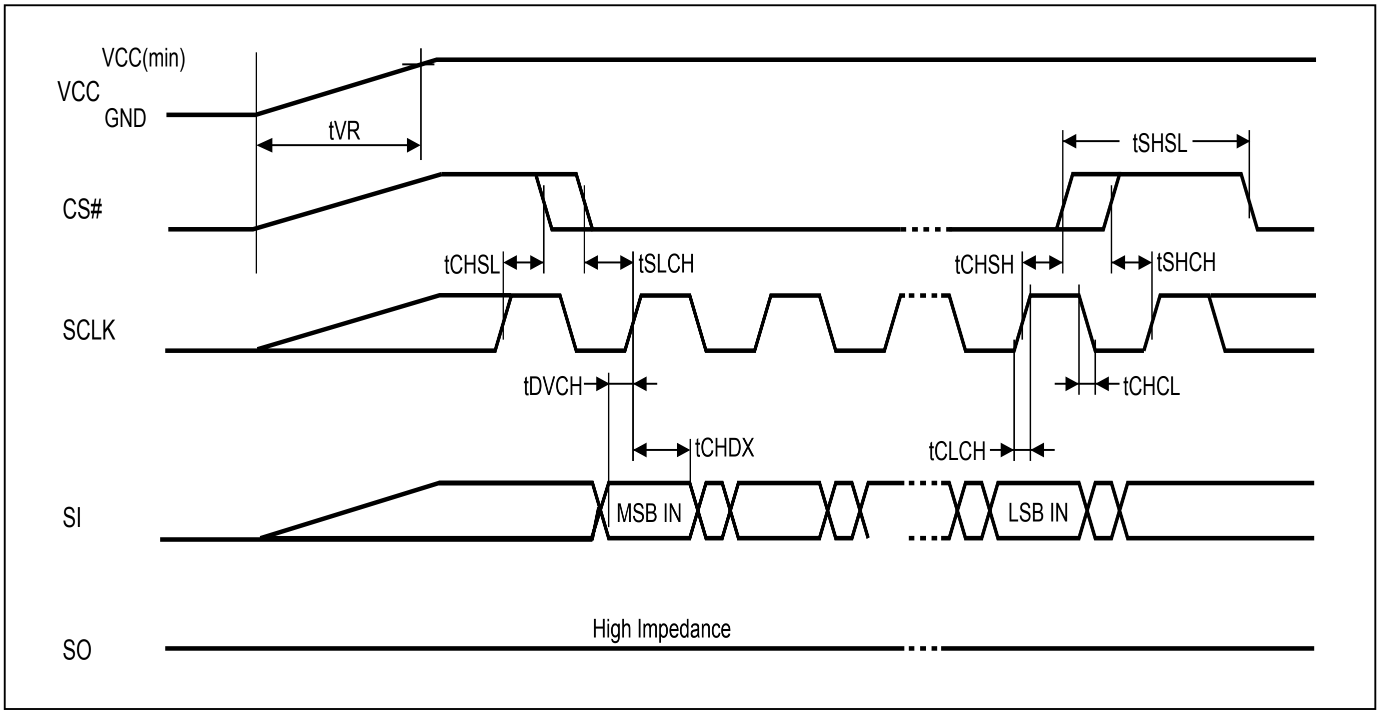
15. OPERATING CONDITIONS

At Device Power-Up and Power-Down

AC timing illustrated in *Figure 113* and *Figure 114* are for the supply voltages and the control signals at device power-up and power-down. If the timing in the figures is ignored, the device will not operate correctly.

During power-up and power-down, CS# needs to follow the voltage applied on VCC to keep the device not to be selected. The CS# can be driven low when VCC reach Vcc(min.) and wait a period of tVSL.

Figure 113. AC Timing at Device Power-Up



Symbol	Parameter	Notes	Min.	Max.	Unit
tVR	VCC Rise Time	1	20	500000	us/V

Notes :
1. Sampled, not 100% tested.
2. For AC spec tCHSL, tSLCH, tDVCH, tCHDX, tSHSL, tCHSH, tSHCH, tCHCL, tCLCH in the figure, please refer to *Table 23.* AC CHARACTERISTICS.

Figure 114. Power-Down Sequence

During power-down, CS# needs to follow the voltage drop on VCC to avoid mis-operation.

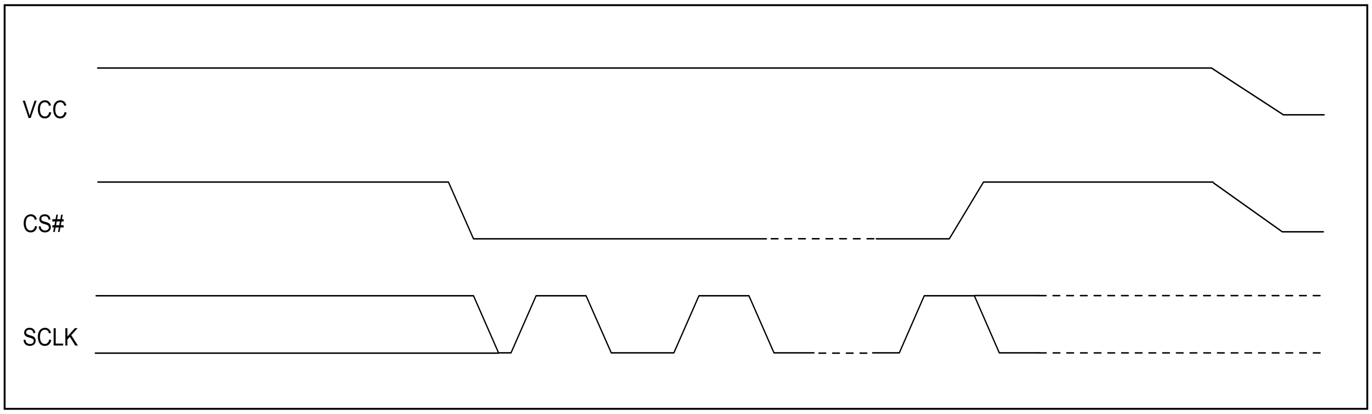


Figure 115. Power-up Timing

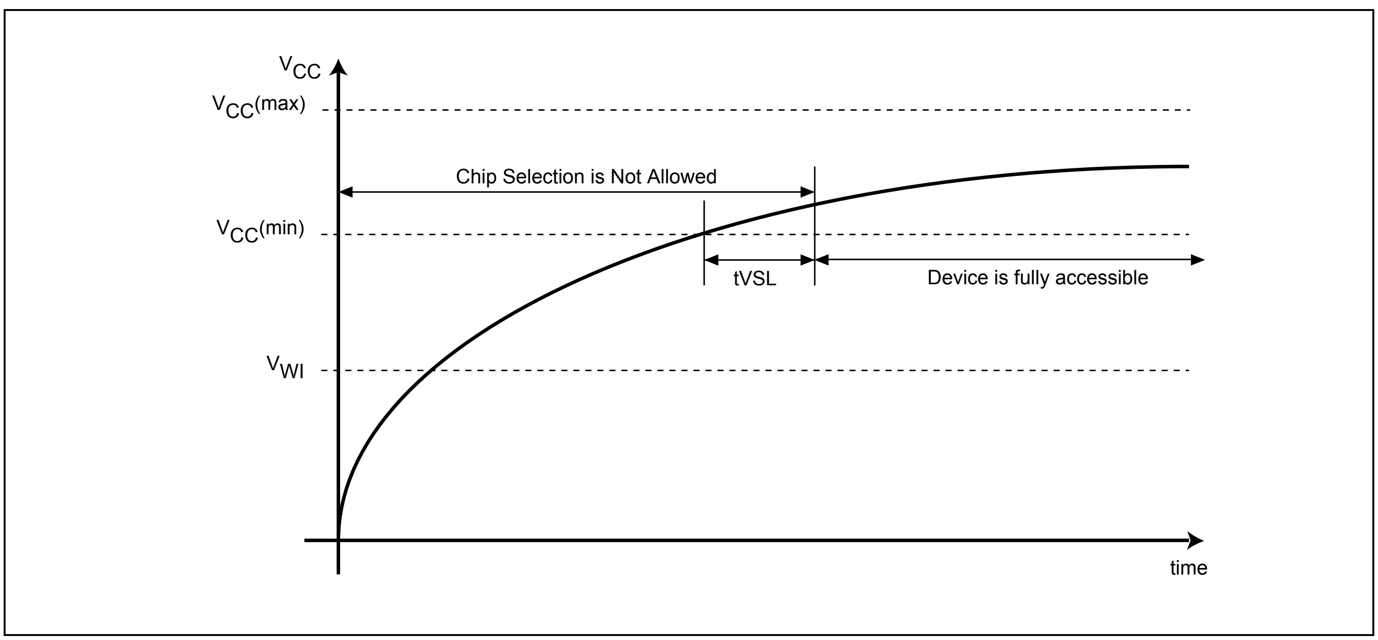


Figure 116. Power Up/Down and Voltage Drop

For Power-down to Power-up operation, the VCC of flash device must below V_{PWD} for at least tPWD timing. Please check the table below for more detail.

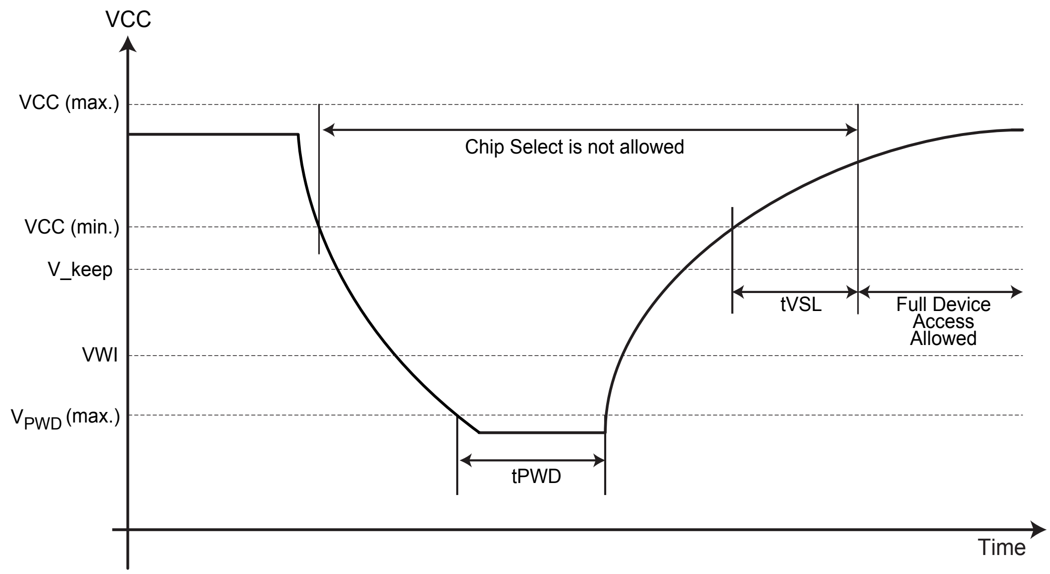


Table 24. Power-Up/Down Voltage and Timing

Symbol	Parameter	Min.	Max.	Unit
V_{PWD}	VCC voltage needed to below V_{PWD} for ensuring initialization will occur		0.9	V
V_keep	Voltage that a re-initialization is necessary if VDD drop below to VKEEP	2.4		V
tPWD	The minimum duration for ensuring initialization will occur	300		us
tVSL	VCC(min.) to device operation	3		ms
tVR	VCC Rise Time	20	500000	us/V
VCC	VCC Power Supply	2.7	3.6	V
VWI	Write Inhibit Voltage	2.0	2.3	V

15-1. INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0). DEFDOPI# in CR2 depends on shipping device model.

16. ERASE AND PROGRAMMING PERFORMANCE

Parameter	Min.	Typ. (1)	Max. (2)	Unit
Write Status Register Cycle Time			40	ms
Sector Erase Cycle Time (4KB)		25	400	ms
Block Erase Cycle Time (64KB)		220	2000	ms
Chip Erase Cycle Time		150	300	s
Page Program Time		0.15	1.5	ms
Erase/Program Cycle		100,000		cycles

Note:
1. Typical program and erase time assumes the following conditions: 25°C, 3V, and checkboard pattern.
2. Under worst conditions of 2.7V.
3. System-level overhead is the time required to execute the first-bus-cycle sequence for the programming command.
4. The maximum chip programming time is evaluated under the worst conditions of 0°C, VCC=3.3V, and 100K cycle with 90% confidence level.

17. DATA RETENTION

Parameter	Condition	Min.	Max.	Unit
Data retention	55˚C	20		years

18. LATCH-UP CHARACTERISTICS

	Min.	Max.
Input Voltage with respect to GND on all power pins		1.5 VCCmax
Input current with respect to GND on all non-power pins	-100mA	+100mA
Test conditions are compliant to JEDEC JDESD78 standard		

19. ORDERING INFORMATION

Please contact our regional sales for the latest product selection and available form factors.

PART NO.	CLOCK (MHz)	TEMPERATURE	PACKAGE	Remark
MX25LM51245GXDI0A	133	-40°C to 85°C	24-Ball BGA (5x5 ball array)	Default x1I/O
MX25LM51245GMI0A	133	-40°C to 85°C	16-SOP (300mil)	Default x1I/O

20. PART NAME DESCRIPTION

MX 25 LM 51245G XD I 0A

MODEL CODE:
0A: Default STR, x1 I/O enable
1A: Default DTR, x8 I/O enable

TEMPERATURE RANGE:
I: Industrial (-40°C to 85°C)

PACKAGE:
XD: 24-Ball BGA (5x5 ball array)
M: 16-SOP (300mil)

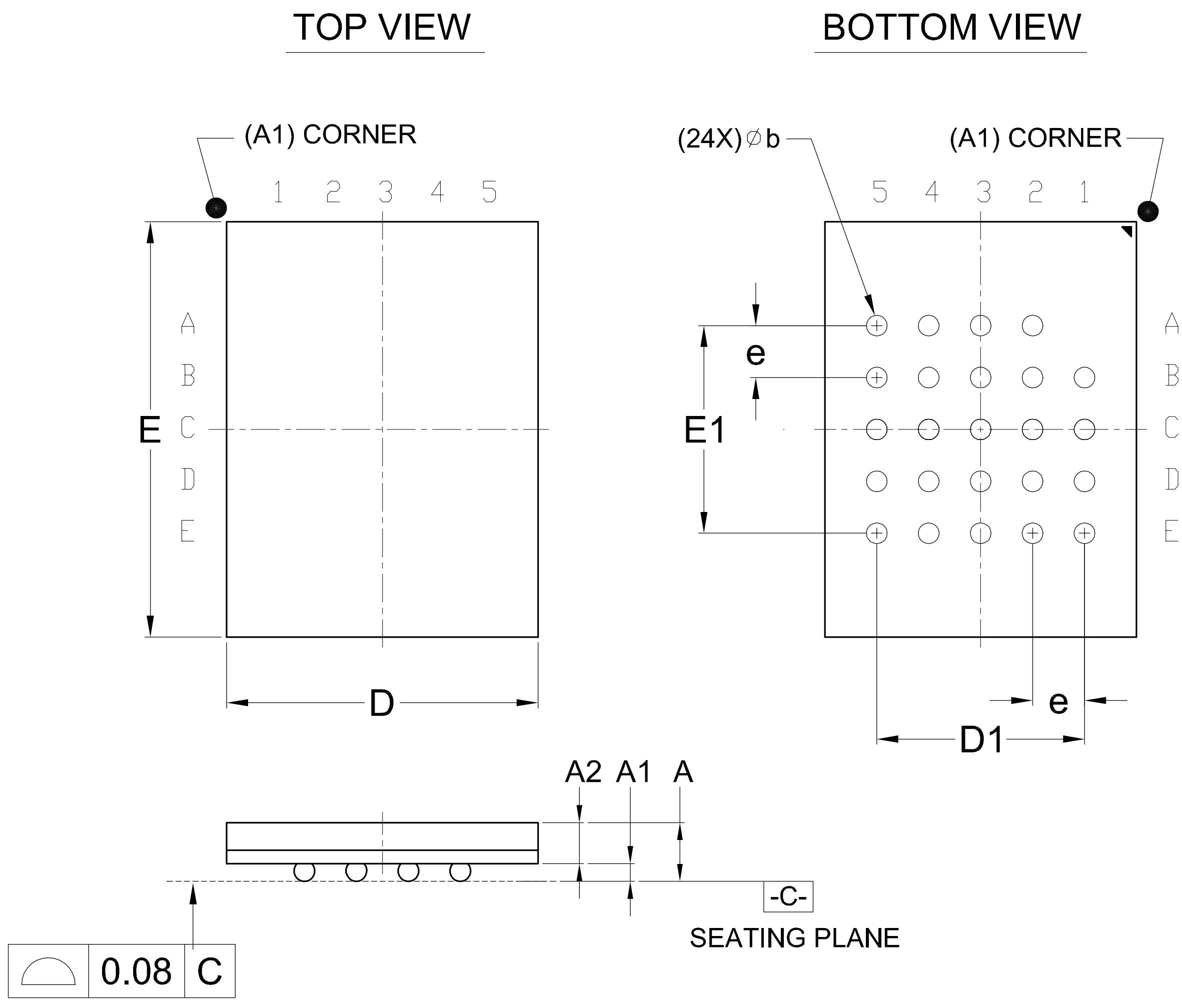
DENSITY & MODE:
51245G: 512Mb

TYPE:
LM: 3V Octa I/O

DEVICE:
25: Serial NOR Flash

21. PACKAGE INFORMATION

Doc. Title: Package Outline for CSP 24BALL (6x8x1.2MM, BALL PITCH 1.0MM, BALL DIAMETER 0.4MM)

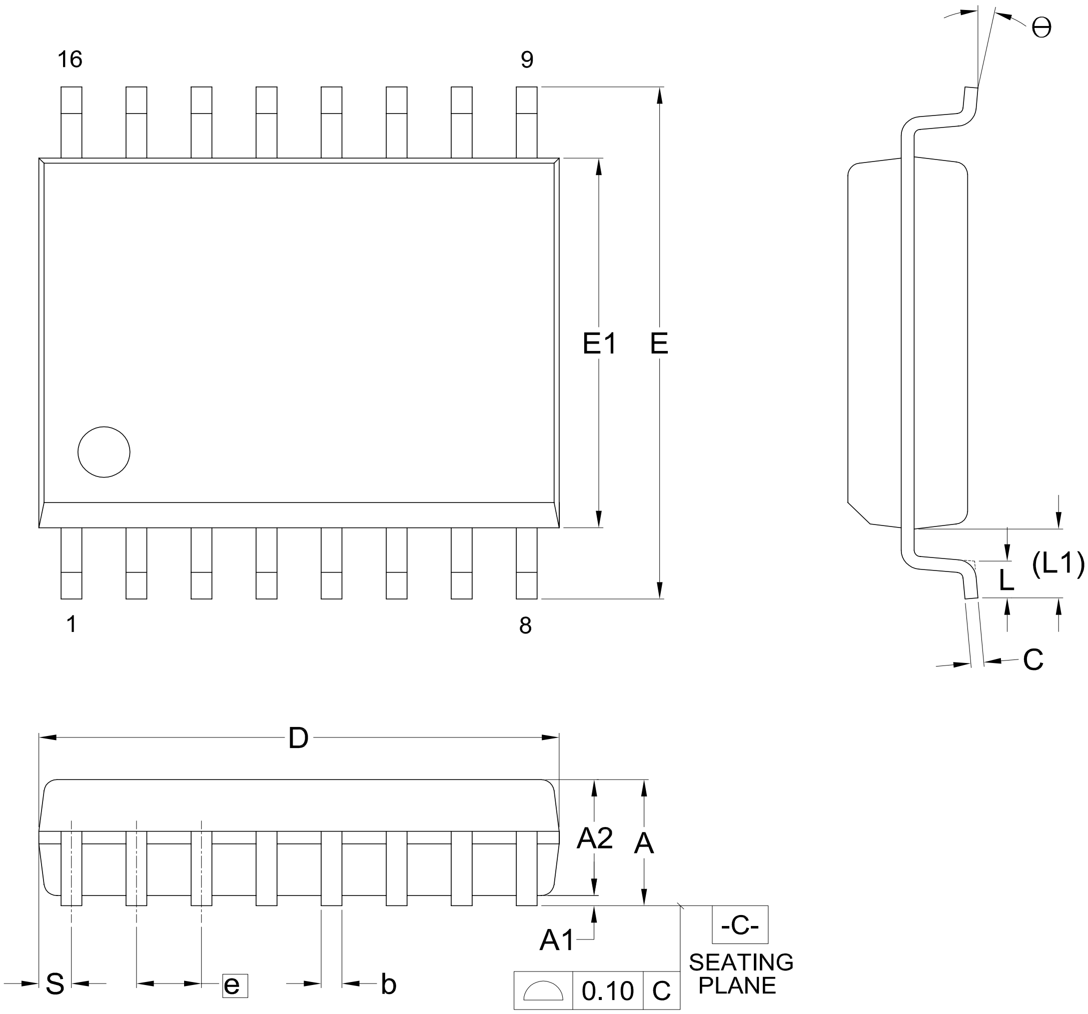


Dimensions (inch dimensions are derived from the original mm dimensions)

UNIT \ SYMBOL		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.25	0.65	0.35	5.90	---	7.90	---	---
	Nom.	---	0.30	---	0.40	6.00	4.00	8.00	4.00	1.00
	Max.	1.20	0.35	---	0.45	6.10	---	8.10	---	---
Inch	Min.	---	0.010	0.026	0.014	0.232	---	0.311	---	---
	Nom.	---	0.012	---	0.016	0.236	0.157	0.315	0.157	0.039
	Max.	0.047	0.014	---	0.018	0.240	---	0.319	---	---

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-4257.1	0				

Doc. Title: Package Outline for SOP 16L (300MIL)



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	E	E1	e	L	L1	S	Θ
mm	Min.	---	0.10	2.25	0.31	0.20	10.10	10.10	7.42	---	0.40	1.31	0.51	0°
	Nom.	---	0.20	2.35	0.41	0.25	10.30	10.30	7.52	1.27	0.84	1.44	0.64	5°
	Max.	2.65	0.30	2.45	0.51	0.30	10.50	10.50	7.60	---	1.27	1.57	0.77	8°
Inch	Min.	---	0.004	0.089	0.012	0.008	0.397	0.397	0.292	---	0.016	0.052	0.020	0°
	Nom.	---	0.008	0.093	0.016	0.010	0.405	0.405	0.296	0.050	0.033	0.057	0.025	5°
	Max.	0.104	0.012	0.096	0.020	0.012	0.413	0.413	0.299	---	0.050	0.062	0.030	8°

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-1402	13	MS-013			

22. REVISION HISTORY

Revision No.	Description	Page	Date
0.01	1. Updated parameters for DC/AC Characteristics	P82-84	MAR/10/2016
	2. Updated Erase and Programming Performance	P88	
	3. Updated CIN & COUT value	P80	
	4. Modified *Figure 3 & Figure 4*	P15	
	5. Added 16-SOP Package information	P6,8,89,90,92	
	6. Content correction	P25,26,46,70,73	

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