USB to Dual Serial Ports Chip CH9103

Datasheet

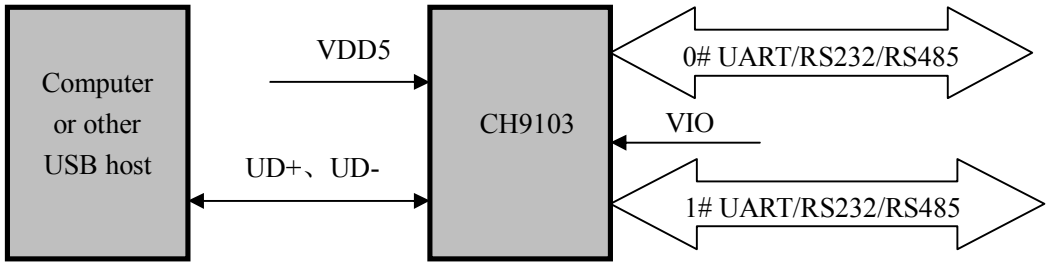
Version: 1A

http://wch.cn

1. Introduction

CH9103 is a USB bus converter chip, which converts USB to dual serial ports.

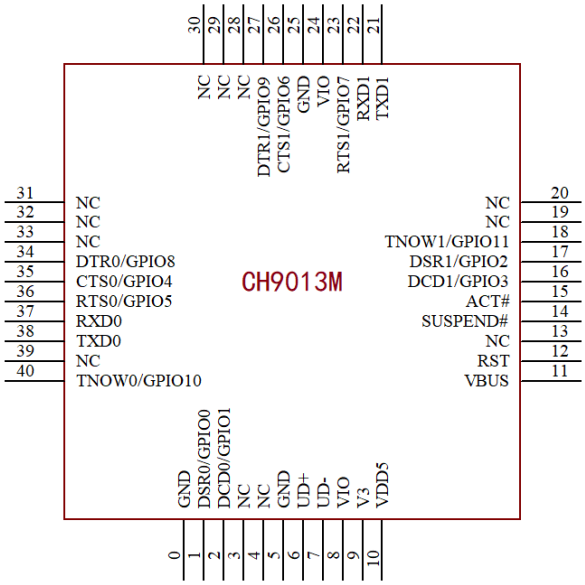
Each UART supports high-speed full-duplex and odd/even parity, provides standard MODEM signals, used to expand serial ports for computer or upgrade directly from normal serial device or MCU to USB bus.



2. Features

- Full-speed USB device interface, USB 2.0 compatible.
- Built-in firmware, emulate standard UART interface, used to upgrade the original serial peripheral or expand additional UART via USB.
- Original serial applications are totally compatible without any modification in Windows operating systems.
- Supports free installation OS which built-in CDC driver or multi-functional high-speed VCP vendor driver.
- Hardware full duplex UART interface, integrated independent transmit-receive buffer, supports communication baud rate varies from 50bps to 3Mbps.
- UART supports 5, 6, 7 or 8 data bits, supports odd, even, space, mark and none parity.
- Supports common MODEM interface signals RTS, DTR, DCD, DSR and CTS.
- Supports CTS and RTS hardware automatic flow control.
- Supports half-duplex, provides sending status TNOW, used for controlling RS485 to transmit-receive switch.
- Supports RS232 interface, through external voltage conversion chip.
- Supports 5V and 3.3V power supply voltages.
- UART interface I/O powered independently, supports 5V, 3.3V, 2.5V, 1.8V power supply voltages.
- Integrated power-on reset, integrated clock, no external crystal required.
- Built-in EEPROM used to configure the chip of VID, PID, maximum current value, vendor and product information string, etc.
- Integrated Unique ID (USB Serial Number).
- RoHS compliant QFN40 lead-free package.

3. Packages



Package	Body size	Lead pitch		Description	Part No.
QFN40_6X6	6*6mm	0.5mm	19.7mil	Square leadless 40-pin patch	CH9103M

Note:

The backplane is 0# pin GND, which is an optional but recommended connection; other GND are necessary connections.

The USB transceiver of CH9103 is designed according to the built-in design of USB2.0, and it is recommended that no external resistor is in series with UD+ and UD- pins.

4. Pin definitions

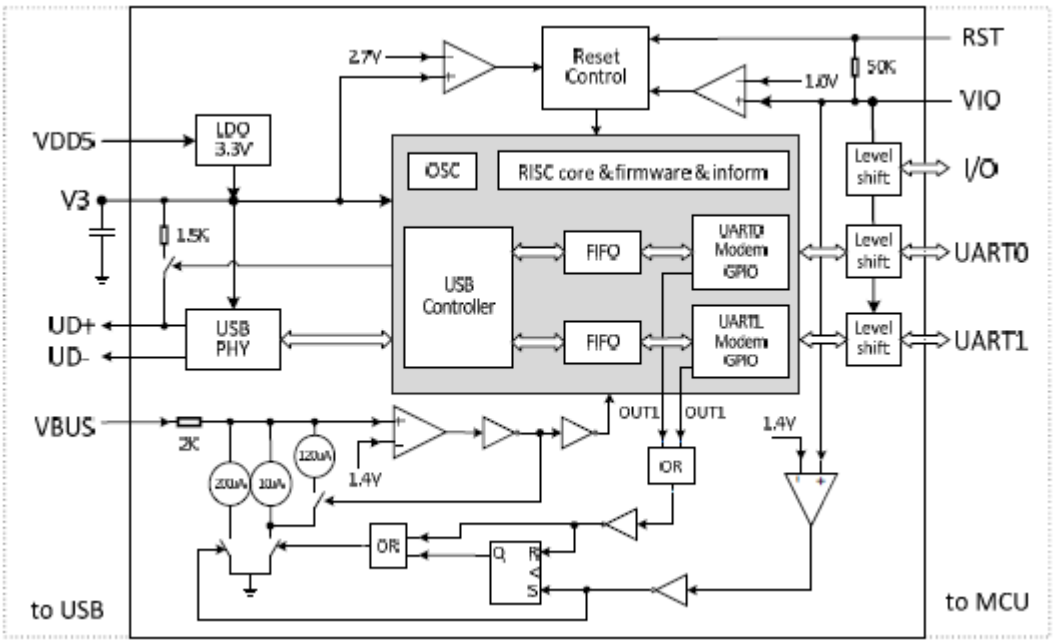
Pin No.	Pin Name	Pin Type	Pin Description
10	VDD5	POWER	Power supply voltage input of power regulator, require an external decoupling capacitor
8, 24	VIO	POWER	I/O Power supply voltage input, require an external decoupling capacitor
0, 5, 25	GND	POWER	Ground, connected to ground of USB bus directly
9	V3	POWER	Internal power regulator output and core and USB power input, When VDD5 voltage is less than 3.6V, connect VDD5 to input the external power supply, an external power decoupling capacitor is required to be connected when the VDD5 voltage is greater than 3.6V
12	RST	IN	Input of external reset, active low, built-in pull-up resistor
6	UD+	USB signal	Connect to USB D+ Signal directly, do not series resistors
7	UD-	USB signal	Connect to USB D- Signal directly, do not series resistors
11	VBUS	IN	VBUS status detect input of USB bus, built-in pull-down resistor

38	TXD0	OUT	Transmit asynchronous data output of UART0, high when idle
37	RXD0	IN	Receive asynchronous data input of UART0, built-in pull-up resistor
35	CTS0/ GPIO4	IN / (IN/OUT)	MODEM input signal, clear to send, active low, general GPIO4, input and output controlled by driver software
34	DTR0/ GPIO8	OUT / (IN/OUT)	MODEM output signal, data terminal ready, active low, general GPIO8, input and output controlled by driver software
36	RTS0/ GPIO5	OUT / (IN/OUT)	MODEM output signal, request to send, active low, general GPIO5, used for IO input or output, Note: if RST0 has detected that an external pull-down resistor is connected during power-on, disable internal EEPROM configuration parameter, enable chip default parameter
40	TNOW0/ GPIO10	OUT / (IN/OUT)	The UART0 sends the status indication in progress, active high, general GPIO10, input and output controlled by driver software, Note: default is disabled TNOW, if TNOW0 has detected that an external pull-down resistor is connected during power-on, enable TNOW
1	DSR0/ GPIO0	IN / (IN/OUT)	MODEM output signal, data set ready, active low, general GPIO0, input and output controlled by driver software
2	DCD0/ GPIO1	IN / (IN/OUT)	MODEM output signal, data carrier detect, active low, general GPIO1, input and output controlled by driver software
21	TXD1	OUT	Transmit asynchronous data output of UART1, high when idle
22	RXD1	IN	Receive asynchronous data input of UART1, built-in pull-up resistor
26	CTS1/ GPIO6	IN / (IN/OUT)	MODEM input signal, clear to send, active low, general GPIO6, input and output controlled by driver software
27	DTR1/ GPIO9	OUT / (IN/OUT)	MODEM output signal, data terminal ready, active low, general GPIO9, input and output controlled by driver software
23	RTS1/ GPIO7	OUT / (IN/OUT)	MODEM output signal, request to send, active low, general GPIO7, used for IO input or output,
18	TNOW1/ GPIO11	OUT / (IN/OUT)	UART 1 sends an ongoing status indication, active high, general GPIO11, input and output controlled by driver software
17	DSR1/ GPIO2	IN / (IN/OUT)	MODEM output signal, data set ready, active low, general GPIO2, input and output controlled by driver software
16	DCD1/ GPIO3	IN / (IN/OUT)	MODEM output signal, data carrier detect, active low, general GPIO3, input and output controlled by driver software
15	ACT#	OUT	USB configuration completed status output, active low, invalid when suspend
14	SUSPEND#	OUT	USB suspend state output, active low, normal working state output high level, output low level after suspension

3,4,13,19,20,28,29,30,31,32,33,39	NC	None	No connection, must be suspended

5. Function descriptions

5.1. Internal structure



5.2. Power and power consumption

CH9103 has 3 power supplies, built-in power regulator that generates 3.3V. VDD5 is the input of power regulator, V3 is the output of power regulator and USB transceiver and core power supply input, and VIO is the I/O power supply.

CH9103 supports 5V or 3.3V supply voltage, the V3 should be connected to an external power decoupling capacitor of about 0.1uF. When using 5V power supply(more than 3.8V), VDD5 inputs external 5V power supply (for example, the USB bus power supply), the internal power regulator generates 3.3V on V3 which used for USB transceiver. When using 3.3V or lower operating voltage (less than 3.6V), V3 should be connected to VDD5, and input external 3.3V power supply simultaneously. V3 still need to connect with an external power decoupling capacitor.

The VIO pin of CH9103 is used to provide I/O power supply for I/O and RST pin and supports 1.8V~5V supply voltage. VIO, MCU and other peripheral devices should use the same power supply. UD+, UD- and VBUS use V3 power supply, not use VIO.

CH9103 supports automatically USB device suspension to save power consumption. In the USB suspend status, if the I/O output pin has not external load, I/O input pin is floating (internal pull-up) or at a high level status, then VIO power supply will not consume current. In addition, when V3 and VDD5 lose power supply and are at 0V, the current consumption situation of VIO is the same as above, and VIO will not flow backwards current to VDD5 or V3.

VBUS should be connected to USB bus power supply, and when the missing of USB power is detected, CH9103 will turn off the USB and to sleep (suspend). The built-in pull-down resistor of VBUS pin can be

controlled by computer software which setting OUT1 signal of MCR register (SERIAL_IOC_MCR_OUT1). Turning on the pull-down resistor when OUT1 is invalid (default) or turning off it when OUT1 is valid.

CH9103 provides VIO low-voltage protection mechanism when VBUS connects resistor in series which used to control VIO power through PMOS. During the shutdown of the VBUS pull-down resistor, if VIO voltage is lower than about 1.4V which is detected, then CH9103 will automatically absorb about 300uA discharge current on VBUS, until the VIO voltage rises and the discharge current finished, starting the pull-down resistor automatically.

Several power supply connection schemes for reference here:

<table>
<tr><td rowspan="2">Power supply scheme</td><td rowspan="2">UART signals voltage
MCU operating voltage</td><td>VDD5</td><td>V3</td><td>VIO</td><td>MCU or peripheral power supply</td></tr>
<tr><td>Not less than V3 voltage</td><td>Rated around 3.3V</td><td colspan="2">Both use the same power supply, 1.8V～5V</td></tr>
<tr><td rowspan="4">All USB power supply</td><td>5V</td><td>USB powered 5V</td><td>Only connect to capacitor</td><td colspan="2">USB powered 5V</td></tr>
<tr><td>3.3V</td><td>USB powered 5V</td><td>Connect to capacitor</td><td colspan="2">Powered by V3 for 3.3V, up to 10mA</td></tr>
<tr><td>3.3V</td><td colspan="4">USB 5V power stepped down to 3.3V via external LDO power regulator, V3 connects to external capacitor</td></tr>
<tr><td>1.8V～4V</td><td>USB powered 5V</td><td>Only connect to capacitor</td><td colspan="2">USB powered, step-down via external LDO regulator</td></tr>
<tr><td>USB+ self-powered Dual power supply</td><td>1.8V～5V</td><td>USB powered 5V</td><td>Only connect to capacitor</td><td colspan="2">Self-powered 1.8V～5V (1.8V,2.5V,3.3V,5V)</td></tr>
<tr><td rowspan="2">All self-powered</td><td>4V～5V</td><td>Self-powered 4V～5V</td><td>Only connect to capacitor</td><td colspan="2">Self-powered 4V～5V</td></tr>
<tr><td>1.8V～5V</td><td colspan="2">Self-powered, rated 3.3V, connects to external capacitor</td><td colspan="2">Self-powered 1.8V～5V</td></tr>
</table>

Recommended dual power supplies scheme, only VIO and MCU use the same power supply, low-current consumption VIO current is only 2uA when USB suspend or sleep.

5.3. UART description

In UART mode, CH9103 contains: data transfer pins, MODEM interface signal pins and assistant pins.

Data transfer pins contain: TXD and RXD. RXD is high when UART input is idle. TXD is high when UART output is idle.

MODEM interface signals contain: CTS, DSR, DCD, DTR and RTS. All these MODEM interface signals are controlled and defined function by computer applications.

Assistant pins contain: SUSPEND# and ACT#, etc.

SUSPEND# is the output pin of chip suspend status. When the chip is in a normal operating status, SUSPEND# outputs a high level, and SUSPEND# outputs a low level when the chip is in a suspend status.

ACT# is output pin of the USB device configuration completed status, which can be used to notify MCU or drive connected to the LED of VIO after connecting the current limiting resistor in series.

If installing VCP vendor driver, some pins can map to common GPIO function.

The UART of CH9103 supports CTS and RTS hardware automatic flow control, which can be enabled by software. If enabled, UART only will continue to send the next data when CTS input is valid (active low), otherwise the UART transmission will be stopped; UART will automatically set RTS to be valid (active low) when the receiving buffer is empty, it will automatically invalidate RTS until the data in the receiving buffer is nearly full, and RTS will be valid again when the buffer is empty. While using hardware automatic flow control, CTS of CH9103 should connect to RTS of the counterpart, and RTS of CH9103 should connect to CTS of the counterpart.

CH9103 has integrated separate transmit-receive buffer and supports simplex, half-duplex and full-duplex UART communication. UART data contains a low-level start bit, 5, 6, 7 or 8 data bits and 1 or 2 high-level stop bits, supports odd/even/mark/space parity. CH9103 supports common communication baud rate: 50, 75, 100, 110, 134.5, 150, 300, 600, 900, 1200, 1800, 2400, 3600, 4800, 9600, 14400, 19200, 28800, 33600, 38400, 56000, 57600, 76800, 115200, 128000, 153600, 230400, 256000, 307200, 460800, 1M, 1.5M, 2M, 3M, etc.

In applications with higher communication baud rate, it is recommended to enable hardware automatic flow control. Full-speed USB is only 12Mbps. Considering the protocol spending and other factors, in practical applications, the dual UARTs should be avoided in a continuous or full-duplex of 1Mbps and above high-speed communication status at the same time.

The allowable baud rate error of CH9103's UART reception is not more than 2%, the baud rate error of UART transmission is less than 1.5%.

On operating systems, CH9103 supports CDC class driver that comes with system, and VCP manufacturer driver could be installed to support high speed communication and other functions. It can simulate the standard serial port, so most serial port applications are fully compatible, usually without any modification.

CH9103 can be used to upgrade the original UART peripheral devices, or expand extra UART for computers via USB bus, provides further RS232, RS485, RS422 interface, etc. through external voltage conversion chip.

5.4. Clock, reset and others

CH9103 has a built-in USB pull-up resistor, and the UD+ and UD- pins should be directly connected to the USB bus.

CH9103 has a built-in power-on reset circuit, and also provides an external reset input pin with active low level. When the RST pin is at a low level, CH9103 will be reset; when the RST pin returns to a high level, CH9103 internal will continue to delay reset for about 15mS, and then enter the normal working state

CH9103 has a built-in low-voltage reset circuit, and monitors the voltage of the V3 pin and VIO pin at the same time. When the voltage of V3 is lower than VRV3 or the voltage of VIO is lower than VRVIO, the chip will automatically reset by hardware.

CH9103 has built-in clock generator, without external crystal and oscillation capacitor.

5.5. Parameter configuration

In larger batch applications, the vendor identification code (VID) and product identification code (PID) of CH9103 and product information can be customized.

In less batch applications, parameters can be configured by built-in EEPROM. After installs VCP vendor driver, through configuration tool CH34xSerCfg.exe provided by chip manufacturer, it can be flexibly configured the identification code (VID), product identification code (PID), maximum current value, BCD version number, manufacturer information and product information string and other descriptor, etc.

6. Parameters

6.1. Absolute maximum ratings

(Operating in critical ratings or exceeding the absolute maximum ratings may cause chip to not work or even be damaged)

Name	Parameter Description	Min.	Max.	Unit
TA	Operating ambient temperature	-40	85	℃
TS	Storage temperature	-55	125	℃
VDD5	USB power supply voltage(VDD5 connects to power, GND connects to ground)	-0.5	6.0	V
VIO	Serial port I/O power supply voltage(VIO connects to power, GND connects to ground)	-0.5	6.0	V
VVBUS	VBUS voltage	-0.5	6.5	V
VUSB	USB signal voltage	-0.5	V3+0.5	V
VUART	Voltage on UART and other pins	-0.5	VIO+0.5	V

6.2. Electrical parameters

(Test conditions: TA=25℃,VDD5=5V or VDD5=V3=3.3V, VIO=1.8V~5V, exclude USB pin)

Name	Parameter Description		Min.	Typ.	Max.	Unit
VDD5	USB power supply voltage	V3 doesn't connect to VDD5, V3 connects to capacitor	4.0	5	5.5	V
		V3 connects to VDD5, VDD5=V3	3.0	3.3	3.6	V
VIO	Serial port and other I/O power supply voltage		1.7	5	5.5	V
IVDD	Operating VDD5 or V3 power supply current			3	15	mA
IVIO	Operating VIO power supply current(depend on I/O load)			0	(10)	mA
ISLP	The supply current when USB is suspended	VDD5 power supply =5V		0.09	0.16	mA
		VDD5=V3 power supply =3.3V		0.085	0.15	mA
		VIO power supply, no I/O load/pull up		0.002	0.05	mA
ILDO	External load capacity of internal power regulator				10	mA
VIL	Input high voltage	VIO=5V	0		1.5	V

		VIO=3.3V	0		0.9	V
		VIO=1.8V	0		0.5	V
VIH	Input high voltage	VIO=5V	2.5		VIO	V
		VIO=3.3V	1.9		VIO	V
		VIO=1.8V	1.3		VIO	V
VIHVBS	high-level voltage of VBUS pin	VIO=1.8～5V	1.7		5.8	V
VOL	Output low voltage	VIO=5V, 15mA draw current		0.4	0.5	V
		VIO=3.3V, 8mA draw current		0.3	0.4	V
		VIO=1.8V, 3mA draw current		0.3	0.4	V
VOH	Output high voltage, non-reset status	VIO=5V, 10mA output current	VIO-0.5	VIO-0.4		V
		VIO=3.3V, 5mA output current	VIO-0.4	VIO-0.3		V
		VIO=1.8V, 2mA output current	VIO-0.4	VIO-0.3		V
IPUP	Pull-up current of serial port and RST pin (pull-up to VIO voltage)	VIO=5V	35	150	220	uA
		VIO=3.3V	15	60	90	uA
		VIO=1.8V	3	14	21	uA
IPDN	Pull-down current of VBUS pin	VBUS>1.6V	6	10	16	uA
		VBUS<1.3V	50	140	200	uA
VRV3	V3 Power-on reset/low voltage reset voltage threshold		2.5	2.7	2.9	V
VRVIO	VIO power supply low voltage reset voltage threshold		0.8	1.0	1.15	V
VESD	HBM ESD withstand voltage on USB or I/O pins		5	6		KV

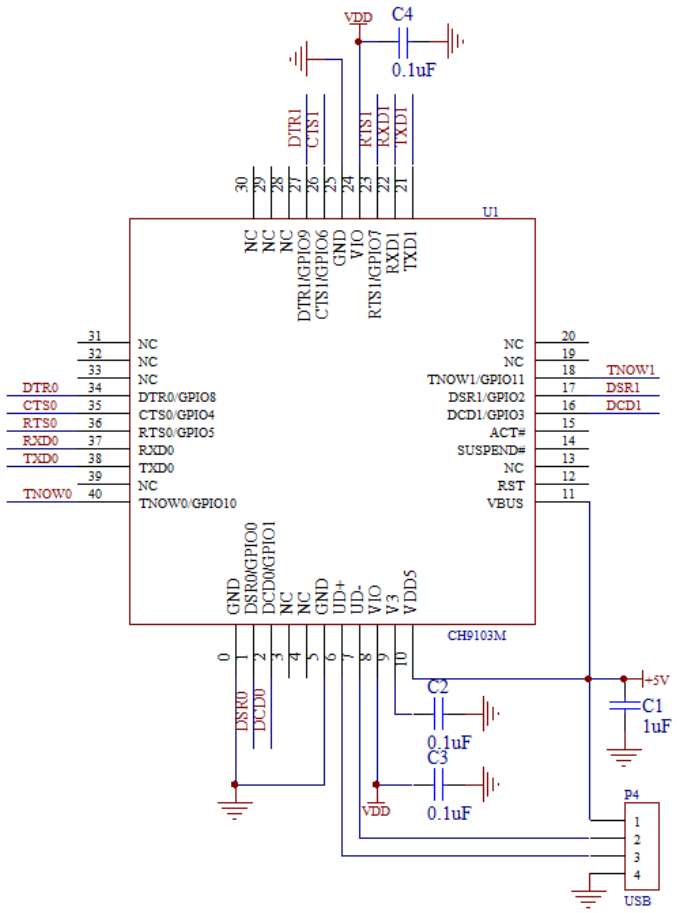
6.3. Timing parameters

(Test conditions: TA=25℃,VDD5=5V or VDD5=V3=3.3V, VIO=1.8V～5V)

Name	Parameter Description		Min.	Typ.	Max.	Unit
FD	Error of internal clock (influence baud rate comparatively)	TA=-15℃～60℃	-1.0	±0.5	+1.0	%
		TA=-40℃～85℃	-1.5	±0.8	+1.5	%
TRSTD	Reset delay after power on or external reset input		9	15	25	mS
TRI	Effective signal width of RST external reset input		100			nS
TSUSP	Detect USB automatic suspend time		3	5	9	mS
TWAKE	Wake-up completion time after chip sleep		1.2	1.5	5	uS

7. Applications

7.1. USB to Dual 9-line TTL UART



The figure above is the USB to TTL converter realized by CH9103. Only RXD, TXD and public ground are necessary connection, while the others are optional.

P4 is USB port, USB bus contains a pair of 5V power lines and a pair of data signals. Usually, the color of +5V power line is red, the black one is ground. D+ signal line is green and the D- signal line is white. The max supply current of USB bus is up to 500mA. The VBUS pin detects the USB power supply status here.

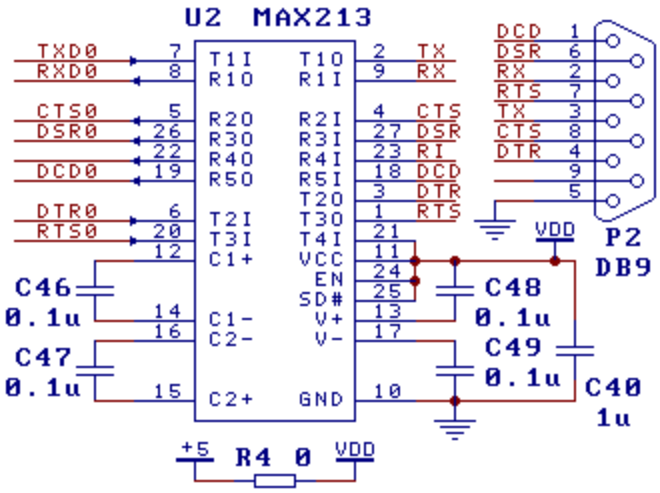
The capacitor C2 on V3 is 0.1uF which is used for CH9103 internal power node decoupling. C1, C3 and C4 are used for external power decoupling.

In application, if VIO has connected to V3, capacitor C3 cannot need. In VIO=V3=VDD5 all self-powered 3.3V case, capacitor C2 and C3 can be omitted.

Three power supply schemes: One is all USB power supply, CH9103 and USB products directly use the 5V power supply provided by the USB bus, that is, VDD5=VBUS=USB 5V power, VIO=VMCU=USB 5V or 1.8V~4V after step-down; The second is separate and independent power supply. The VIO of CH9103 and the MCU of the product use self-supplied standing power VDD, while CH9103 uses USB power, and its VDD5 is connected to the USB power, that is, VDD5=USB 5V power, VIO=VMCU=VDD= self-supply 1.8V~5V; The third is all self-powered, only detecting but not using USB power, USB products provide power VDD through self-powered mode, mainly VDD5=VIO=VMCU=VDD=self-supplied 5V or VDD5=V3=VIO=VMCU=VDD=self-supplied 3.3 V two kinds.

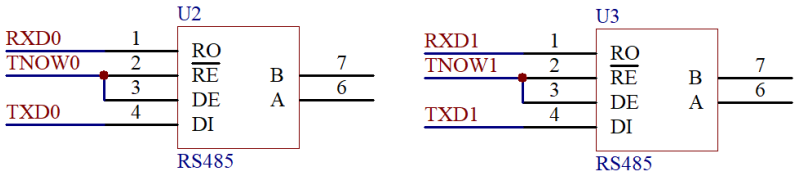
When designing the PCB, pay attention to: decoupling capacitor C1,C2,C3 and C4 should be as close as possible to the connected pins of CH9103; The D+ and D- signal lines are placed close to the parallel wiring, and ground or copper should be provided on both sides to reduce signal interference from the other parts.

7.2. USB to Dual 9-line RS232 UART



CH9103 provides common UART signals and MODEM signals, converts one of TTL to RS232 through level conversion chip U2, the other one is similar with this. Port P2 is DB9 connector, the pins and their functions are the same as common PC DB9 connector, the chips similar with U2 have MAX213/ADM213/SP213/MAX211 etc.U2 in the image is uniformly powered by the USB bus through R4.

7.3. USB to Dual RS485 UART



In the figure, TNOW is the switch pin, the TNOW pin can be used to control DE (active high and transmit enabled) and RE# (active low and receive enabled) pin of RS485 transceiver. RS485 transceiver should use the same power supply as VIO.